T-52-33-90

LH5045 CMOS Real Time Clock LSI

■ Description

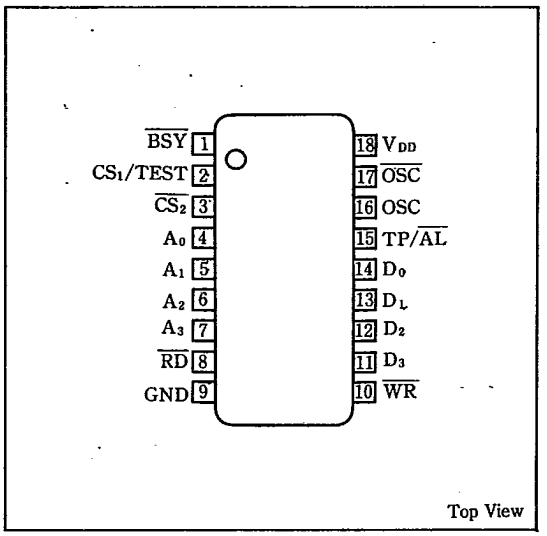
The LH5045 is a CMOS real time clock LSI for microprosessor with time and calendar data I/O facilities.

It may be accessed to read/write in the same way as static memory.

■ Features

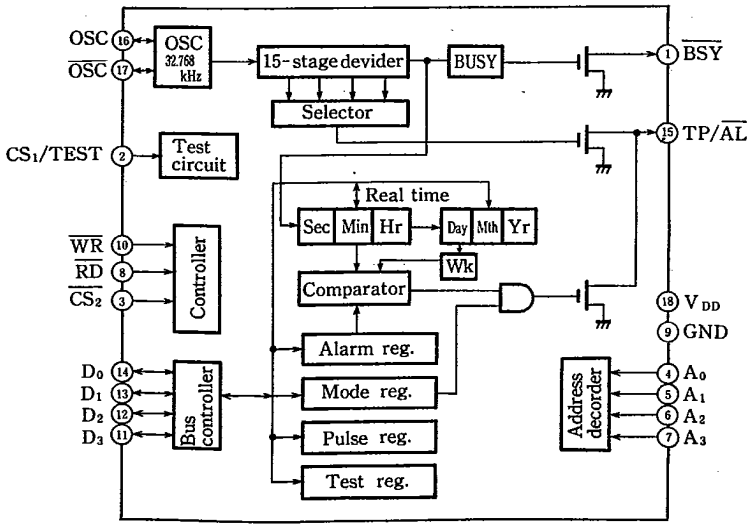
1. On-chip counter for real-time (hour: minute: second) and date (day, date, month, year).
2. 4-bit parallel I/O data in BCD.
3. Automatic leap year processing.
4. Switchable between 24-hour clock and 12-hour with AM/PM clock.
5. Battery backup capability.
5. Alarm feature.
6. 18-pin dual-in-line package.

■ Pin Connections



Top View

■ Block Diagram



Note : $\overline{BSY}$, D_0-D_3 and TP/$\overline{ALARM}$ pins are open drain outputs.

■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3 to +6	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	−10 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

■ Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	4.5		5.5	V
Data holding voltage	V_{DH}	2.2		5.5	V
Crystal frequency	f_{xt}		32.768		kHz

■ DC Characteristics (V_{DD}=5V±5%, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH1}		2.0			V	1
	V_{IH2}		V_{DD}−0.5			V	2
Input "Low" voltage	V_{IL}				0.8	V	
Output "Low" voltage	V_{OL}	I_{OL}=2mA			0.4	V	4
Input "High" current	I_{IH}	V_I=5V			1	μA	3
Input "Low" current	I_{IL}	V_I=0V	−100			μA	3
Off leakage current (D_0-D_3 inputs)	I_{LIH}/I_{LIL}	V_I=5V			5	μA	
		V_I=0V	−5				
Current consumption	I_{DD}	V_{DD}=5V		30	120	μA	
		V_{DD}=3V		5	20		

Note 1 : Applied to pins $\overline{CS_2}$, $\overline{WR}$, $\overline{RD}$, A_0-A_3, and D_0-D_3 pins.
Note 2 : Applied to pins CS_1/TEST pin
Note 3 : Applied to pins A_0-A_3, $\overline{RD}$, $\overline{WR}$, $\overline{CS_2}$, and CS_1/TEST pins.
Note 4 : Applied to pins D_0-D_3, TP/$\overline{ALRM}$, and $\overline{BSY}$pins.

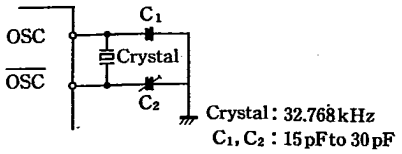
■ AC Characteristics (V_{DD}=5V±5%, Ta=−10 to +70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	0.1			μs
Address hold time	t_{AH}	0.2			μs
RD/WR pulse width	t_W	1.4			μs
Read access time	t_{RA}			*	μs
Read data hold time	t_{RH}			0.4	μs
Write data setup time	t_{WS}	0.35			μs
Write data hold time	t_{WH}	0			μs

*t_{RA}=1μs+CR. ln[V_{DD}/(V_{DD}−V_{IH})]
C: Wiring stray capacity on data bus lines
R: Pull-up resistor
V_{IH} : MAX. input high voltage for devices connected to data bus lines.
ln: Natural logarithm

■ Pin Descriptions

(1) OSC, $\overline{OSC}$ pin



(2) CS_1/TEST pit (active High) (normally used at High level.)

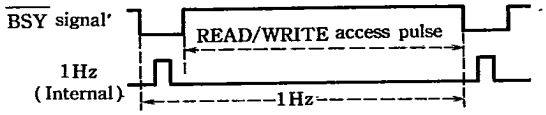
This pin accepts a test clock signal or a power-down detection signal. It should normally be connected to the power-down detector output.

(3) $\overline{CS_2}$ pin (active Low)

This pin accepts a Chip Select signal for the device.

(4) $\overline{BSY}$ pin (active Low)

This pin provides an internal device status signal. Device's internal counters are incrementing when this pin is at Low. If the device is to be accessed without using this pin, read access must be attempted twice consecutively so that only matched data be taken as read data; write access should always be followed by read access to verify write data integrity.



(5) A_0-A_3 D_0-D_3 pins (active High)

Pins A_0-A_3 are address inputs; D_0-D_3 are data I/O pins.

(6) $\overline{RD}$ pin (active Low)

This pin accepts an $\overline{RD}$ signal. Data is output from an internal counter or register selected by address information to the data I/O pins while the RD pin is kept at Low. This output operation should, as a rule, be executed when the $\overline{BSY}$ signal is at High.

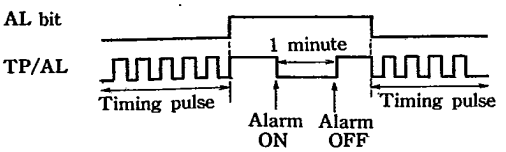
(7) $\overline{WR}$ pin (active Low)

When the time counter or register requires initial preset or correction, the $\overline{WR}$ signal applied to this pin should be set to Low to write time data. This input operation should, as a rule, be executed when the $\overline{BSY}$ signal is at High.

(8) TP/$\overline{ALRM}$ pin ($\overline{ALRM}$ active Low)

This pin serves as both Timing Pulse output and Alarm On signal output. The Timing Pulse (TP) may be selected from four frequencies (duty 50%) by setting the TP register:

The active-Low Alarm On signal is asserted when the realtime clock data matches the Alarm-On register value. Whether or not the coincidence signal is to be output to the TP/$\overline{ALRM}$ pin can be controlled by setting (output enable) or resetting (output disable) the AL bit of the Mode register. When the AL bit is reset, this pin always provides Timing Pulse.



Any of the alarm registers may be masked from comparison For example, if the Day register is masked, alarm can be activated every day. The following table shows the mask bit status.

■ Function Table

Address in hex.	MODE 0								MODE 1				
	Address input pins				Contents	Data I/O pins				Contents	Data I/O pins			
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0		D_3	D_2	D_1	D_0
0	0	0	0	0	S_1 counter	○	○	○	○	—	×	×	×	×
1	0	0	0	1	S_{10} counter	×	○	○	○	—	×	×	×	×
2	0	0	1	0	Mi_1 counter	○	○	○	○	Alarm ON Mi_1 register	○	○	○	○
3	0	0	1	1	Mi_{10} counter	×	○	○	○	Alarm ON Mi_{10} register	×	○	○	○
4	0	1	0	0	H_1 counter	○	○	○	○	Alarm ON H_1 register	○	○	○	○
5	0	1	0	1	H_{10} counter	×	■	▲	○	Alarm ON H_{10} register	×	×	○	○
6	0	1	1	0	W counter	×	○	○	○	Alarm ON W register	×	○	○	○
7	0	1	1	1	D_1 counter	○	○	○	○	—	×	×	×	×
8	1	0	0	0	D_{10} counter	◎	◎	○	○	—	×	×	×	×
9	1	0	0	1	MO_1 counter	○	○	○	○	—	×	×	×	×
A	1	0	1	0	MO_{10} counter	×	×	×	○	—	×	×	×	×
B	1	0	1	1	Y_1 counter	○	○	○	○	—	×	×	×	×
C	1	1	0	0	Y_{10} counter	○	○	○	○	—	×	×	×	×
D	1	1	0	1	MODE register	×	SP	AL	M	MODE register	×	SP	AL	M
E	1	1	1	0	TEST register	T_3	T_2	T_1	T_0	TEST register	T_3	T_2	T_1	T_0
F	1	1	1	1	TP register	×	×	P_1	P_0	TP register	×	×	P_1	P_0

Note 1 : Mark "○" in the data I/O pin columns indicates valid bits.
Mark "×" in the same columns indicates invalid bits, which are set at Low when read.

D_2	D_1	Contents
0	0	AM for 12H clock
0	1	PM for 12H clock
1	0	(00-19) hour for 24H clock
1	1	(20-23) hour for 24H clock

Note 2 : The bit marked "■" is used for selecting $\overline{12}$/24-hour clocks.
The bit marked "▲" is used to select AM/PM for $\overline{12}$ hour clocks, and as the tens digit data bit for 24-hour clock.

Year	D_3	D_2	Remainder of (year ÷ 4)
Dominical year	0	0	0
ERA3	0	1	3
ERA2	1	0	2
ERA1	1	1	1

Note 3 : The bits marked "◎" are used to select leap year.
Note 4 : The MODE, TEST, and TP registers are write-only registers. All bits will be set at Low if they are read.

Day of the week	W counter
Sunday	0
Monday	1
⋮	⋮
Saturday	6

Note 5 : Day of the week is given by a number from 0 to 6.

■ Register Contents

(1) Mode register

D_3	D_2	D_1	D_0
×	SP	AL	M

- 0 MODE$_0$ function
- 1 MODE$_1$ function
- 0 ALARM output disable
- 1 ALARM output enable
- 0 Real time counter start
- 1 Real time counter stop

(2) Test register

D_3	D_2	D_1	D_0
T_3	T_2	T_1	T_0

- 0 TEST MODE$_0$ disable
- 1 TEST MODE$_0$ enable
- 0 TEST MODE$_1$ disable
- 1 TEST MODE$_1$ enable
- 0 TEST MODE$_2$ disable
- 1 TEST MODE$_2$ enable
- 0 TEST MODE$_3$ disable
- 1 TEST MODE$_3$ enable

Note : If any one of bits of this Test register is set to 1 at power on, the device will enter the Test mode. Be sure to reset all bits to (0000) to clear the Test mode.

(3) TP register

D_3	D_2	D_1	D_0
×	×	P_1	P_0

P_1	P_0	Output pulse (Hz)
0	0	1
0	1	64
1	0	256
1	1	1024

(4) Alarm register

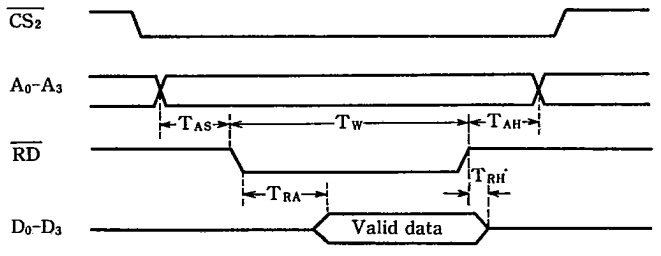
(To set each bit inactivates corresponding bit of the register.)

Alarm register name	Mask status D_3	D_2	D_1	D_0	Interval output (AL=1)
Day of the week	X	1	1	1	Daily
Hour (tens digit)	X	1*	X	X	Hourly
Hour (ones digit)	1	1	1	1	Interval of 10 minutes
Minuts (tens digit)	X	1	1	1	Usually output Low level
Minuts (ones digit)	1	1	1	1	

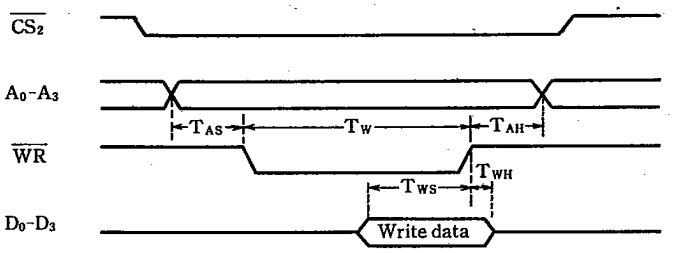
Note: For the tens dight register of hour, bit D_2 is used for masked (1) and unmasked (0) control.
X : Don't care

■ Timing Diagram

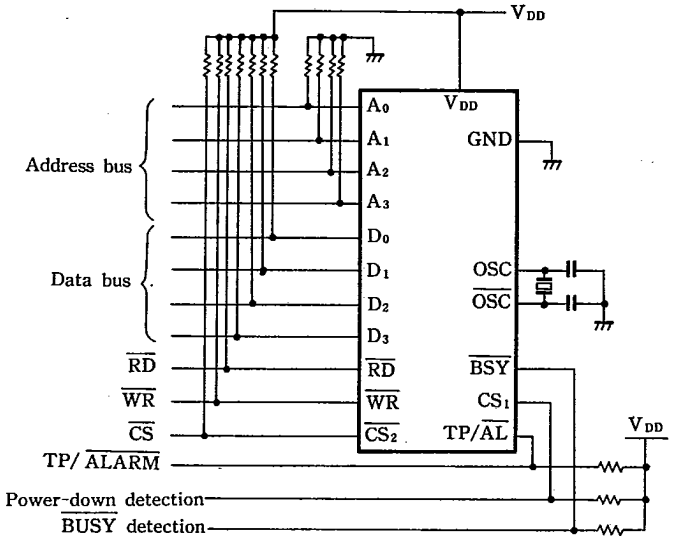
(1) Write Mode (CS_1=H)



(2) Read Mode (CS_1=H)

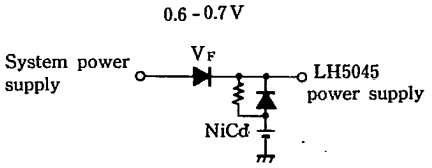


■ Basic Connection Diagram



■ Power Switching Circuit Examples

(Example 1)



(Example 2)