

LH50506/N

CMOS 8-Bit A/D Converter

DESCRIPTION

LH50506/N is an 8-bit flash A/D converter using high-speed 0.8 μm CMOS process.

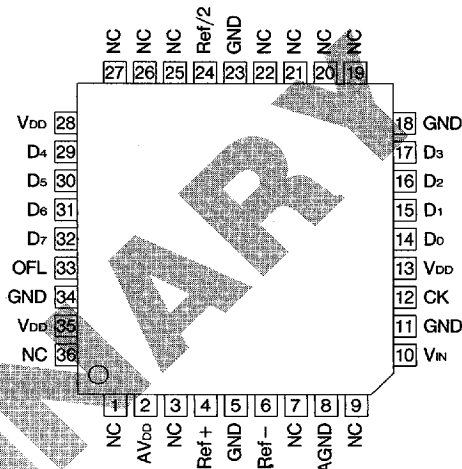
FEATURES

- 8-bit flash A/D converter
- 16 Msp/s sampling rate
- 75 mW low power ($V_{DD}=3.0\text{ V}$, Sampling=1 MHz)
- +3.3 V DC operation
- Unnecessary external S/H circuit
- Package :
 LH50506 : 36-pin QFP(QFP036-P-1010)
 LH50506N : 24-pin SOP(SOP024-P-0450B)

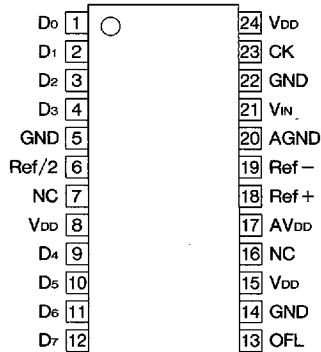
PIN CONNECTIONS

36-PIN QFP

TOP VIEW



24-PIN SOP



8180798 0014161 17T

The diagram illustrates a 24-bit DAC architecture. The input V_{IN} is connected to a resistor ladder. The nodes of the ladder are labeled $Ref+$, 256, 129, 128, 2, 1, and $Ref-$. The ladder is followed by a series of DFFs and encoders. The output is a 24-bit digital word with bits labeled OFL , D_7 (MSB), D_6 , D_5 , D_4 , D_3 , D_2 , D_1 , and D_0 (LSB). A Generator block provides a clock signal CK to the DFFs.

DFF : D-Flip Flop

A/D • D/A CONVERTERS

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PIN DESCRIPTION

● LH50506

PIN NO.	NAME	FUNCTION	I/O	PIN NO.	NAME	FUNCTION	I/O
1	NC	No Connection	—	19	NC	No Connection	—
2	AVDD	Analog Power Supply	—	20	NC	No Connection	—
3	NC	No Connection	—	21	NC	No Connection	—
4	Ref +	Reference Voltage (Top)	—	22	NC	No Connection	—
5	GND	Digital Ground	—	23	GND	Digital Ground	—
6	Ref -	Reference Voltage (Bottom)	—	24	Ref/2	Reference Voltage (Middle)	—
7	NC	No Connection	—	25	NC	No Connection	—
8	AGND	Analog Ground	—	26	NC	No Connection	—
9	NC	No Connection	—	27	NC	No Connection	—
10	VIN	Analog Input	I	28	VDD	Digital Power Supply	—
11	GND	Digital Ground	—	29	D4	Digital Output	O
12	CK	Clock Input	I	30	D5	Digital Output	O
13	VDD	Digital Power Supply	—	31	D6	Digital Output	O
14	D0	Digital Output (LSB)	O	32	D7	Digital Output (MSB)	O
15	D1	Digital Output	O	33	OFL	Over Flow Output	O
16	D2	Digital Output	O	34	GND	Digital Ground	—
17	D3	Digital Output	O	35	VDD	Digital Power Supply	—
18	GND	Digital Ground	—	36	NC	No Connection	—

● LH50506N

PIN NO.	NAME	FUNCTION	I/O	PIN NO.	NAME	FUNCTION	I/O
1	D0	Digital Output (LSB)	O	13	OFL	Over Flow Output	O
2	D1	Digital Output	O	14	GND	Digital Ground	—
3	D2	Digital Output	O	15	VDD	Digital Power Supply	—
4	D3	Digital Output	O	16	NC	No Connection	—
5	GND	Digital Ground	—	17	AVDD	Analog Power Supply	—
6	Ref/2	Reference Voltage (Middle)	—	18	Ref +	Reference Voltage (Top)	—
7	NC	No Connection	—	19	Ref -	Reference Voltage (Bottom)	—
8	VDD	Digital Power Supply	—	20	AGND	Analog Ground	—
9	D4	Digital Output	O	21	VIN	Analog Input	I
10	D5	Digital Output	O	22	GND	Digital Ground	—
11	D6	Digital Output	O	23	CK	Clock Input	I
12	D7	Digital Output (MSB)	O	24	VDD	Digital Power Supply	—

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{DD}	-0.3 to +7.0	V
Input voltage	V _{IN}	GND to V _{DD}	V
Reference voltage	Ref +, Ref -	GND to V _{DD}	V
Output voltage	V _{OUT}	-0.3 to V _{DD} + 0.3	V
Storage temperature	T _{stg}	-50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{DD}	2.7	3.3	3.6	V
Reference voltage (Top)	Ref +	2.0		V _{DD}	V
Reference voltage (Bottom)	Ref -	GND			V
Reference range	W _{Ref}	1.0			V
Analog input voltage	V _{IN}	Ref -		Ref +	V
Operating temperature	T _{opr}	-20		70	°C

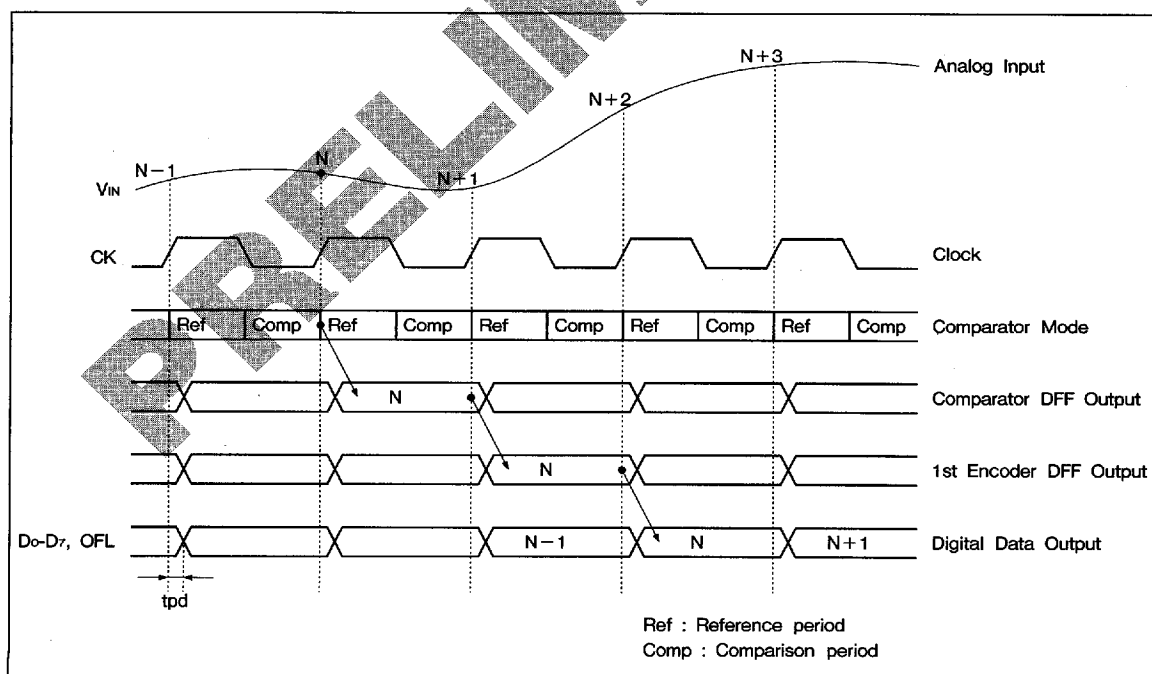
ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0 V, CK = 16 MHz, Ref + = 2.0 V, Ref - = 1.0 V, T_{opr} = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Resolution			8		bit
Supply current	I _{DD}		100		mA
Reference resistance	R _{ref}		256		Ω
Linearity error	INE				LSB
Differential linearity error	DNE			±1	LSB
Maximum conversion rate		16.0			Msp/s

FUNCTIONAL OPERATION

- Each of internal 256 chopper type comparators has two input terminals. One is given a reference voltage, that is divided into 256 equal voltages between Ref+ and Ref- by reference resistors. The other is given an analog input (V_{IN}).
 - While clock input CK is "High", every comparator samples the reference voltage.
 - While clock input CK is "Low", every comparator compares V_{IN} with the sampled reference voltage previously.
 - When the clock has been "High", DFF of every comparator stores the latest comparison result and outputs the thermometer code such as "11 ... 1100 ... 00" from Ref- side in order.
 - The transition point of the thermometer code is detected, based on the outputs of two adjoining comparators. And then the code is converted into the 8-bit binary code by the 1st encoder.
 - The 1st encoder encodes the thermometer code for the upper 128 comparators and the lower 128 comparators separately. DFF of the 1st encoder stores the converted data on the rising edge of the next clock.
 - The 2nd encoder converts the data received from the two 1st encoders into 8-bit digital data.
 - On the rising edge of the next clock, the data is stored in the output DFF and is output through the output buffer. The output data is output at 2-clock after the rising edge of sampling clock.
- * A single-phase input with 50% duty ratio is enough for the clock. However, it should be designed so that "High" period is 8 ns or more at least.



SYSTEM CONFIGURATION EXAMPLE

