LH5080 Z80 CMOS CPU Central Processing Unit

Description

The LH5080 is a Z80 CPU fabricated with CMOS silicon-gate process technology and is compatible with the conventional Z80 NMOS CPU (LH0080)

Due to the CMOS static structure, it provides low power consumption and large operating margin.

The power save mode can be obtained with a software control on the models suffixed with "L".

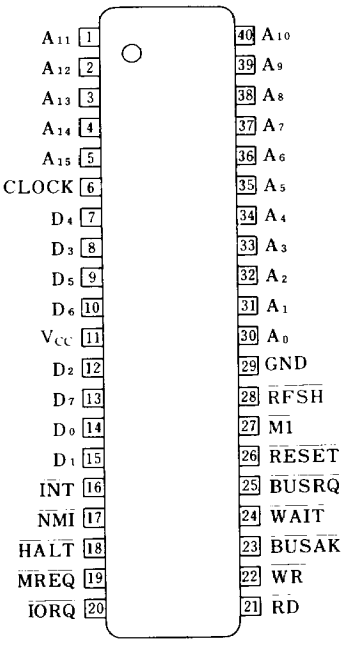
Features

1. Z80 CMOS CPU
2. Compatible with the Z80 NMOS CPU (LH0080)
3. 158 instructions
4. 22 registers
5. 3 modes of maskable interrupt and a nonmaskable interrupt
6. Instruction fetch cycle 1.6 μs/1.0 μs
7. Single +5V power supply and single phase clock
8. All inputs and outputs except clock input fully TTL compatible
9. Fully static operation DC to 2.5MHz/DC to 4MHz
10. Low power consumption
11. Power save mode (L suffix)
12. 40-pin DIP (DIP40-P-600)
    44-pin QFP (QFP44-P-1010A)

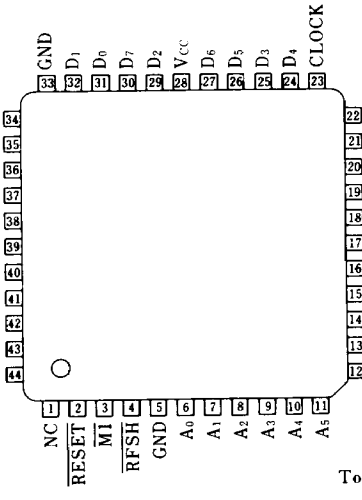
Note: The Z80 CMOS CPU (LH5080) is compatible with the Z80 NMOS CPU (LH0080). So there is no description here about the pins, CPU registers, architecture, interrupts, basic timings, and instruction sets. Refer back to the Z80 NMOS CPU described earlier.

Pin Connections

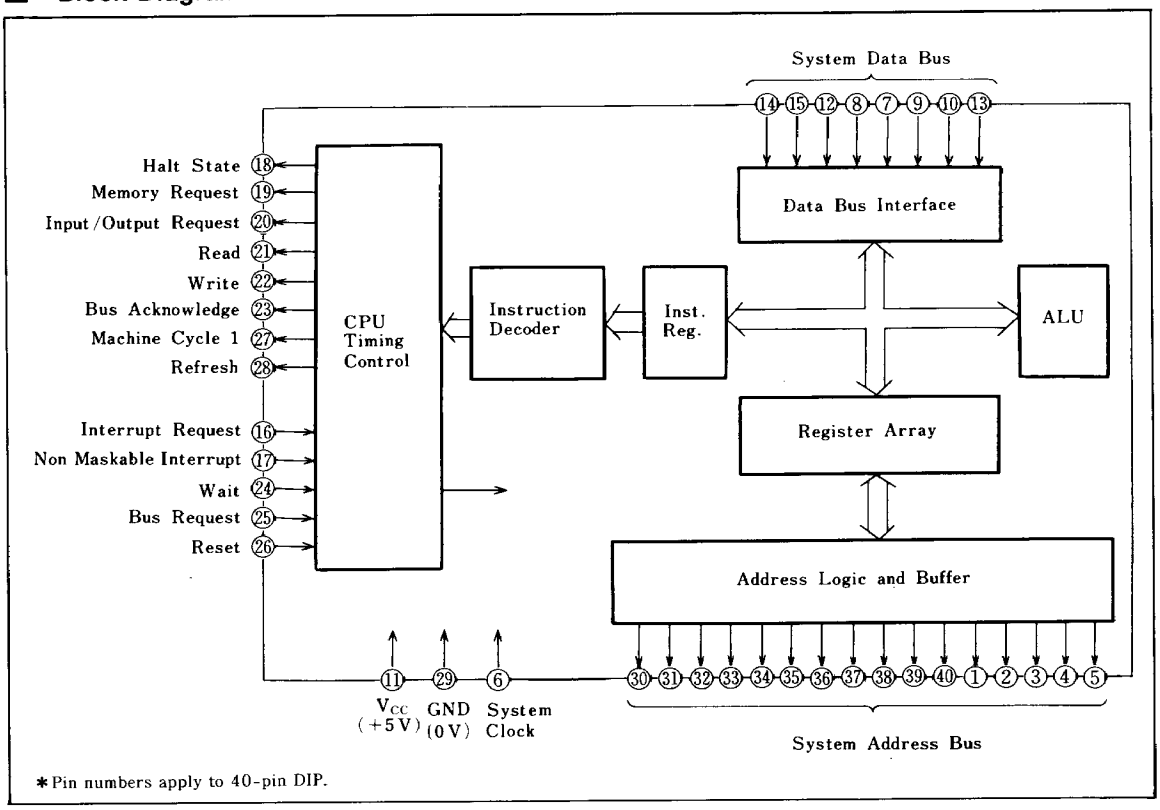
LH5080/LH5080L/LH5080A/LH5080AL



LH5080M/LH5080LM/LH5080AM/LH5080ALM



Block Diagram



*Pin numbers apply to 40-pin DIP.

Ordering Information

LH5080 X X X

- Package
  - Blank: 40-pin DIP (DIP40-P-600)
  - M: 44-pin QFP (QFP44-P-1010A)
- Power save mode
  - Blank: No power save
  - L: Power save
- Clock frequency
  - Blank: 2.5MHz
  - A: 4MHz
- Model No.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−65 to +150	℃

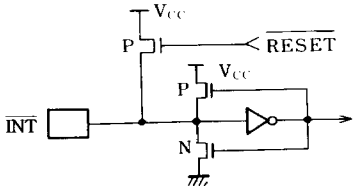
■ DC Characterisitics

(V_{CC}=5V±10%, Ta=0 to+70℃)

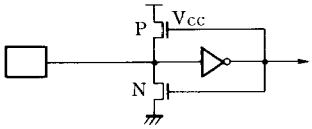
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Clock input low voltage	V_{ILC}			−0.3		0.45	V	
Clock input high voltage	V_{IHC}			V_{CC}−0.6		V_{CC}+0.3	V	
Input low voltage	V_{IL}			−0.3		0.8	V	
Input high voltage	V_{IH}			2.4		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=1.8mA				0.4	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA		2.4			V	
		I_{OH}=−50 μA		V_{CC}−0.4				
Current consumption	I_{CC}	V_{IL}=0.4V, V_{IH}=V_{CC}−0.4V Outputs open	LH5080/L		10	15	mA	1
			LH5080A/AL		15	20		2
Input leakage current	$\|I_{LI}\|$	V_{IN}=0V, V_{CC}				10	μA	3
3-state output leakage current	$\|I_{LOH}\|$	V_{OUT}=V_{CC}				10	μA	4
3-state output leakage current	$\|I_{LOL}\|$	V_{OUT}=0V				10	μA	4
Data bus leakage current	$\|I_{LD}\|$	0≦V_{IN}≦V_{CC}				10	μA	
Current consumption in PS mode (LH5080L/LH5080LM)	I_{CCPS}	V_{IH}=0V, V_{CC} Outputs open	LH5080L		50	150	μA	1
			LH5080AL		80	200		2

Note 1: TcC=400ns
Note 2: TcC=250ns

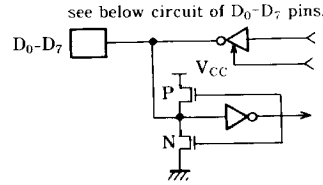
Note 3−(1): For $|I_{LI}|$ Specification, see below circuits of $\overline{INT}$ pin.



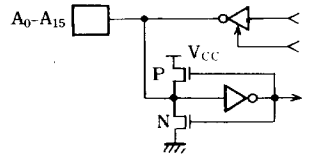
Note 3−(2): For $|I_{LI}|$ Specification, see below circuits of $\overline{WAIT}$, $\overline{NMI}$ and $\overline{BUSRQ}$.



Note 3 and 4: For $|I_{LI}|$, $|I_{LOH}|$ and $|I_{LOL}|$ Specifications, see below circuit of D_0-D_7 pins.



Note 4: For $|I_{LOH}|$ and $|I_{LOL}|$ Specifications, see below circuit of A_0-A_{15} pins.



■ Capacititance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground	5	pF
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{OUT}		10	pF

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0 to+70°C)

No.	Parameter	Symbol	LH5080		LH5080A		Unit
			MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	TcC	400*		250*		ns
2	Clock pluse high width	TwCh	180*		110*		ns
3	Clock pluse low width	TwCl	180		110		ns
4	Clock fall time	TfC		30		30	ns
5	Clock rise time	TrC		30		30	ns
6	Clock ↑ to address valid delay	TdCr (A)		145		110	ns
7	Address valid to $\overline{MREQ}$ ↓ delay	TdA (MREQf)	125*		65*		ns
8	Clock ↓ to $\overline{MREQ}$ ↓ delay	TdCf (MREQf)		100		85	ns
9	Clock ↑ to $\overline{MREQ}$ ↑ delay	TdCr (MREQr)		100		85	ns
10	$\overline{MREQ}$ pulse high width	TwMREQh	170*		110*		ns
11	$\overline{MREQ}$ pulse low width	TwMREQl	360*		220*		ns
12	Clock ↓ to $\overline{MREQ}$ ↑ delay	TdCf (MREQr)		100		85	ns
13	Clock ↓ to $\overline{RD}$ ↓ delay	TdCf (RDf)		130		95	ns
14	Clock ↑ to $\overline{RD}$ ↑ delay	TdCr (RDr)		100		85	ns
15	Data setup time to clock ↑	TsD (Cr)	50		35		ns
16	Data hold time after $\overline{RD}$ ↑	ThD (RDr)	15		15		ns
17	$\overline{WAIT}$ setup time to clock ↓	TsWAIT (Cf)	70		70		ns
18	$\overline{WAIT}$ hold time after clock ↓	ThWAIT (Cf)	15		15		ns
19	Clock ↑ to $\overline{M1}$ ↓ delay	TdCr (M1f)		130		100	ns
20	Clock ↑ to $\overline{M1}$ ↑ delay	TdCr (M1r)		130		100	np
21	Clock ↑ to $\overline{RFSH}$ ↓ delay	TdCr (RFSHf)		180		130	ns
22	Clock ↑ to $\overline{RFSH}$ ↑ delay	TdCr (RFSHr)		150		120	ns
23	Clock ↓ to $\overline{RD}$ ↑ delay	TdCf (RDr)		110		85	ns
24	Clock ↑ to $\overline{RD}$ ↓ delay	TdCr (RDf)		100		85	ns
25	Data setup to clock ↑ during M_2, M_3, M_4 or M_5 cycles	TsD (Cf)	60		50		ns
26	Address stable prior to $\overline{IORQ}$ ↓	TdA (IORQf)	320*		180*		ns
27	Clock ↑ to $\overline{IORQ}$ ↓ delay	TdCr (IORQf)		90		75	ns
28	Clock ↓ to $\overline{IORQ}$ ↑ delay	TdCf (IORQr)		110		85	ns
29	Data stable prior to $\overline{WR}$ ↓ (memory cycle)	TdDm (WRf)	190*		80*		ns
30	Clock ↓ to $\overline{WR}$ ↓ delay	TdCf (WRf)		90		80	ns
31	$\overline{WR}$ pulse width	TwWR	360*		220*		ns
32	Clock ↓ to $\overline{WR}$ ↑ delay	TdCf (WRr)		100		80	ns
33	Data stable prior to $\overline{WR}$ ↓ (I/O cycle)	TdDi (WRf)	20*		−10*		ns
34	Clock ↑ to $\overline{WR}$ ↓ delay	TdCr (WRf)		80		65	ns
35	Data stable from $\overline{WR}$ ↑	TdWRr (D)	120*		60*		ns
36	Clock ↓ to $\overline{HALT}$ ↑	TdCf (HALT)		300		300	ns
37	$\overline{NMI}$ pulse width	TwNMI	80		80		ns
38	$\overline{BUSREQ}$ setup time to clock ↑	TsBUSRQ (Cr)	80		50		ns
39	$\overline{BUSREQ}$ hold time after clock ↑	ThBUSRQ (Cr)	15		15		ns
40	Clock ↑ to $\overline{BUSACK}$ ↓ delay	TdCr (BUSAKf)		120		100	ns
41	Clock ↓ to $\overline{BUSACK}$ ↑ delay	TdCf (BUSAKr)		110		100	ns
42	Clock ↑ data float delay	TdCr (Dz)		90		90	ns
43	Clock ↑ to control output float delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)	TdCr (CTz)		110		80	ns

↑ Rising edge, ↓ Falling edge.

No.	Parameter	Symbol	LH5080		LH5080A		Unit
			MIN.	MAX.	MIN.	MAX.	
44	Clock ↑ to address float delay	TdCr (Az)		110		90	ns
45	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to address hold time	TdCTr (A)	160*		80*		ns
46	$\overline{RESET}$ to clock ↑ setup time	TsRESET (Cr)	90		60		ns
47	Clock ↑ to $\overline{RESET}$ hold time	ThRESET (Cr)	15		15		ns
48	$\overline{INT}$ to clock ↑ setup time	TsINTf (Cr)	80		80		ns
49	Clock ↑ to $\overline{INT}$ hold time	ThINTr (Cr)	15		15		ns
50	$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ delay	TdM1f (IORQf)	920*		565*		ns
51	Clock ↓ to $\overline{IORQ}$ ↓ delay	TdCf (IORQf)		110		85	ns
52	Clock ↑ to $\overline{IORQ}$ ↑ delay	TdCf (IORQr)		100		85	ns
53	Clock ↓ to data valid delay	TdCf (D)		230		150	ns

↑ Rising edge, ↓ Falling edge
* For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table below

Footnotes to AC Characteristics

No.	Symbol	Formula
1	TcC	TwCh+TwCl+TrC+TfC
2	TwCh	MAX. 200 μs
7	TdA (MREQf)	TwCh+TfC−75
10	TwMREQh	TwCh+TfC−30
11	TwMREQl	TcC−40
26	TdA (IORQf)	TcC−80
29	TdD (WRf)	TcC−210
31	TwWR	TcC−40
33	TdD (WRf)	TwCl+TrC−180
35	TdWRr (D)	TwCl+TrC−80
45	TdCTr (A)	TwCl+TrC−40
50	TdM1f (IORQf)	2TcC+TwCh+TfC−80

AC Test Conditions

- Input voltage amplitude : 0.4V to 2.8V
- Clock input voltage amplitude : 0.4V to V_{CC}−0.6V
- Input signal rise and fall time : 10 ns
- Input judge level : 0.8V and 2.0V
- Output judge level : 0.8V and 2.0V
- Output load : ITTL+100 pF

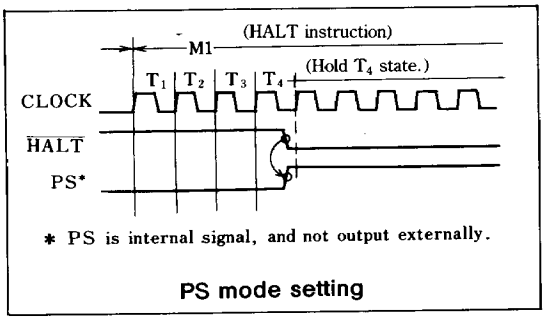
■ Power Save Function

The LH5080L series features the power save (PS) function. After a HALT instruction has been executed, the internal clock signal is automatically cut off to bring the CPU into the halt mode.

(1) PS mode setting

With a HALT instruction executed, the PS mode will be automatically established. In this mode, the internal clock signal is cut off to save the power consumed for the clock signal operation. Cutting an external clock signal does not give any problem inside, therefore, in this mode. To cut off the external clock, it is possible to utilize the rise timing of a $\overline{\text{HALT}}$ signal output. It should be noted, however, that this timing cannot be used to restart the external clock.

In the PS mode, the bus request ($\overline{\text{BUSRQ}}$) is not accepted and the memory refresh is not done, either.



* PS is internal signal, and not output externally.

PS mode setting

(2) PS mode clear

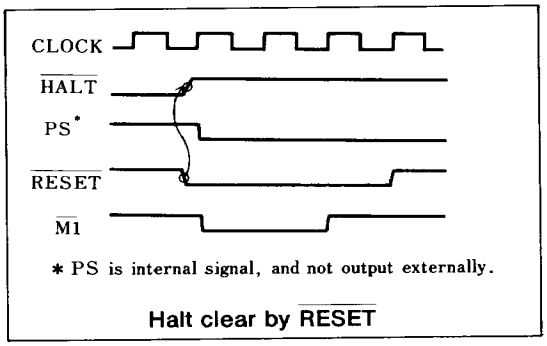
The PS mode is cleared by any of the following; reset (RESET), non-maskable interrupt ($\overline{\text{NMI}}$) and maskable interrupt ($\overline{\text{INT}}$).

When the external clock is shut down in the PS mode, a stable clock signal must be input before clearing the PS mode.

(i) Clearing with RESET: Input the $\overline{\text{RESET}}$ signal for more than 3 clock cycles. The PS mode is then cleared and the reset just as before is carried out.

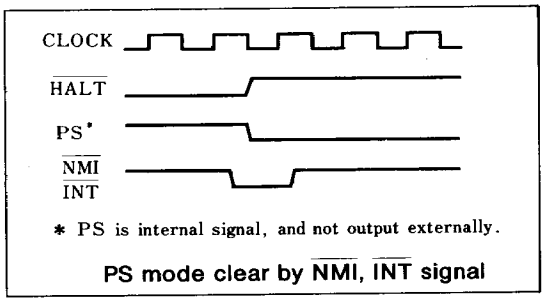
(ii) Clearing with $\overline{\text{NMI}}$: Input the $\overline{\text{NMI}}$ signal (edge trigger) to clear the PS mode and to carry out the instruction next to the HALT. Now the non-maskable interrupt processing routine will be introduced.

(iii) Clearing with $\overline{\text{INT}}$: Input the $\overline{\text{INT}}$ signal (level trigger) regardless of which state the interrupt enable flag is in. The PS mode is now cleared and the HALT instruction executed. If the interrupt enable flag is set up and the $\overline{\text{INT}}$ signal is "Low" at the clock pulse rise timing in the last clock cycle of the HALT instruction, the maskable interrupt processing routine will be introduced as the next machine cycle.



* PS is internal signal, and not output externally.

Halt clear by $\overline{\text{RESET}}$



* PS is internal signal, and not output externally.

PS mode clear by $\overline{\text{NMI}}$, $\overline{\text{INT}}$ signal

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