LH5081 Z80 CMOS PIO Parallel I/O Controller

Description

The LH5081 is a Z80 PIO fabricated with CMOS silicon gate process technology and is compatible with the conventional Z80 NMOS PIO (LH0081)

Due to the CMOS static structure, it provides low power consumption and large operating margin.

The power save mode can be obtained with a software control on the models suffixed with "L".

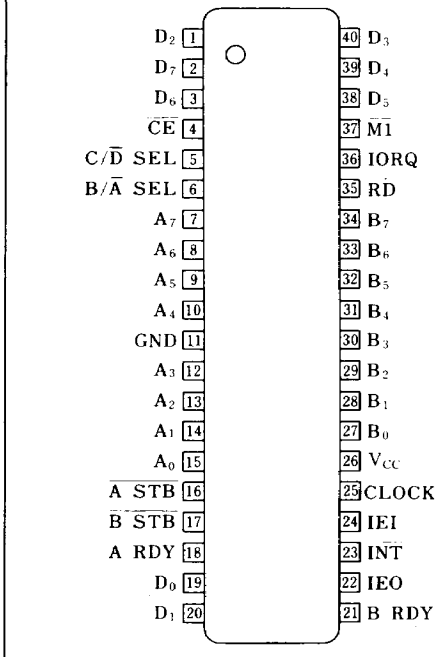
Features

1. Z80 CMOS PIO
2. Compatible with NMOS Z80 PIO (LH0081)
3. Tow independent 8-bit bidirectional peripheral interface ports with handshake data transfer control
4. 4 programmable operating modes
   - Byte input mode
   - Byte output mode
   - Byte bidirectional bus mode (Port A only)
   - Byte control mode
5. Programmable interrupt on peripheral status conditions
6. Vectored daisy chain priority interrupt
7. Darlington transistor drive capability (Port B output)
8. All inputs and outputs except clock input fully TTL compatible
9. Single +5V power supply and single phase clock
10. Fully static operation (DC to 2.5MHz/4MHz/6MHz)
11. Low power consumption
12. Power save mode (L suffix)
13. Status read mode (L suffix)
14. 40-pin DIP (DIP40-P-600)
    44-pin QFP (QFP44-P-1010A)

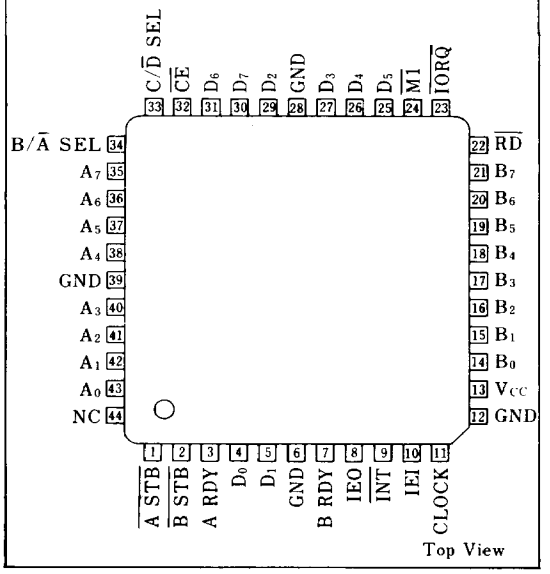
Note: The Z80 CMOS CPU (LH5081) is compatible with the Z80 NMOS PIO (LH0081). So there is no description here about the pins, programming, and basic timings waveforms. Refer back to the Z80 NMOS PIO described earlier.

Pin Connections

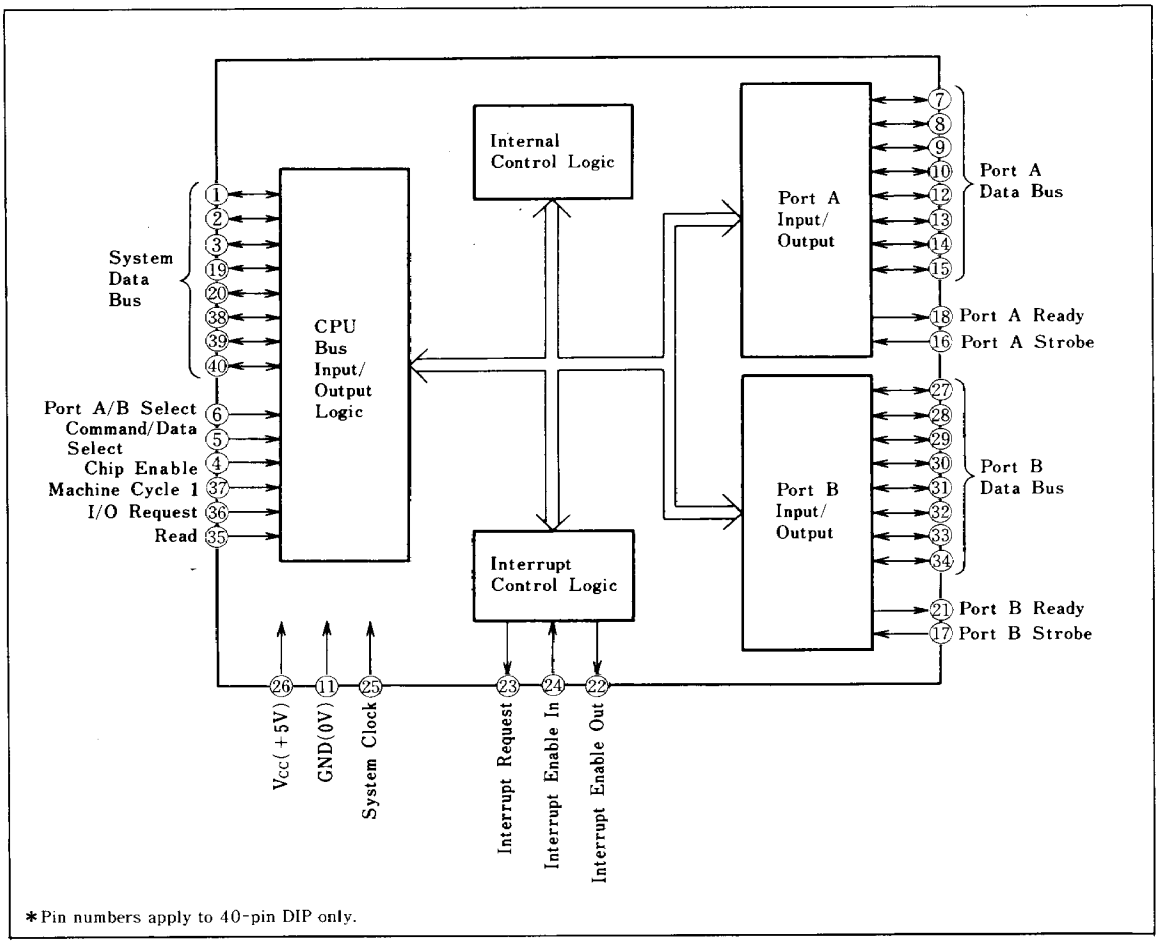
LH5081/LH5081A/LH5081B
LH5081L/LH5081AL/LH5081BL



LH5081M/LH5081AM
LH5081LM/LH5081ALM



Block Diagram



*Pin numbers apply to 40-pin DIP only.

Ordering Information

LH5081 X X X

- Package *
  - Blank: 40-pin DIP (DIP40-P-600)
  - M: 44-pin QFP (QFP44-P-1010A)
- Power save mode
  - Blank: No power save
  - L: Power save
- Clock frequency
  - Blank: 2.5MHz
  - A: 4MHz
  - B: 6MHz
- Model No.

* The 6MHz type is packaged in 40-pin DIP only.

■ Absolute Maximum Ratings

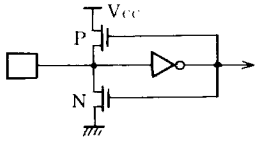
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3 to 7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−65 to +150	℃

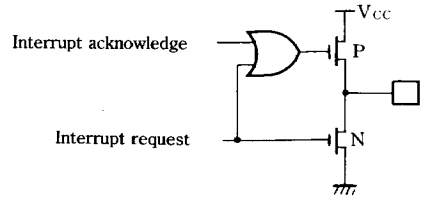
■ DC Characteristics

(V_{CC}=5V±10%, Ta=0 to +70℃)

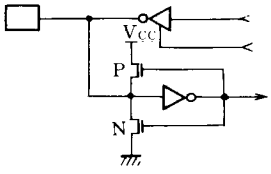
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Clock input low voltage	V_{ILC}			−0.3		0.45	V	
Clock input high voltage	V_{IHC}			V_{CC}−0.6		V_{CC}+0.3	V	
Input low voltage	V_{IL}			−0.3		0.8	V	
Input high voltage	V_{IH}			2.2		V_{CC}+0.3	V	
Output low voltage	V_{OL}	I_{OL}=2mA				0.4	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA		2.4			V	
		I_{OH}=−50 μA		V_{CC}−0.4V			V	
Current consumption	I_{CC}	V_{IL}=0.4, V_{IH}=V_{CC}−0.4V, output open	LH5081/L		1	3	mA	1
			LH5081A/AL		4	6	mA	2
			LH5081B		6	8	mA	3
Input leakage current	$\|I_{LI}\|$	V_{IN}=0V, V_{CC}				10	μA	4
3-state output leakage current	$\|I_{LOH}\|$	V_{OUT}=V_{CC}				10	μA	5
3-state output leakage current	$\|I_{LOL}\|$	V_{OUT}=0V				10	μA	5
Data bus leakage current input	$\|I_{LD}\|$	0≦V_{IN}≦V_{CC}				10	μA	
Darlington drive current	I_{OHD}	V_{OH}=1.5V, Port B only		−1.5			mA	
Current consumption in PS mode	I_{CCPS}	V_{IN}=0V, V_{CC} Outputs open	LH5081L		1	100	μA	1
			LH5081AL		1	100		2

Note 1: TcC=400ns, V_{IL}=0.4V, V_{IH}=V_{CC}−0.4V, outputs open.
Note 2: TcC=250ns
Note 3: TcC=167ns
Note 4: (1) For $|I_{LI}|$ specification, see below circuit of $\overline{A\ STB}$ and $\overline{B\ STB}$. 2978 (2) The $\overline{INT}$ pin is arraged as shown below.





Note 5: For $|I_{LOH}|$ and $|I_{LOL}|$ specifications, see below circuit of A_0-A_7 and B_0-B_7



■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground	7	pF
Input capacitance	C_{IN}		7	pF
Output capacitance	C_{OUT}		10	pF

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0 to +70℃)

No.	Parameter	Symbol	LH5081		LH5081A		LH5081B		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	Clock cycle time	TcC	400	(Note 1)	250	(Note 1)	165	(Note 1)	ns	
2	Clock high width	TwCh	170		105		65		ns	
3	Clock low width	TwCl	170		105		65		ns	
4	Clock fall time	TfC		30		30		20	ns	
5	Clock rise time	TrC		30		30		20	ns	
6	$\overline{CE}$, B/$\overline{A}$, C/$\overline{D}$ to $\overline{RD}$, $\overline{IORQ}$↓ setup time	TsCS (RI)	50		50		50		ns	6
7	Any hold times for specified setup time	Th	15		15		15		ns	
8	$\overline{RD}$, $\overline{IORQ}$ to clock ↑ setup time	TsRI (C)	115		115		70		ns	
9	$\overline{RD}$, $\overline{IORQ}$↓ to data output delay	TdRI (DO)		430		380		300	ns	2
10	$\overline{RD}$, $\overline{IORQ}$↑ to data output float delay	TdRI (DOs)		160		110		70	ns	
11	Data in to clock ↑ setup time	TsDI (C)	50		50		40		ns	C_L=50pF
12	$\overline{IORQ}$↓ to data out delay (INTACK cycle)	TdIO (DOI)		340		160		120	ns	3
13	$\overline{M1}$↓ to clock ↑ setup time	TsM1 (Cr)	210		90		70		ns	
14	$\overline{M1}$↑ to clock ↓ setup time ($\overline{M1}$ cycle)	TsM1 (Cf)	0		0		0		ns	8
15	$\overline{M1}$↓ to IEO ↓ delay (interrupt immediately precceding $\overline{M1}$↓)	TdMI (IEO)		300		190		100	ns	5, 7
16	IEI to $\overline{IORQ}$↓ setup time (INTACK cycle)	TsIEI (IO)	140		140		100		ns	7
17	IEI↓ to IEO↓ delay	TdIEI (IEOf)		190		130		120	ns	5 C_L=50pF
18	IEI↑ to IEO↑ delay (after ED decode)	TdIEI (IEOr)		210		160		160	ns	5
19	$\overline{IORQ}$↑ to clock ↓ setup time (to activate READY on next clock cycle)	TcIO (C)	220		200		170		ns	
20	Clock ↓ to READY ↑ delay	TdC (RDYr)		200		190		170	ns	5 C_L=50pF
21	Clock ↓ to READY ↓ delay TdC (RDYf)	TdC (RDYr)		150		140		120	ns	5
22	$\overline{STROBE}$ pulse width	TwSTB	150		150		120		ns	4
23	$\overline{STROBE}$↑ to clock ↓ setup time (to activate READY on next clock cycle)	TsSTB (C)	220		220		150		ns	5
24	$\overline{IORQ}$↑ to PORT DATA stable delay (mode 0)	TdIO (PD)		200		180		160	ns	5
25	PORT DATA to $\overline{STROBE}$↑ setup time (mode 1)	TsPD (STB)	260		230		190		ns	
26	$\overline{STROBE}$↓ to PORT DATA stable (mode 2)	TdSTB (PD)		230		210		180	ns	5
27	$\overline{STROBE}$↑ to PORT DATA float delay (mode 2)	TdSTB (PDr)		200		180		160	ns	C_L=50pF
28	PORT DATA match to $\overline{INT}$↓ delay (mode 3)	TdPD (INT)		540		490		430	ns	
29	$\overline{STROBE}$↑ to $\overline{INT}$↓ delay	TdSTB (INT)		490		440		350	ns	

↑ Rising edge, ↓ Falling edge

Note 1 : TcC=TwCh+TwCl+TrC+TIC.

Note 2 : Increase TdRI (DO) by 10 ns for each 50 pF increase in load up to 200 pF max.

Note 3 : Increase TdIO (DOI) by 10 ns for each 50 pF, increase in loading up to 200 pF max.

Note 4 : For Mode 2 : TwSTB>TsPD (STB).

Note 5 : Increase these values by 2 ns for each 10 pF increase in loading up to 100 pF max.

Note 6 : TsCS (RI) may be reduced. However, the time substracted from TsCS (RI) will be added to TdRI (DO).

Note 7 : 2.5 TcC > (N-2) TdIEI (IEOf)+TdM1 (IEO)+TsIEI (IO)+TTL Buffer Delay, if any.

Note 8 : $\overline{M1}$ must be active for a minimum of two clock cycles to reset the PIO.

AC Test Conditions :

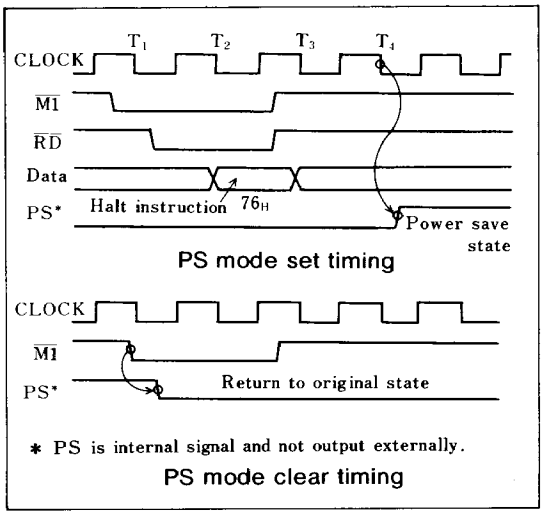
- Input voltage amplitude : 0.4V to 2.8V
- Clock input voltage amplitude : 0.4V to $V_{CC}-0.6V$
- Input signal rise and fall time : 10ns
- Input judge level : 0.8V and 2.0V
- Output judge level : 0.8V and 2.0V
- Output load : ITTL+100pF (unless otherwise specified)

■ Power Save and Status Information Read Function

Unlike the LH0081/LH5081, the LH5081L series has the power save (PS) and status information read functions.

(1) Power save function

(i) PS mode setting When the CPU (LH5080L series) has executed an HALT instruction in the PS mode, the LH5081L series reads this HALT instruction to automatically go into the PS mode. Now the internal clock signal is cut off. Therefore, cutting an external clock input gives no problem inside in this mode.



(ii) PS mode clear The PS mode is cleared by detecting the fall of the $\overline{M1}$ signal. When the external clock is off in the PS mode, however, a stable clock signal must be input before clearing the PS mode.

When the CPU (LH5080L series) is cleared from the PS mode and comes into the next fetch cycle, therefore, the LH5081L series is also cleared from its PS mode at the fall of the first $\overline{M1}$ signal in this cycle.

The PS mode clearing can be done by issuing an interrupt request.

Set up the interrupt generate conditions in Mode 3 of the LH5081L series. By this, an interrupt request (INT) is issued even in the PS mode, the CPU (LH5080L series) is cleared from the PS mode, and thus LH5081L series is also cleared.

(2) Status information read

Under the following conditions, the mode setup bits and handshake signals of Port A and Port B are read from the data bus during the read cycle. See the chart below.

Conditions: CE = "Low", $\overline{RD}$ = "Low", $\overline{IORQ}$ = "Low", C/D = "High", B/A = X (undefined)