LH5082 Z80 CMOS CTC Counter Timer Circuit

Description

The LH5082 is a Z80 CTC fabricated with CMOS silicon-gate process technology and is compatible with the conventional Z80 NMOS CTC (LH0082)

The LH5082 is designed with CMOS fully static circuits and so provides low power consumption and wide range power supply voltage operation.

The LH5082L/LH5082LM provides power save mode controlled by software.

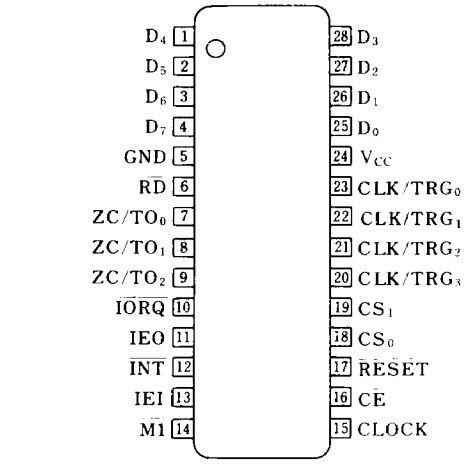
Features

1. Z80 CMOS CTC
2. Compatible with the Z80 NMOS CTC (LH0082)
3. 4 independent programmable 8-bit counter/16-bit timer channels
4. Selectable counter/timer mode for each channel
5. Programmable interrupt triggered by counter/timer
6. Downcounters reloaded automatically at zero count
7. Readable downcounters
8. Selectable 16 or 256 prescaler (timer mode)
9. Selectable positive or negative triggers for timer and selectable positive or negative clock edge for counter
10. ZC/TO outputs of three channels capable of driving Darlington transistors
11. Vectored and daisy chain piority interrupt
12. Single +5V power supply and single phase clock
13. All inputs and outputs except clock input fully TTL compatible
14. Fully static operation (DC to 2.5MHz/4MHz/6MHz)
15. Low power consumption
16. Power save mode (L suffix)
17. 28-pin DIP (DIP28-P-600)
    44-pin QFP (QFP44-P-1010A)

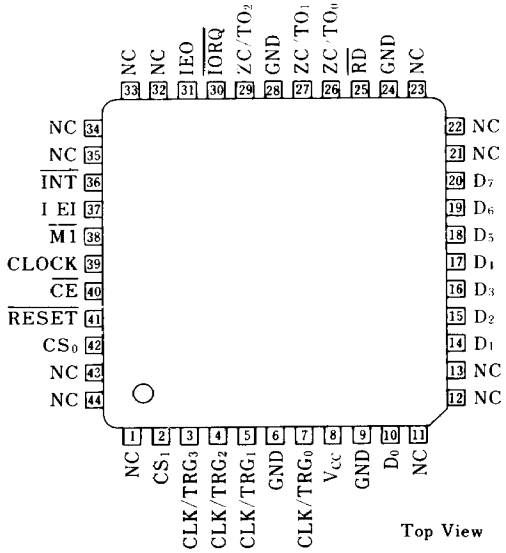
Note: The Z80 CMOS CTC (LH5082) is compatible with the Z80 NMOS CTC (LH0082). So there is no description here about the pins, programming, and basic timing waveform. Refer back to the Z80 NMOS CTC described earlier.

Pin Connections

LH5082/LH5082A/LH5082B
LH5082L/LH5082AL/LH5082BL



LH5082M/LH5082AM
LH5082LM/LH5082ALM



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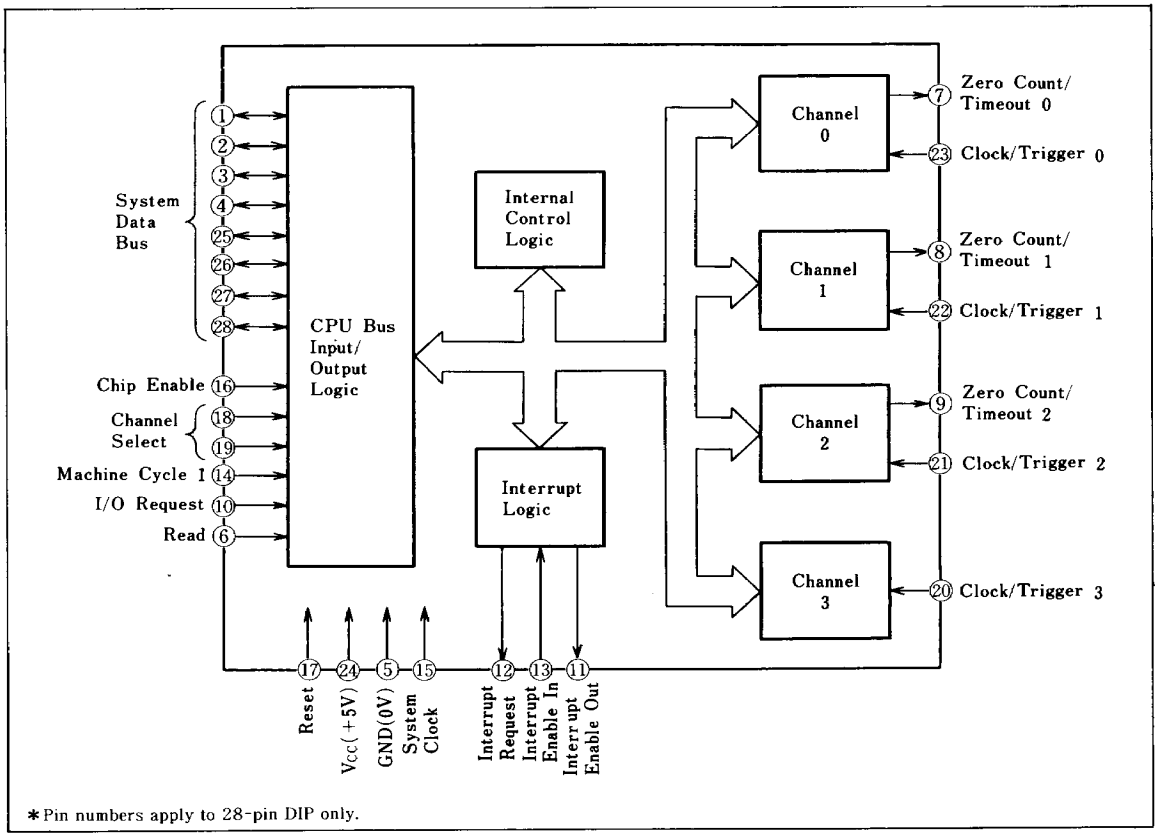
■ Block Diagram



*Pin numbers apply to 28-pin DIP only.

■ Ordering Information

LH5082 X X X

- Package *
  - Blank: 28-pin DIP (DIP28-P-600)
  - M: 44-pin QFP (QFP44-P-1010A)
- Power save mode
  - Blank: No power save
  - L: Power save
- Clock frequency
  - Blank: 2.5MHz
  - A: 4MHz
  - B: 6MHz
- Model No.

* The 6MHz type is packaged in 28-pin DIP only.

■ Absolute Maximum Ratings

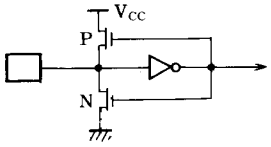
Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−65 to +150	℃

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0 to +70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Clock input low voltage	V_{ILC}			−0.3		0.45	V	
Clock input high voltage	V_{IHC}			V_{CC}−0.6		V_{CC}+0.3	V	
Input low voltage	V_{IL}			−0.3		0.8	V	
Input high voltage	V_{LH}			2.2		V_{CC}	V	
Output low voltage	V_{OL}	I_{OL}=2mA				0.4	V	
Output high voltage	V_{OH}	I_{OH}=−250 μA		2.4			V	
		I_{OH}=−50 μA		V_{CC}−0.4V			V	
Current consumption	$\lvert I_{CC} \rvert$	V_{IL}=0.4V, V_{IH}=V_{CC}−0.4V, outputs open	LH5082/L		2	4	mA	1
			LH5082A/AL		3	6	mA	2
			LH5082B/BL		5	8	mA	3
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V, V_{CC}				10	μA	4
3-state output leakage current	$\lvert I_{LOH} \rvert$	V_{OUT}=V_{CC}				10	μA	
3-state output leakage current	$\lvert I_{IOL} \rvert$	V_{OUT}=0V				10	μA	
Darlington drive current	I_{OHD}	V_{OH}=1.5V Applicated to ZC/TO_0-ZC/TO_2		−1.5			mA	
Current consumption in PS mode	I_{CCPS}	V_{IN}=0V, V_{CC} Outputs open	LH5082L		1	100	μA	1
			LH5082AL		1	100		2
			LH5082BL		1	100		3

Note 1: TcC=400ns
Note 2: TcC=250ns
Note 3: TcC=167ns
Note 4: For $\lvert I_{LI} \rvert$ specification, see below circuit of CLK/TRG_0-CLK/TG_3.



■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground	5	pF
Input capacitance	C_{IN}		5	pF
Output capacitance	C_{OUT}		10	pF

■ AC Characteristics

(V_{CC}=5V±10%, Ta=0 to +70℃)

No.	Parameter	Symbol	LH5082		LH5082A		LH5082B		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	Clock cycle time	TcC	400	(Note 1)	250	(Note 1)	165		ns	
2	Clock high width	TwCh	170		105		65		ns	
3	Clock low width	TwCl	170		105		65		ns	
4	Clock fall time	TfC		30		30		20	ns	
5	Clock rise time	TrC		30		30		20	ns	
6	All hold times	Th	15		15		15		ns	
7	$\overline{CS}$ to clock ↑ setup time	TcCS (C)	250		160		100		ns	
8	$\overline{CE}$ to clock ↑ setup time	TsCE (C)	200		150		100		ns	
9	$\overline{IORQ}$ ↓ to clock ↑ setup time	TsIO (C)	250		115		70		ns	
10	$\overline{RD}$ ↓ clock ↑ setup time	TsRD (C)	240		115		70		ns	
11	Clock ↑ to data out delay	TdC (DO)		240		200		130	ns	2
12	Clock ↓ to data out float dalay	TdC (DOz)		230		110		90	ns	
13	Data In to clock ↑ setup time	TsDI (C)	60		50		40		ns	
14	$\overline{M1}$ to clock ↑ setup time	TsM1 (C)	210		90		70		ns	
15	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt immediately preceding $\overline{M1}$)	TdM1 (IEO)		300		190		130	ns	3
16	$\overline{IORQ}$ ↓ to data out delay (INTA cycle)	TdIO (DOI)		340		160		110	ns	2
17	IEI ↓ to IEO ↓ delay	TdIEI (IEOf)		190		130		100	ns	3
18	IEI ↑ to IEO ↑ delay ↑ (after ED decode)	TdIEI (IEOr)		220		160		110	ns	3
19	Clock ↑ to $\overline{INT}$ ↓ delay	TdC (INT)		TcC+200		TcC+140		TcC+120	ns	4
20	CLK/TRG ↑ to $\overline{INT}$ ↓ delay (tsCTR (C) satisfied)	TdClk (INT)		TcC+230		TcC+160		TcC+130	ns	5
	CLK/TRG ↑ to $\overline{INT}$ ↓ delay (tsCTR (C) not satisfied)	TdCLK (INT)		2TcC+530		2TcC+370		2TcC+280	ns	5
21	CLK/TRG cycte time	TcCTR	2TcC		2TcC		2TcC		ns	5
22	CLK/TRG rise time	TrCTR		50		50		40	ns	
23	CLK/TRG fall time	TfCTR		50		50		40	ns	
24	CLK/TRG low width	TwCTR1	200		200		120		ns	
25	CLK/TRG high width	TwCTRh	200		200		120		ns	
26	CLK/TRG ↑ to clock ↑ setup time for immediate count	TsCTR (Cf)	300		210		150		ns	5
27	CLK/TRG ↑ to clock ↑ setup time for enabling of prescaler on following clock ↑	TsCTR (Ct)	210		210		150		ns	4
28	Clock ↑ to ZC/TO ↑ delay	TdC (ZC/TOr)		260		190		140	ns	
29	Clock ↑ to ZC/TO ↓ delay	TdC (ZC/TOf)		190		190		140	ns	
30	IEI setup time $\overline{IORQ}$ ↓ (INTA cycle)	TsIEI (IO)	140		140		140		ns	

↑ Rising edge, ↓ Falling edge

[A] 2.5 TcC>(n-2) TdIEI (IEOf)+TdMI (IEO) +TsIEI (IO)+TTL buffer delay, if any.

[B] $\overline{RESET}$ must be active for minimum of 3 clock cycles

Note 1 : TcC=TwCh+TwCl+TrC+TfC.

Note 2 : Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines, and 100 pF for control lines.

Note 3 : Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum.

Note 4 : Timer mode.

Note 5 : Counter mode.

* All timing are preliminary and subject to change.

AC Test Conditions

- Input voltage amplitude: 0.4 V to 2.8 V
- Clock input voltage amplitude: 0.4V to V_{CC}-0.6V
- Input signal rise and fall time: 10 ns
- Input judge level: 0.8 V and 2.0 V
- Output judge level: 0.8 V and 2.0 V
- Output load: ITTL + 100 pF (unless otherwise specified)

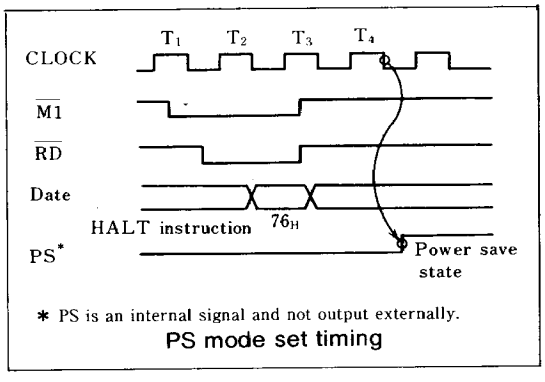
■ Power Save Function

The LH5082L series has the power save (PS) functions.

(1) PS mode setting

When the CPU (LH5080L series) has executed a HALT instruction, the LH5082L series reads this HALT instruction to autmatically go into the PS mode. In this mode, the internal clock signal is cut off. The external clock may be off during the PS mode.

About the external clock stop, the same is true as the power-saving CPU (LH5080L series)



* PS is an internal signal and not output externally.

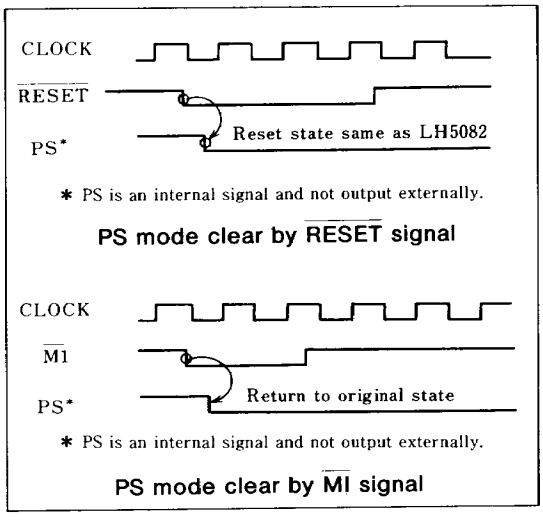
PS mode set timing

(2) PS mode clear

The PS mode is cleared by the fall of $\overline{M1}$ signal or the $\overline{RESET}$ signal.

When the external clock is off the PS mode, however, a stable clock signal must be input before clearing the PS mode.

Once cleared from the PS mode, the power-saving CPU (LH5080L series) comes into the next fetch cycle. At the time when the first M1 signal during this cycle falls, the LH5082L series is also cleared from the PS mode.



* PS is an internal signal and not output externally.

PS mode clear by $\overline{RESET}$ signal

* PS is an internal signal and not output externally.

PS mode clear by $\overline{M1}$ signal