LH5116-15/-20

CMOS 16384-Bit Static Random Access Memory

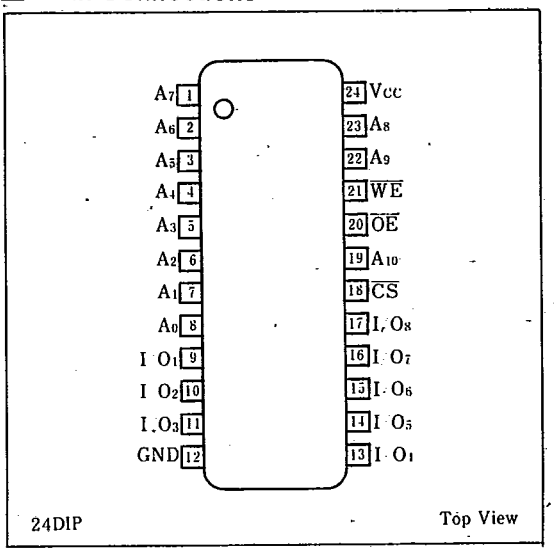
■ Description

The LH5116-15/-20 are fully static RAMs organized as 2,048×8-bit by using silicon-gate CMOS process technology.

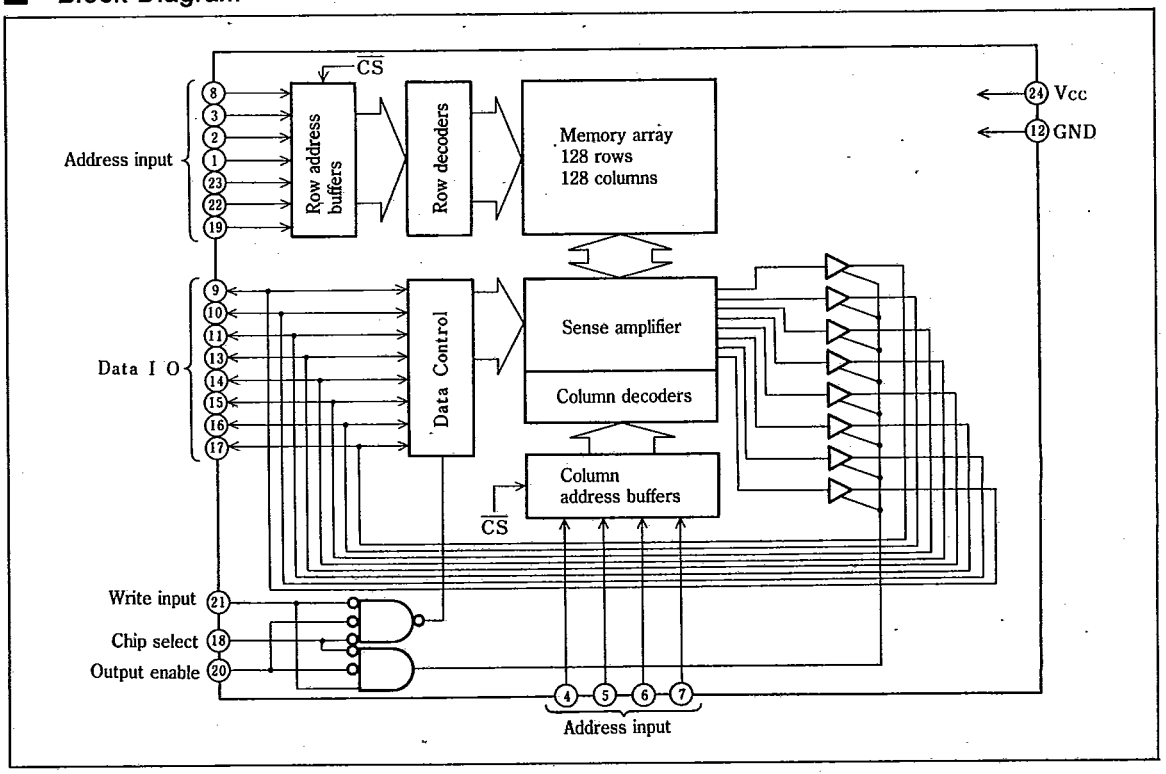
■ Features

1. 2,048×8-bit organization
2. Single +5V power supply
3. Fully static operation
4. All inputs and outputs TTL compatible
5. Three-state outputs
6. Access time (MAX.)
   LH5116-15 : 150ns, LH5116-20 : 200ns
7. Supply current at standby mode 1 μA
   (MAX.) on +2V supply voltage
8. 24-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{CC}	−0.3～+7.0	V	1
Input voltage	V_{IN}	−0.3～V_{CC}+0.3	V	1
Operating temperature	Topr	0～+70	℃	
Storage temperature	Tstg	−55～+150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ DC Characteristics

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{IL}		−0.3		0.8	V	
Input high voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Output low voltage	V_{OL}	I_{OL}=2.1mA			0.4	V	
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0V, V_{CC}			1.0	μA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V～V_{CC}			1.0	μA	
Current consumption	I_{CC1}	$I_{I/O}$=0mA ($\overline{OE}$=V_{CC})		15	30	mA	1
	I_{CC2}	$I_{I/O}$=0mA ($\overline{OE}$=V_{IH})		25	40	mA	2
Current consumption during standby	I_{CCL}	$\overline{CS}$=V_{CC}, all other input pins=0V−V_{CC}			1	μA	

Note 1 : $\overline{CS}$=0V ; all other input pins=V_{CC}
Note 2 : $\overline{CS}$=V_{IL} ; all other input pins=V_{IH}

■ AC Characteristics

(1) Read cycle

(V_{CC}=5V±10%, Ta=0～+70℃)

Parameter	Symbol	LH5116-15			LH5116-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{RC}	150			200			ns
Access time	t_{ACC}			150			200	ns
Chip enable time	t_{CE}			150			200	ns
Chip select time	t_{CS}	15			20			ns
Output enable access time	t_{OE}			75			100	ns
Output select time	t_{OS}	15			20			ns
Output turn-off time (from $\overline{CE_2}$)	t_{DF1}	0		40	0		60	ns
Output turn-off time (from $\overline{CE_1}$)	t_{DF2}	0		40	0		60	ns
Data hold time	t_{OH}	15			20			ns

(2) Write cycle

(V_{CC}=5V±10%, Ta=0～70℃)

Parameter	Symbol	LH5116-15			LH5116-20			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t_{WC}	150			200			ns
Chip select time	t_{CW}	110			135			ns
Access time	t_{AW}	110			135			ns
Address setup time	t_{AS}	0			5			ns
Pulse width	t_{WP}	110			140			ns
Recovery time	t_{WR}	20			35			ns
Output floating time from $\overline{OE}$	t_{DF1}			40			60	ns
Data setup time	t_{DW}	70			80			ns
Data hold time	t_{DH}	10			10			ns
Output active time from $\overline{WE}$	t_{OW}	15			20			ns
Output floating time from $\overline{OE}$	t_{DF2}			40			60	ns

Test conditions of AC characteristics

- Input voltage amplitude ····· 0.8~2.2V
- Input rise/fall time ····· 10ns
- Timing reference level ····· 1.5V
- Output load condition ····· 1TTL+100pF

■ Low Voltage Data Hold Characteristics

(V_{CC}=5V±10%, Ta=0~+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for data hold	V_{CCDR}	$V_{\overline{CS}}=V_{CC}$, $V_{IN}=0V$ or V_{CC}	2.0			V
Supply current for data hold	I_{CCDR}	$V_{CC}=V_{\overline{CS}}=2.0V$, $V_{IN}=0V$ or V_{CC}			1	μA
$\overline{CS}$ setup time	t_{SDR}		t_{RC}			ns
$\overline{CS}$ hold time	t_{RDR}		t_{RC}			ns

■ Capacitance

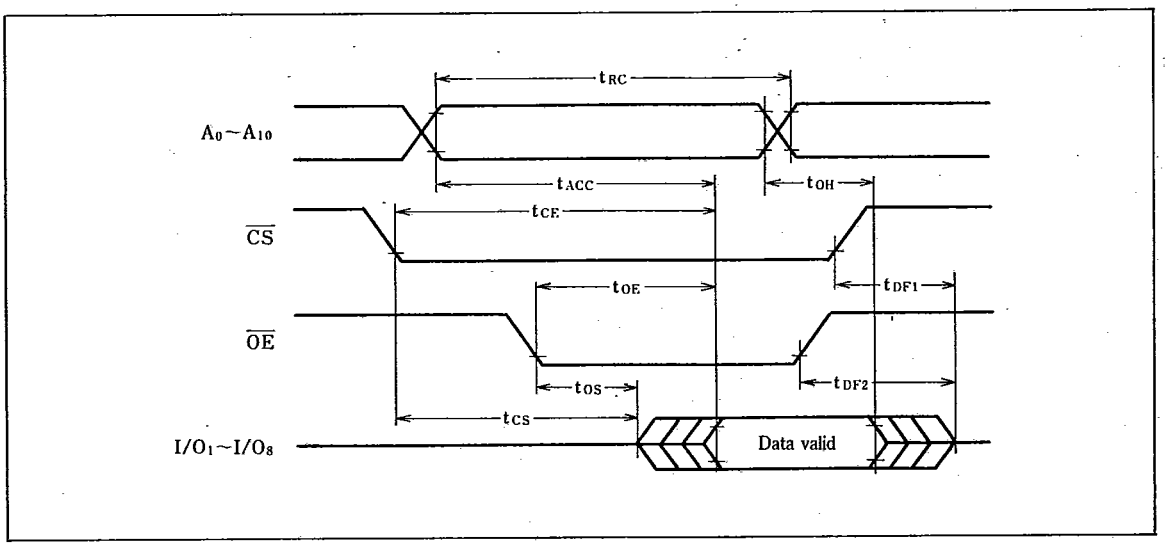
(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$			5	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}=0V$			8	pF

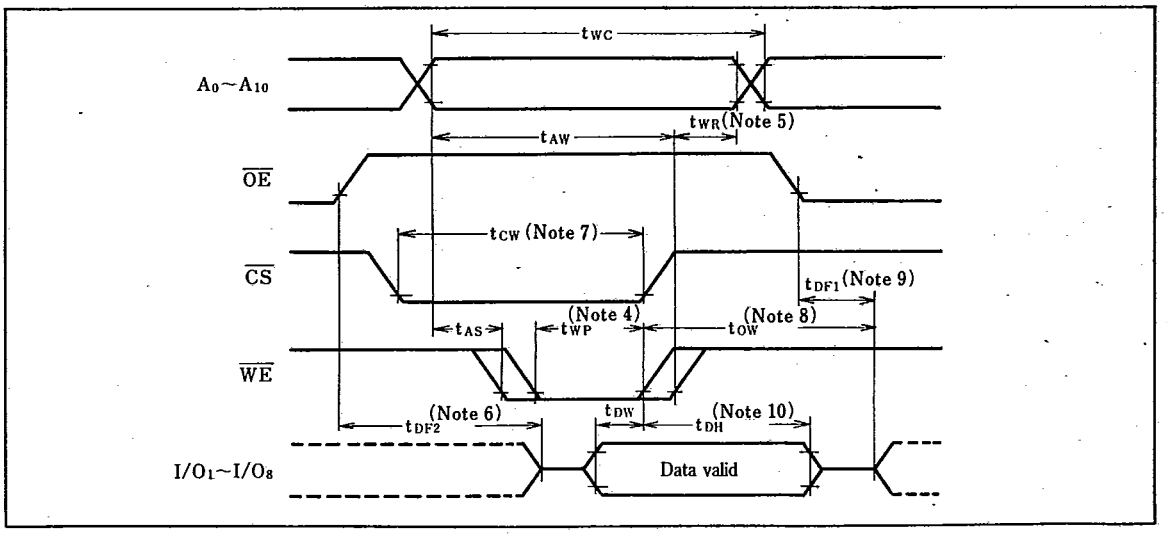
4

■ Timing Diagram

(1) Read cycle



(2) Write cycle (Note 3)



Note 3 : $\overline{WE}$ must be high when there is a change in $A_0 \sim A_{10}$.

Note 4 : When $\overline{CS}$ and $\overline{WE}$ are all low at the same time, write occurs during the period t_{WP}.

Note 5 : t_{WR} is the time from the rise of $\overline{CS}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.

Note 6 : During this period the input/output pin is in an output condition, so input with a phase reversed from that of the output is not permitted.

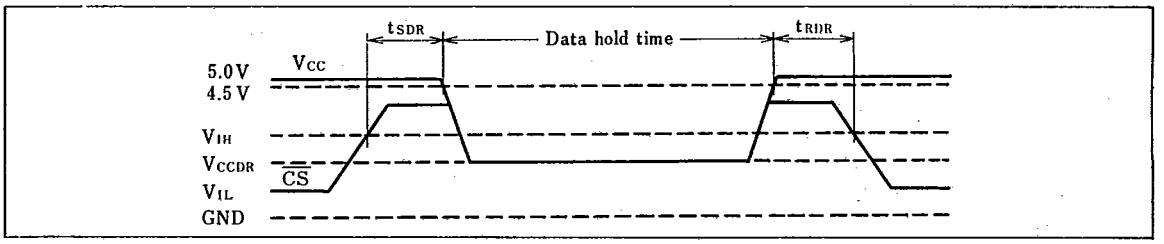
Note 7 : If $\overline{CS}$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high impedance.

Note 8 : $\overline{OE}$ is maintained at "L" level.

Note 9 : Dour outputs data with the same phase as the input data of this write cycle.

Note 10 : If $\overline{CS}$ is low during this period, the input/output pin is in the output condition. During this condition, a data input signal with a phase opposite that of the output is not permitted.

(3) Low voltage data hold



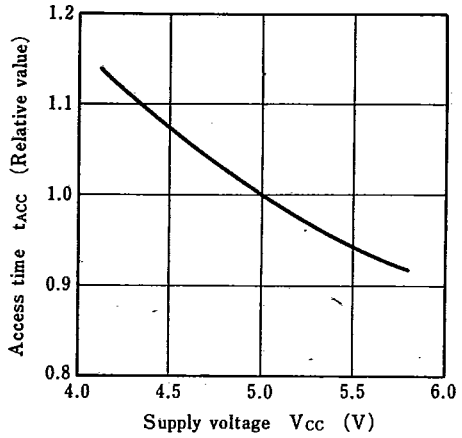
■ Pin Description

Signal	Pin name
$A_0 \sim A_{10}$	Address input
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$I/O_1 \sim I/O_8$	Data input/output
V_{CC}	Power supply
GND	Ground

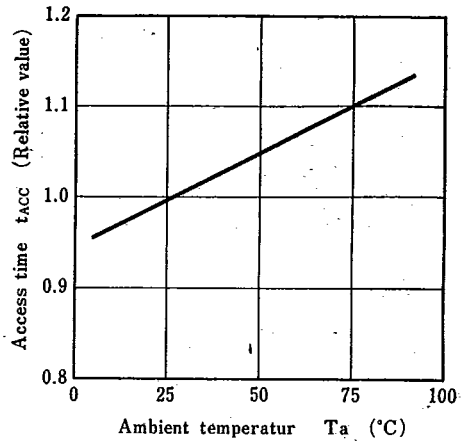
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	$I/O_{1\sim8}$	Supply current
L	X	L	Write	D_{IN}	Operation (I_{CC})
L	L	H	Read	D_{OUT}	Operation (I_{CC})
H	X	X	Deselect	High Z	Standby (I_{CCL})
L	H	X	Output disable	High Z	Operation (I_{CC})

Electrical Characteristics Curves (V_{CC}=5V, Ta=25℃ unless otherwise specified)

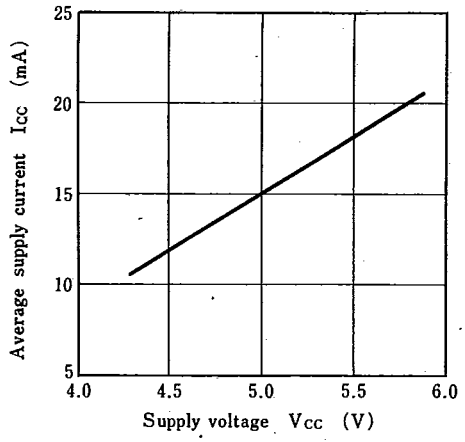
Access time vs. supply voltage



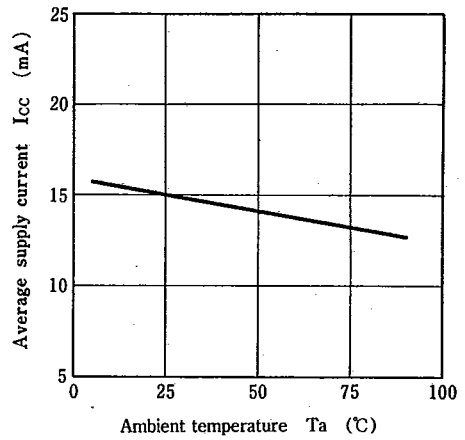
Access time vs. ambient temperature



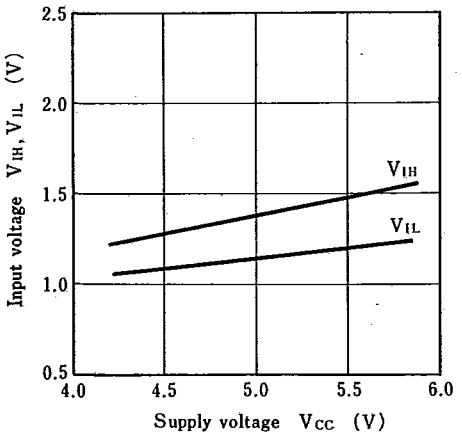
Average supply current vs. supply voltage



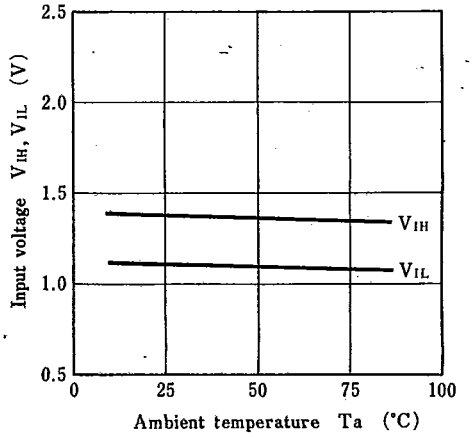
Average supply current vs. ambient temperature



Input voltage vs. supply voltage



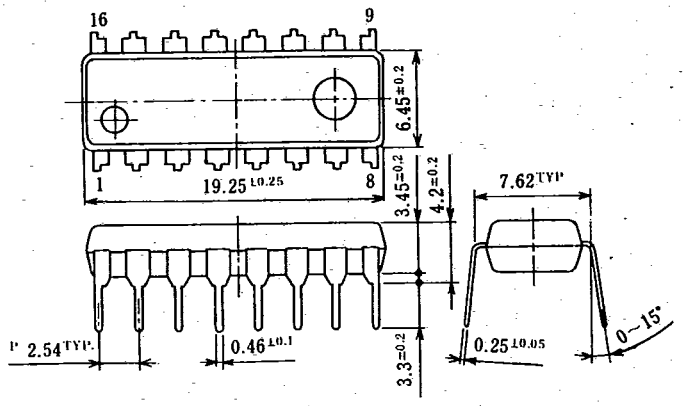
Input voltage vs. ambient temperature



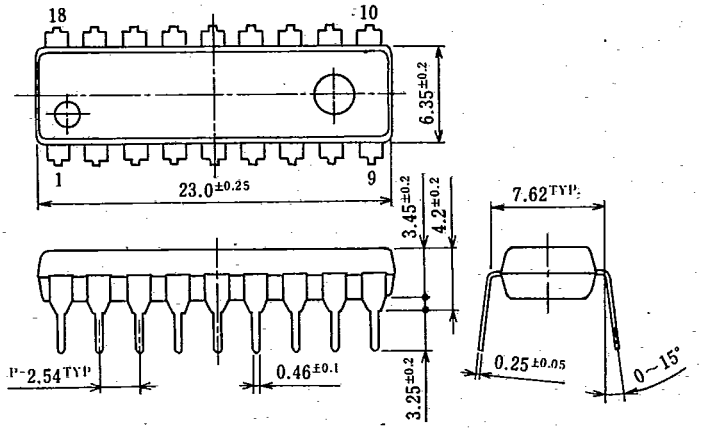
T-90-20

Package Outline (Unit:mm)

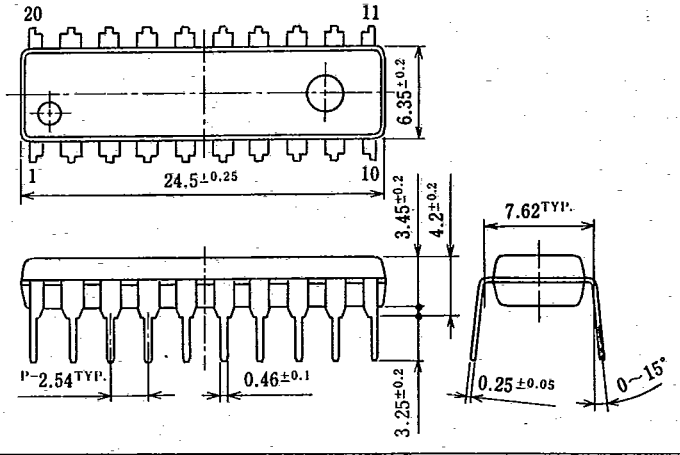
16DIP



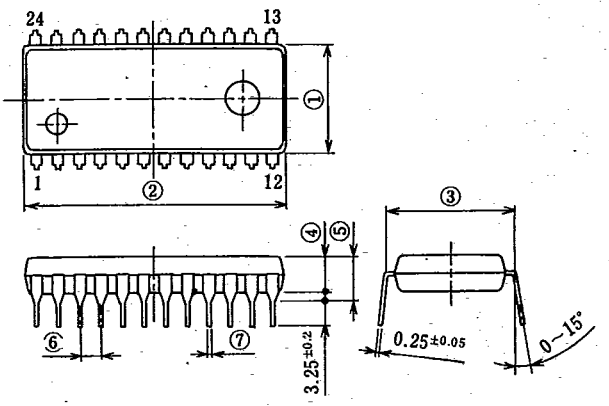
18DIP



20DIP

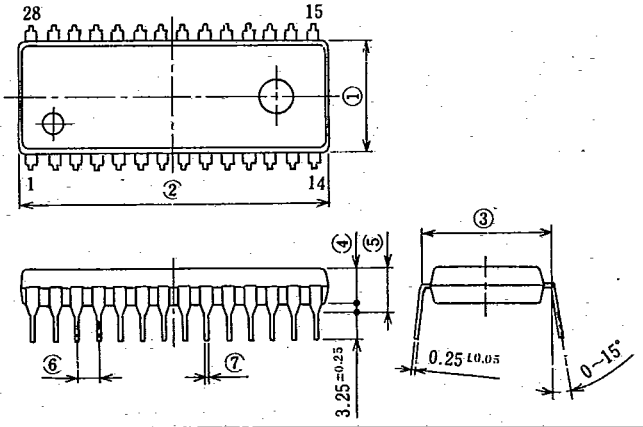


24DIP



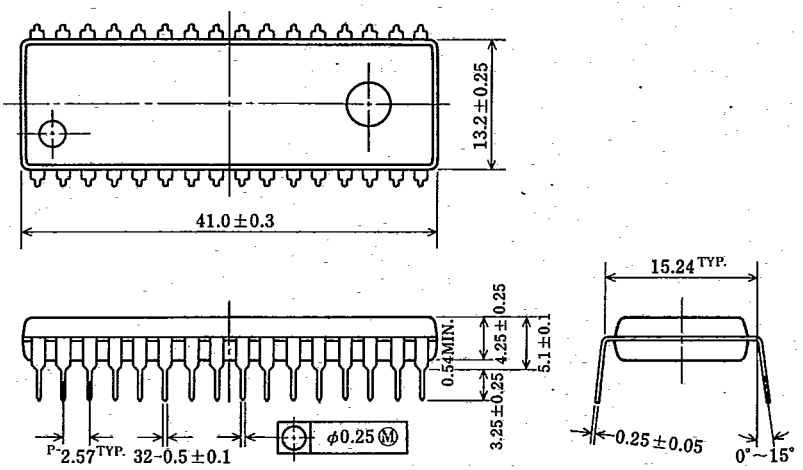
	Normal	Shrink
①	13.2±0.25	6.35±0.2
②	31.0±0.3	22.0±0.25
③	15.24TYP.	7.62TYP.
④	4.25±0.2	3.45±0.2
⑤	5.1±0.2	4.2±0.2
⑥	P-2.54TYP.	P-1.778TYP.
⑦	0.5±0.1	0.46±0.1

28DIP

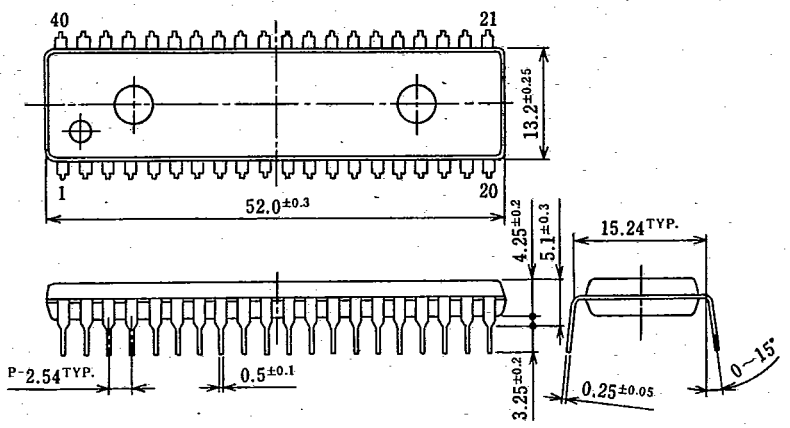


	Normal	Shrink
①	13.2±0.25	8.6±0.2
②	36.0±0.3	25.5±0.25
③	15.24TYP.	10.16TYP.
④	4.25±0.25	3.85±0.2
⑤	5.1±0.2	4.4±0.2
⑥	P-2.54TYP.	P-1.778TYP.
⑦	0.5±0.1	0.46±0.1

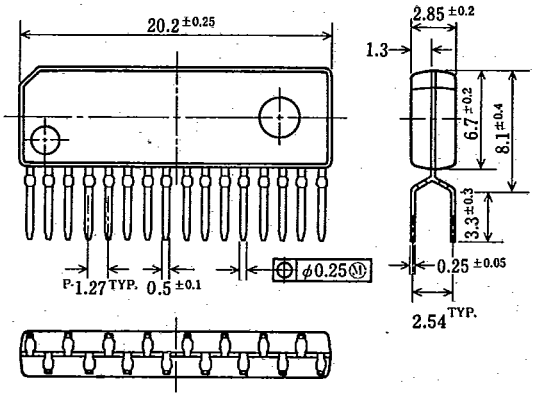
32DIP



40DIP



16ZIP



Package Outline

T-90-20

44QFP