

LH5117

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
100 ns (MAX.)
- Power consumption:
Operating: 220 mW (MAX.)
Standby: 5.5 μ W (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
LH5117H: -40 to +85°C
- Packages:
24-pin, 600-mil DIP
24-pin, 300-mil SK-DIP
24-pin, 450-mil SOP

DESCRIPTION

The LH5117 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The chip select input provides high speed access in read mode.

PIN CONNECTIONS

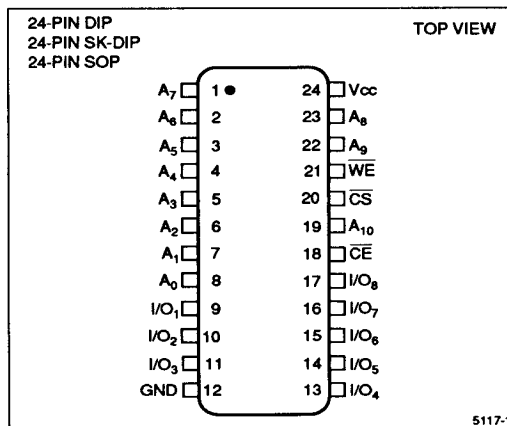


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

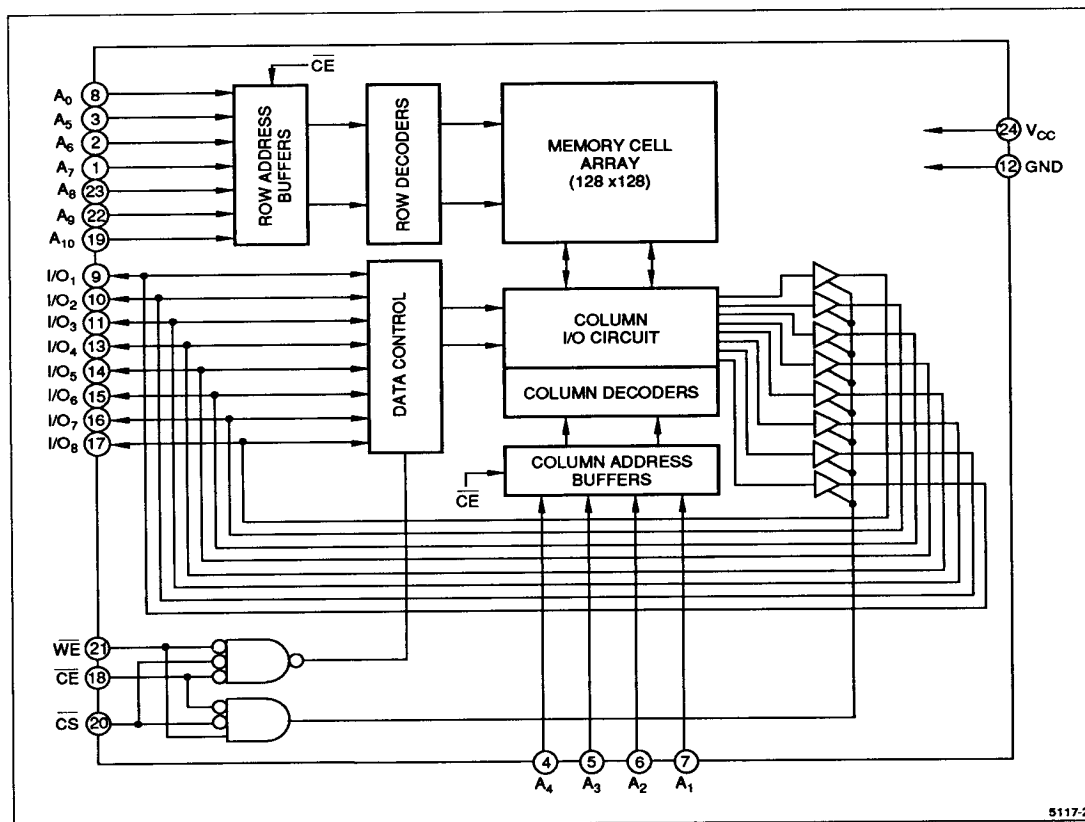


Figure 2. LH5117 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₀	Address input
CE	Chip Enable input
CS	Chip Select input
WE	Write Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data Input/Output
V _{cc}	Power supply
GND	Ground

TRUTH TABLE

CE	CS	WE	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
L	L	L	Write	D _{IN}	Operating (I _{cc})	
L	L	H	Read	D _{OUT}	Operating (I _{cc})	
L	H	X	Deselect	High-Z	Operating (I _{cc})	1
H	X	X	Deselect	High-Z	Standby (I _{sb})	1

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V	1
Operating temperature	T _{opr}	0 to +70	°C	2
		-40 to +85		3
Storage temperature	T _{stg}	-55 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5117/D/N
3. Applied to the LH5117H/HD/HN

RECOMMENDED OPERATING CONDITIONS ¹

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2		V _{CC} + 0.3	V
	V _{IL}	-0.3		0.8	V

NOTE:

1. T_A = 0 to 70°C (LH5117/D/NA), T_A = -40 to +85°C (LH5117H/HD/HN)

DC CHARACTERISTICS ¹ (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V _{OL}	I _{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			V	
Input leakage current	I _{IL}	V _{IN} = 0 V to V _{CC}			1.0	μA	
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$, $\overline{CS} = V_{IH}$, V _{IO} = 0 V to V _{CC}			1.0	μA	
Operating current	I _{CC1}			25	30	mA	2
	I _{CC2}			30	40	mA	3
Standby current	I _{SB}	$\overline{CE} \geq V_{CC} - 0.2 V$, $\overline{CS} \geq V_{CC} - 0.2 V$ or $\overline{CS} \leq 0.2 V$ All other input pins = 0 V to V _{CC}			1.0	μA	
					0.2		4

NOTES:

1. T_A = 0 to 70°C (LH5117/D/N), T_A = -40 to +85°C (LH5117H/HD/HN)
2. $\overline{CE} = 0 V$; all other input pins = 0 V to V_{CC}, outputs open
3. $\overline{CE} = V_L$; all other input pins = V_{IL} to V_{IH}, outputs open
4. T_A = 25°C

AC CHARACTERISTICS ¹**(1) READ CYCLE (V_{CC} = 5 V ± 10%)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t _{RC}	100			ns	
Address access time	t _{AA}			100	ns	
Chip enable access time	t _{ACE}			100	ns	
Chip enable Low to output in Low-Z	t _{CLZ}	10			ns	2
Chip select access time	t _{ACS}			40	ns	
Chip select Low to output in Low-Z	t _{SLZ}	10			ns	2
Chip enable to output in High-Z	t _{CHZ}	0		40	ns	2
Chip select to output in High-Z	t _{SHZ}	0		40	ns	2
Output hold time	t _{OH}	10			ns	

(2) WRITE CYCLE¹ ($V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t _{WC}	100			ns	
Chip enable to end of write	t _{CEW}	80			ns	
Address valid time	t _{AW}	80			ns	
Address setup time	t _{AS}	0			ns	
Write pulse width	t _{WP}	60			ns	
Write recovery time	t _{WR}	10			ns	
Write enable Low to output in High-Z	t _{WEH-Z}			30	ns	2
Data valid to end of write	t _{DW}	30			ns	
Data hold time	t _{DH}	10			ns	
Output active from end of write	t _{OW}	10			ns	2

NOTE:

1. $T_A = 0$ to $+70^\circ\text{C}$ (LH5117/D/N), $T_A = -40$ to $+85^\circ\text{C}$ (LH5117H/HD/HH)
2. Active output to high-impedance and high-impedance to output active tests specified for a ± 500 mV transition from steady state levels into the test load. $C_{LOAD} = 5$ pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS¹

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCRC} - 0.2\text{ V}$	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2$, $\overline{CS} \geq V_{CCDR} - 0.2$ or $\overline{CS} \leq 0.2\text{ V}$, $V_{CCDR} = 3.0\text{ V}$			1.0 0.2	μA	2
Chip disable to data retention	t _{CDR}		0			ns	
Recovery time	t _R		t _{RC}			ns	3

NOTES:

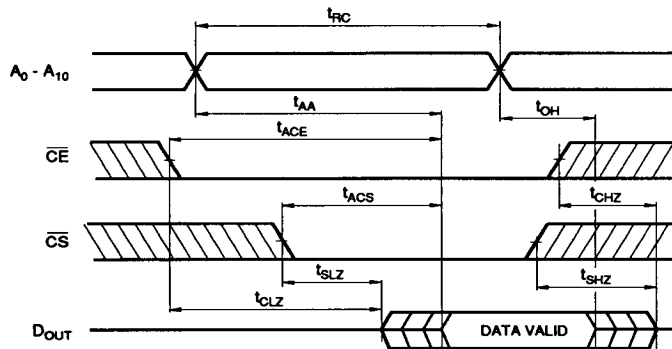
1. $T_A = 0$ to $+70^\circ\text{C}$ (LH5117/D/N), $T_A = -40$ to $+85^\circ\text{C}$ (LH5117H/HD/HH)
2. $T_A = 25^\circ\text{C}$
3. t_{RC} = Read cycle time

CAPACITANCE¹ ($f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C _{IN}	$V_{IN} = 0\text{ V}$			7	pF
Input/output capacitance	C _{IO}	$V_{IO} = 0\text{ V}$			10	pF

NOTE:

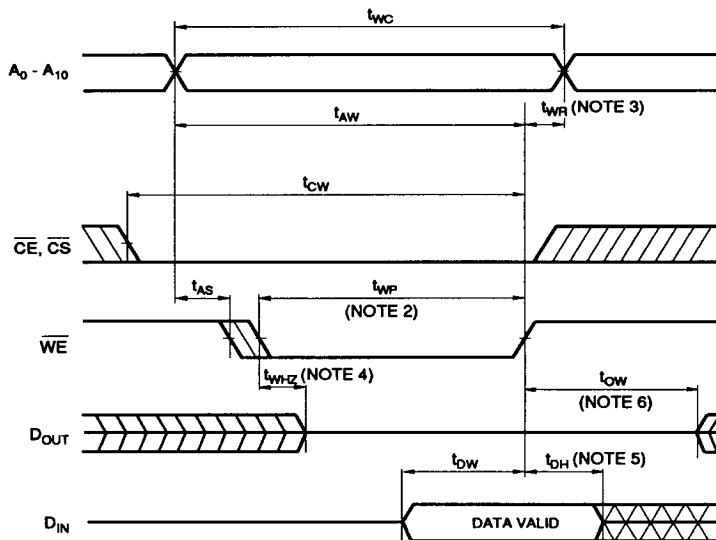
1. This parameter is sampled and not production tested.



NOTE: $\overline{WE}$ = "HIGH"

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Figure 3. Read Cycle

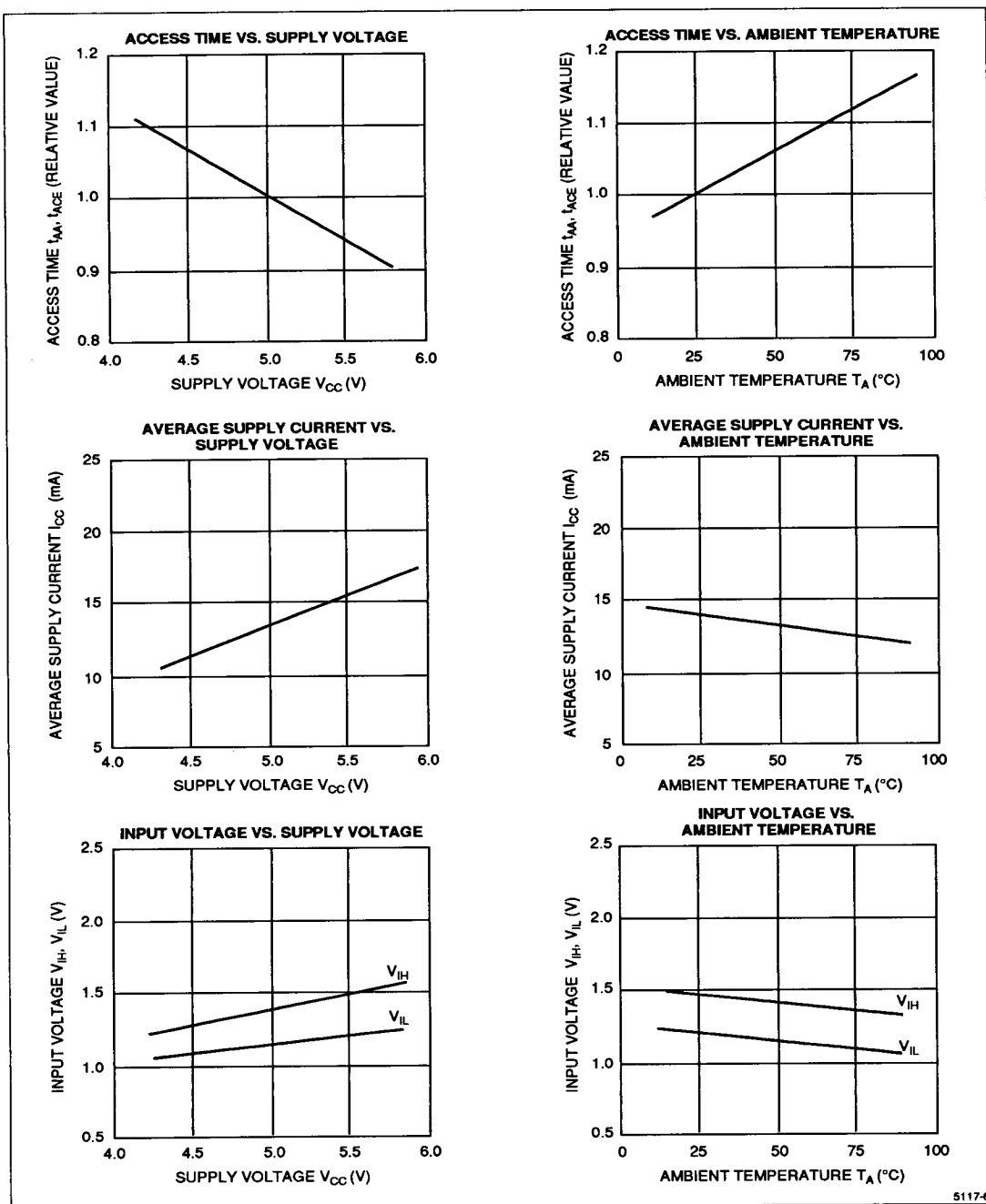


NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in $A_0 - A_{10}$.
2. When CE, CS and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP} .
3. t_{WR} is the time from the rise of CE, CS or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If CE or CS LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If both CE and CS are LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

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Figure 4. Write Cycle



5117-6

Figure 5. Electrical Characteristic Curves
($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ Unless Otherwise Specified)

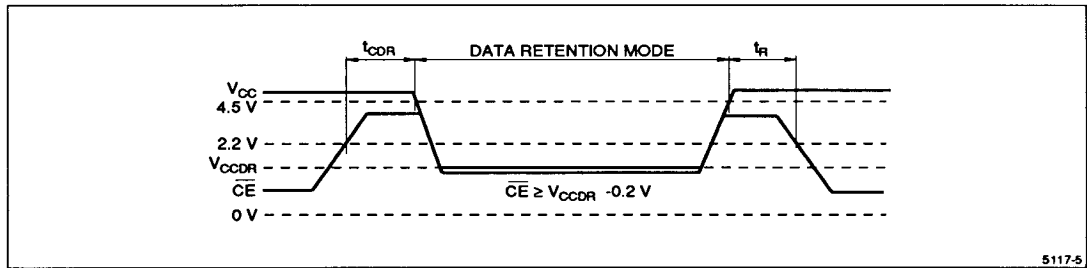


Figure 6. Low Voltage Data Retention

ORDERING INFORMATION ($T_A = 0$ to $+70^\circ\text{C}$)

LH5117	X	- ##	
Device Type	Package	Speed	
		10 100	Access Time (ns)
			{ Blank 24-pin, 600-mil DIP (DIP24-P-600) D 24-pin, 300-mil SK-DIP (DIP24-P-300) N 24-pin, 450-mil SOP (SOP24-P-450)
			CMOS 16K (2K x 8) Static RAM

Example: LH5117N-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

ORDERING INFORMATION ($T_A = -40$ to $+85^\circ\text{C}$)

LH5117H	X	- ##	
Device Type	Package	Speed	
		10 100	Access Time (ns)
			{ Blank 24-pin, 600-mil DIP (DIP24-P-600) D 24-pin, 300-mil SK-DIP (DIP24-P-300) N 24-pin, 450-mil SOP (SOP24-P-450)
			CMOS 16K (2K x 8) Static RAM

Example: LH5117HN-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)