LH5118

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5118H: -40 to + 85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil SOP

DESCRIPTION

The LH5118 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5118 accepts two chip-enables. These allow data to be held with battery back-up for memory expansion (used in systems with multiple memory devices).

Low power mode (I_{SB}) is available with $\overline{CE}_1$ and $\overline{CE}_2$ deactivated.

PIN CONNECTIONS

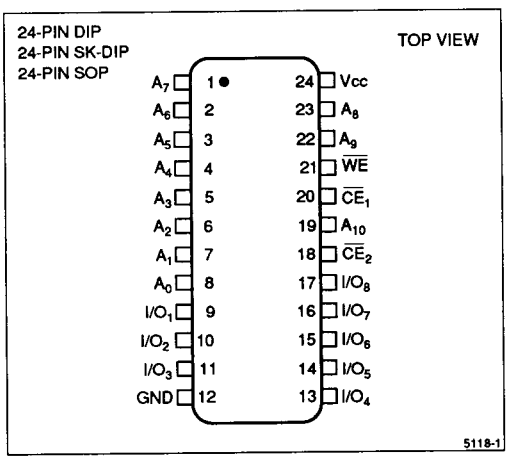


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

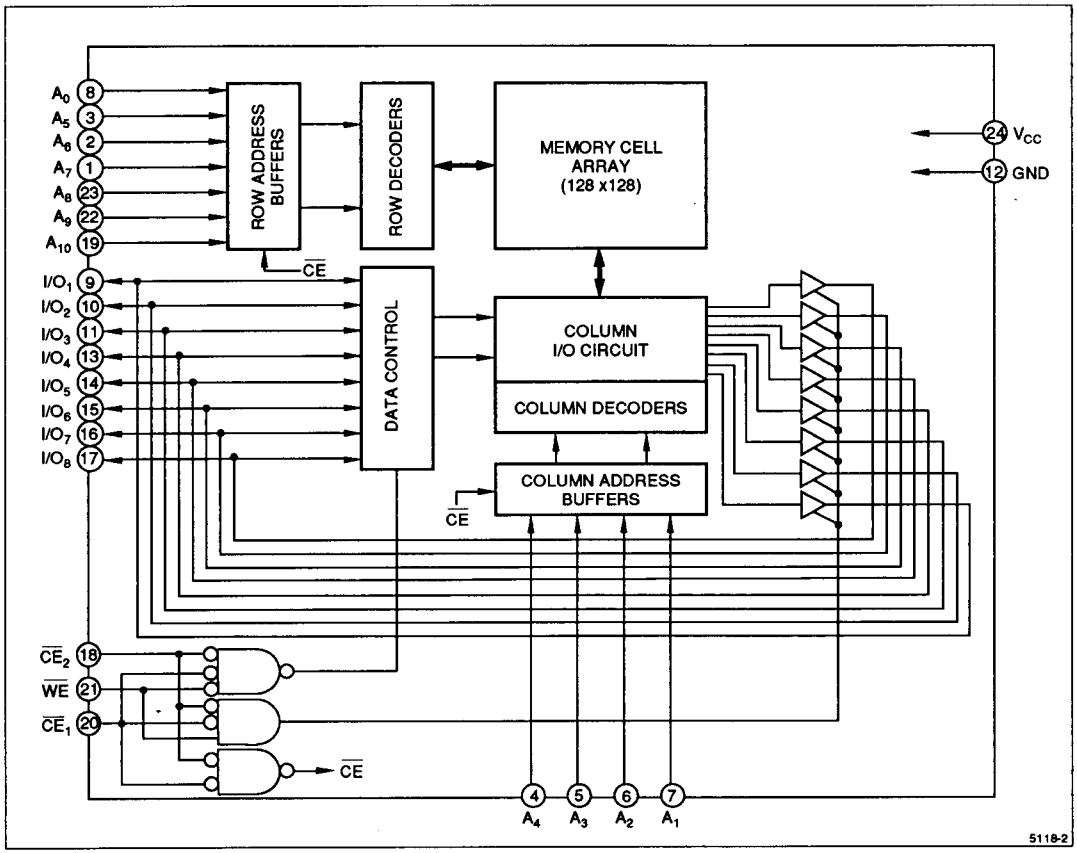


Figure 2. LH5118 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}_2$	Chip Enable input no. 2
$\overline{CE}_1$	Chip Enable input no. 1
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
X	H	X	Deselect	High-Z	Standby (I_{SB})	1
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	L	L	Write	D_{IN}	Operating (I_{CC})	
L	L	H	Read	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5118/D/N
3. Applied to the LH5118H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to +70°C (LH5118/D/NA), T_A = -40 to +85°C (LH5118H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_2}$ = V_{IH} or $\overline{CE_1}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{WE}$ = V_{CC})		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{WE}$ = V_{IH})		30	40	mA	3
Standby current	I_{SB}	(1) $\overline{CE_2} \geq V_{CC}$ - 0.2 V, and ($\overline{CE_1} \geq V_{CC}$ - 0.2 V or $\overline{CE_1} \leq$ 0.2 V) or			1.0	µA	
		(2) $\overline{CE_1} \geq V_{CC}$ - 0.2 V, and ($\overline{CE_2} \geq V_{CC}$ - 0.2 V or $\overline{CE_2} \leq$ 0.2 V) All other inputs = 0 V to V_{CC}			0.2	µA	4

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. $\overline{CE_2}$ = $\overline{CE_1}$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE_2}$ = $\overline{CE_1}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
$\overline{CE}_1$ access time	t_{ACE1}			100	ns	
$\overline{CE}_2$ access time	t_{ACE2}			100	ns	
$\overline{CE}_1$ Low to output in Low-Z	t_{CLZ1}	10			ns	2
$\overline{CE}_2$ Low to output in Low-Z	t_{CLZ2}	10			ns	2
$\overline{CE}_1$ to output in High-Z	t_{CHZ1}	0		40	ns	2
$\overline{CE}_2$ to output in High-Z	t_{CHZ2}	0		40	ns	2
Data hold time	t_{OH}	10			ns	

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output active from end of write	t_{OW}	10			ns	2

NOTE:

1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_1} \geq V_{CCDR} - 0.2V$ or $\overline{CE_2} \geq V_{CCDR} - 0.2$ V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE_1} \geq V_{CCDR} - 0.2V$, and ($\overline{CE_2} \geq V_{CCDR} - 0.2$ V or $\overline{CE_2} \leq 0.2$ V) or			1.0	µA	
		$\overline{CE_2} \geq V_{CCDR} - 0.2V$, and ($\overline{CE_1} \geq V_{CCDR} - 0.2$ V or $\overline{CE_1} \leq 0.2$ V) $V_{CCDR} = 3.0$ V			0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

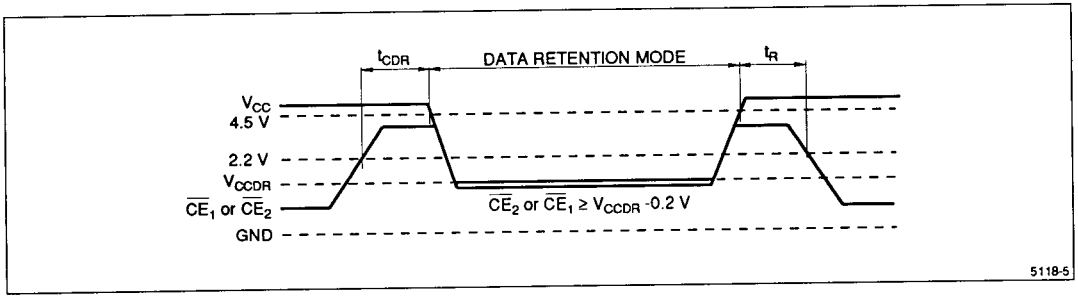
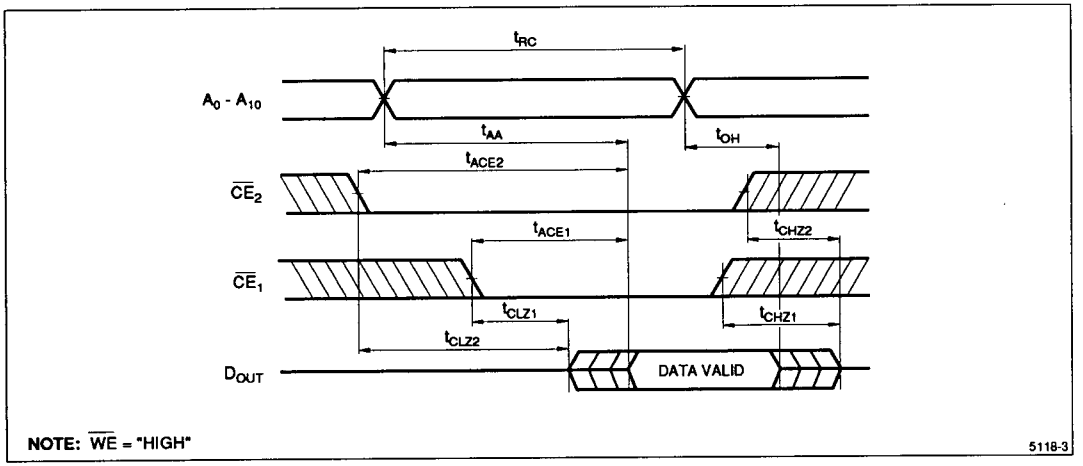


Figure 3. Low Voltage Data Retention



NOTE: $\overline{WE}$ = "HIGH"

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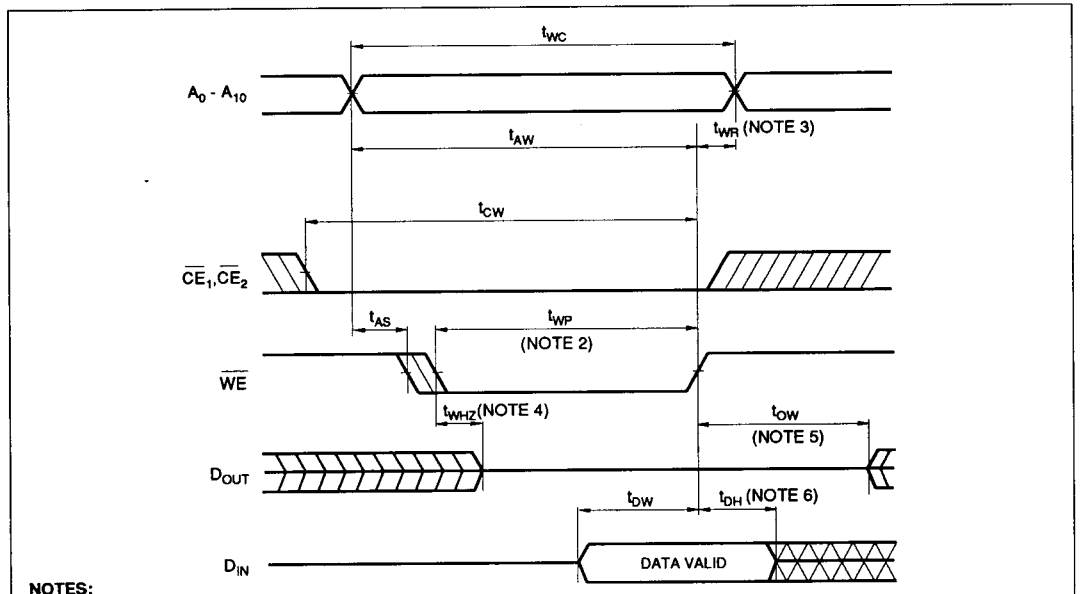
Figure 4. Read Cycle



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}_2$,$\overline{CE}_1$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}_2$,$\overline{CE}_1$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}_2$ or $\overline{CE}_1$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If both $\overline{CE}_1$ and $\overline{CE}_2$ are LOW during this period, the input/output pin is in the output condition. During this condition, a data input signal with a logic level opposite that of the output is not permitted.

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Figure 5. Write Cycle (Note 1)

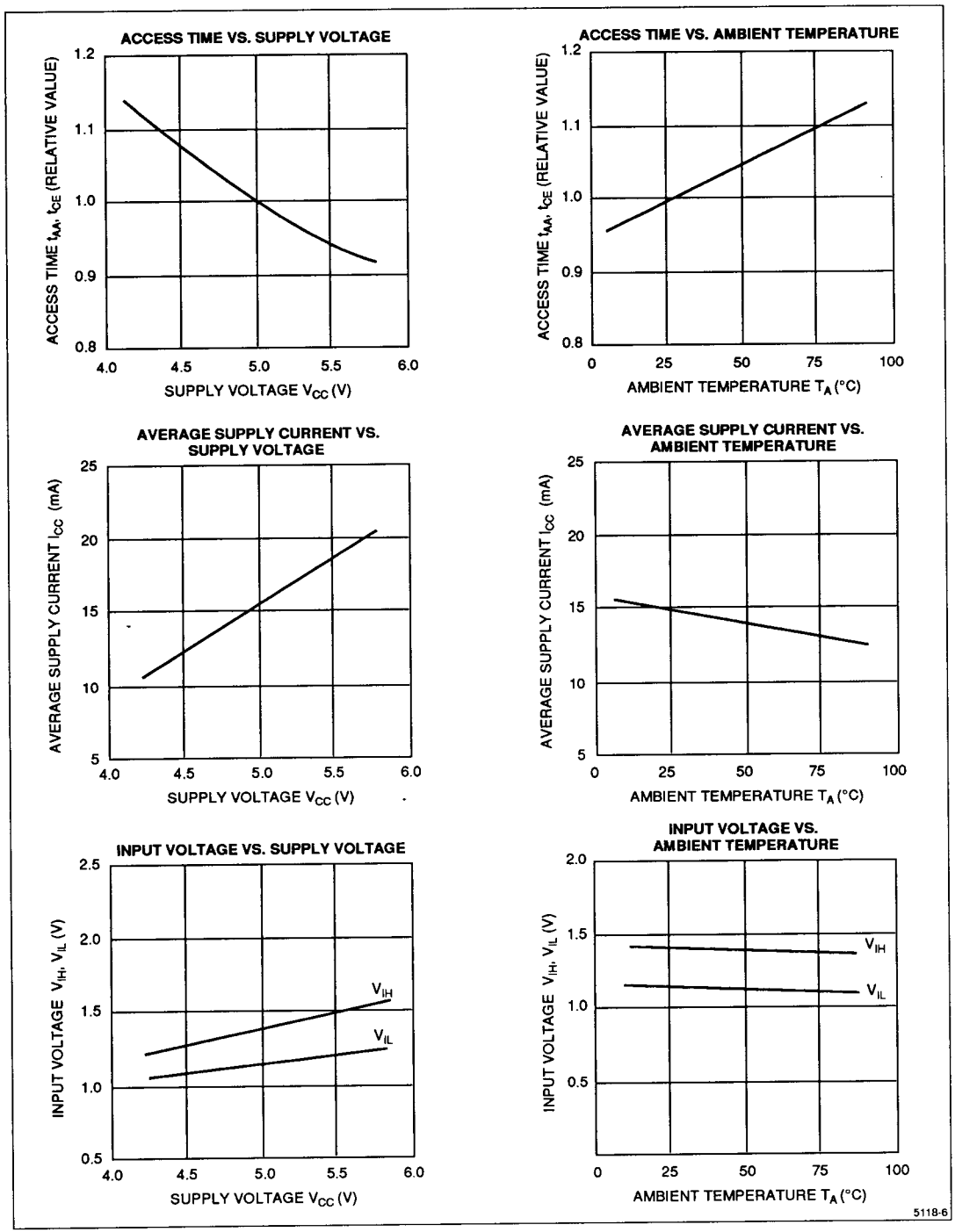
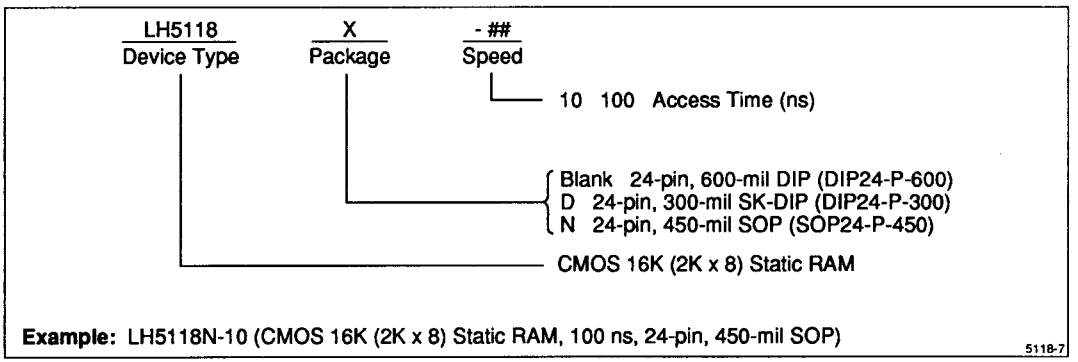


Figure 6. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C Unless Otherwise Specified)

ORDERING INFORMATION (T_A = 0 to +70°C)



Example: LH5118N-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

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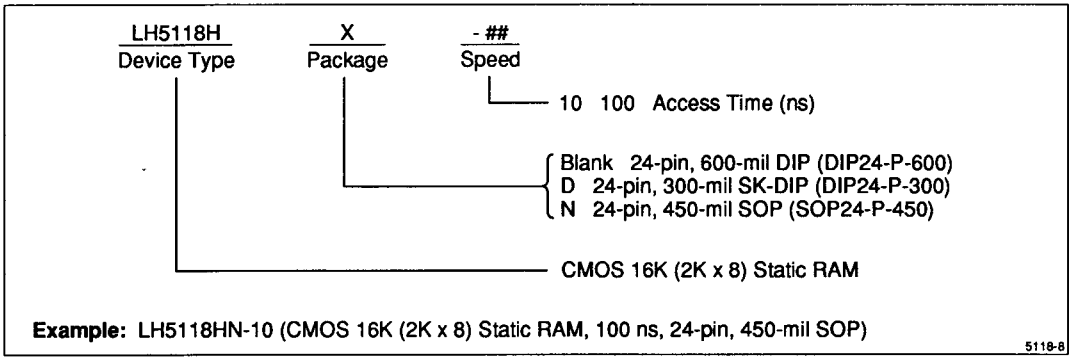
ORDERING INFORMATION (T_A = -40 to +85°C)



Example: LH5118HN-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

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