LH51V1032C4

PRELIMINARY

32K × 32 Pipelined Burst SRAM

+3.3 V Supply, Fully Registered Inputs, Outputs, and Burst Counter

FEATURES

- Fast Access Times: 8 and 9 ns
- Fast Cycle Times:
  15 ns (66.7 MHz)
  17 ns (60 MHz)
- Fast Asynchronous $\overline{OE}$: 5 ns
- Single +3.3 V ±5% Power Supply
- Common Data Inputs and Data Outputs
- Individual BYTE WRITE Control
  – Global Write Enable
  – Byte Write Enable
- Three Chip Enables for Simple Depth Expansion
- Registered Address, Data I/O and Control for Fully Pipelined Applications
- Internally Self-Timed WRITE Cycle
- WRITE Pass-Through Capability
- Burst Address Counter Mode Control Pins
  – User-Selectable Interleaved/Linear Burst Mode Control (MODE)
- Low Capacitive Bus Loading
- Package: 100-pin TQFP

FUNCTIONAL DESCRIPTION

The Sharp Synchronous SRAM family employs high-speed, low-power CMOS designs using a thin-film transistor memory cell. Sharp SRAMs are fabricated using double-layer metal, three-layer polysilicon technology.

The LH51V1032C4 SRAM integrates a 32K × 32 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable, two additional chip enables for easy depth expansion ($\overline{CE}_2$, CE_2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$), the byte write controls ($\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$), Global Write ($\overline{GW}$), and Byte Write Enable ($\overline{BWE}$).

The Global Write control provides for a Write operation to all bytes, ignoring the state of the individual Byte Write controls and Byte Write Enable. Byte Write Enable provides a mechanism for enabling/disabling all individual Byte Write Controls.

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$). The MODE control provides a selection between Interleaved Burst Mode addressing and Linear Burst Mode addressing. The pin should be hardwired to V_{SS} for Linear Burst Mode operation, and floating for Interleaved Burst Mode operation.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response.

The LH51V1032C4 operates from a +3.3 V power supply and all inputs and outputs are LVTTL compatible. The device is ideal for Pentium (P5) pipelined applications and 32- and 64-bit wide applications.

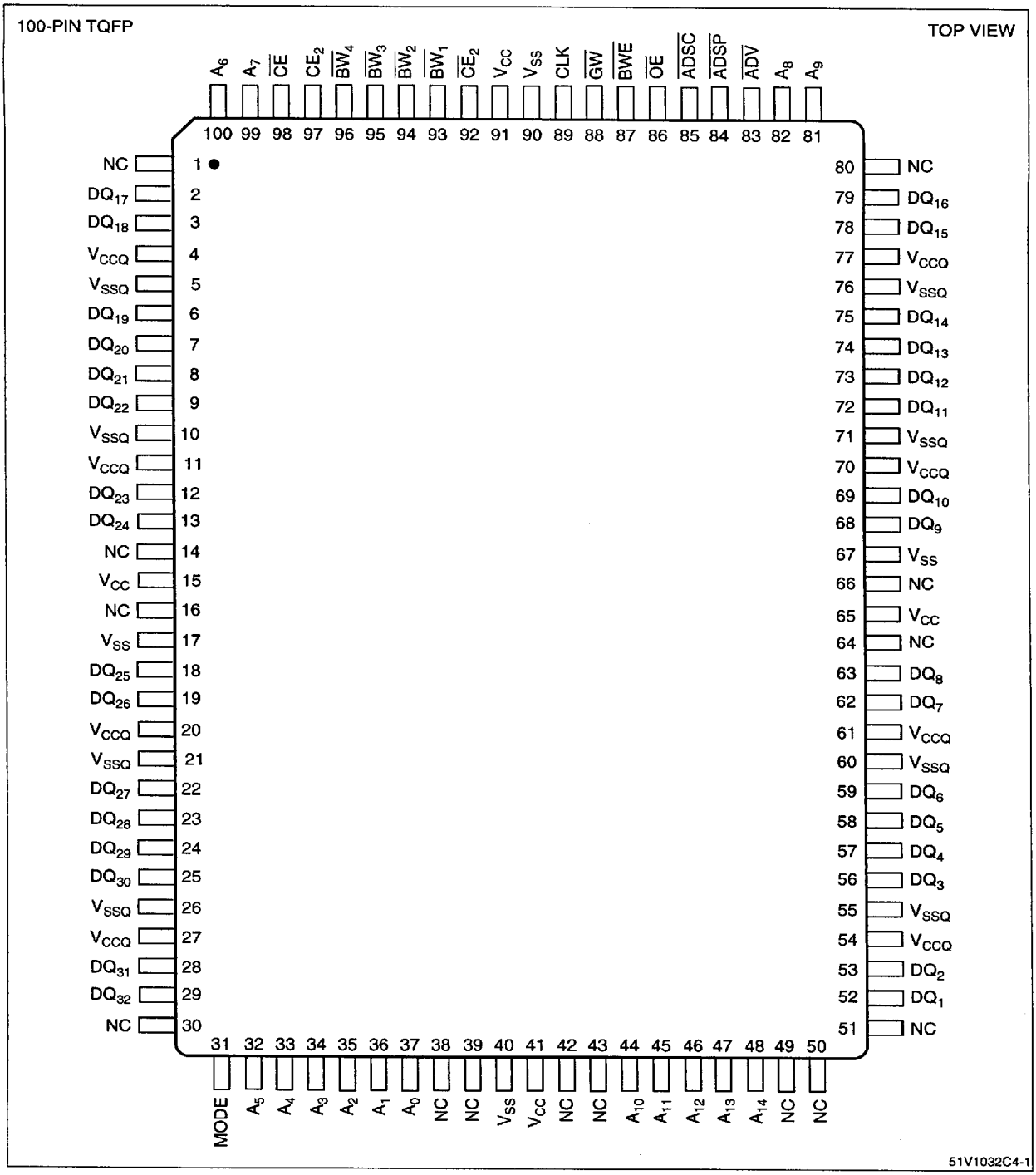


Figure 1. Pin Connections for TQFP Package

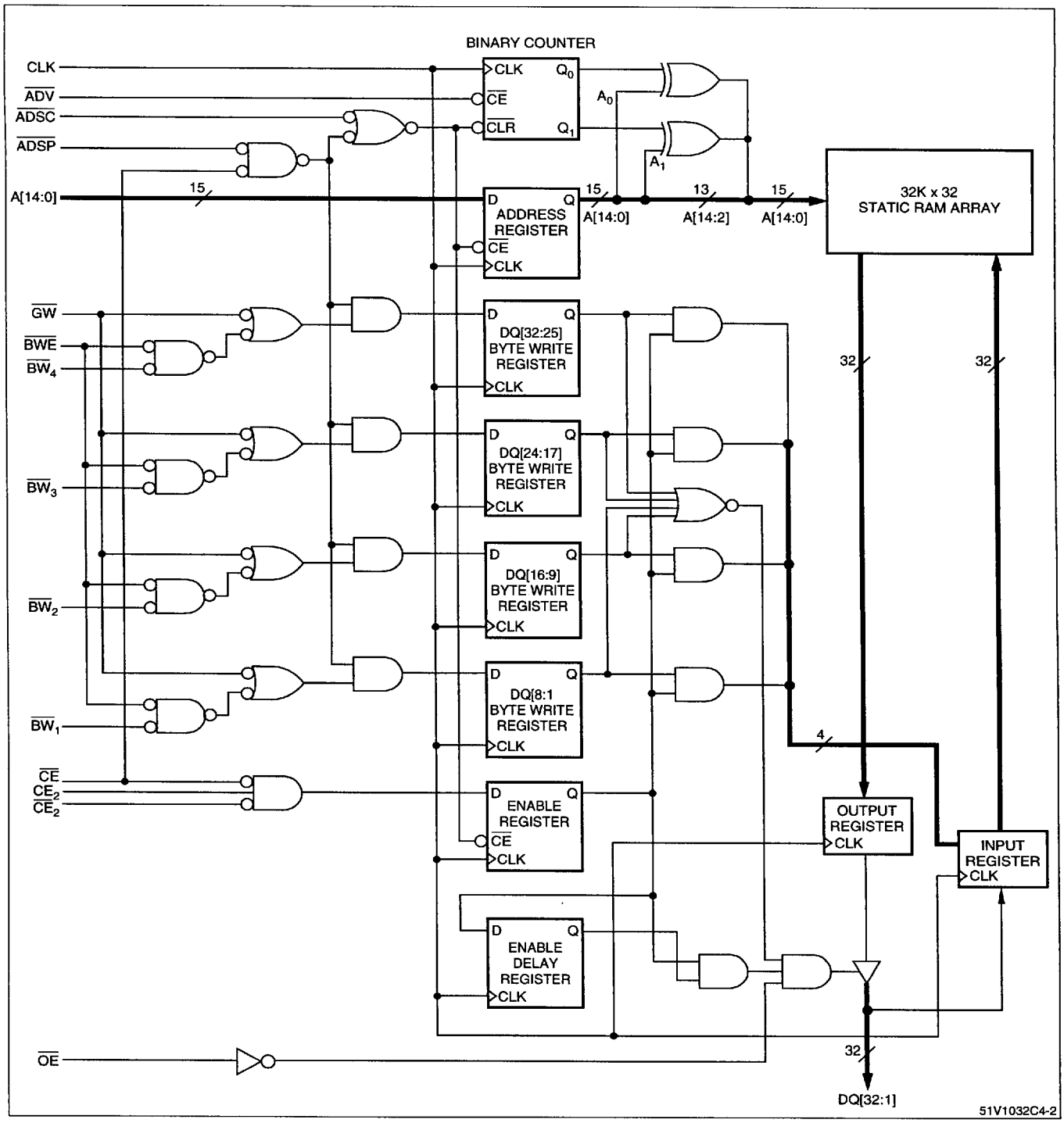


Figure 2a. LH51V1032C4 Block Diagram
(MODE = V_{CC} or NC, Interleaved Addressing)

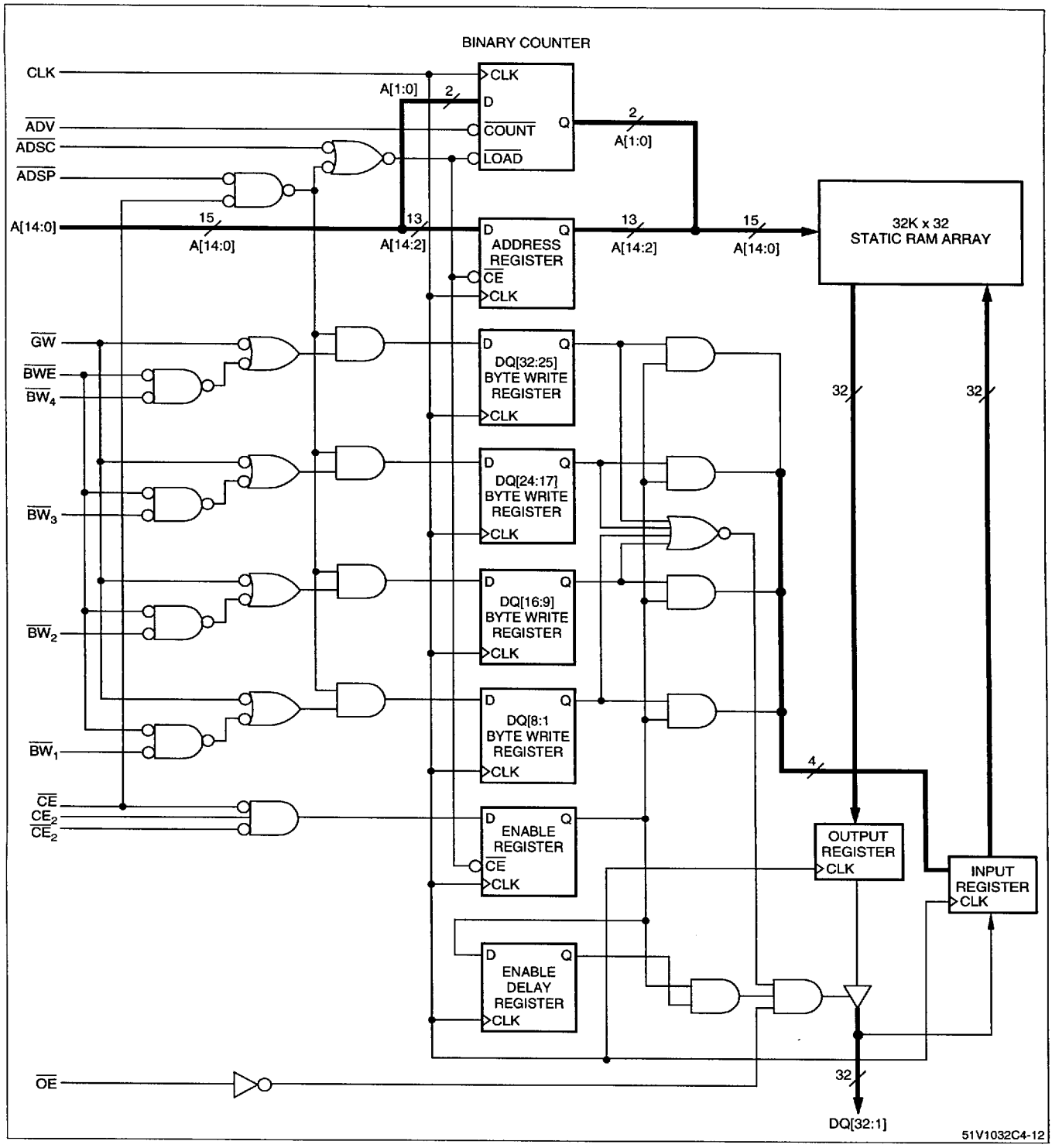


Figure 2b. LH51V1032C4 Block Diagram (MODE = V_{SS}, Linear Addressing)

PIN DESCRIPTIONS

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
32, 33, 34, 35, 36, 37, 44, 45, 46, 47, 48, 81, 82, 99, 100	A_0-A_{14}	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
31	MODE	Input	V_{CC} or No Connect (i.e., float) for Interleaved Burst, tied to V_{SS} for Linear Burst.
93, 94, 95, 96	$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$	Input	Synchronous Byte Write: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A Byte Write Enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW_1}$ controls DQ_1-DQ_8. $\overline{BW_2}$ controls DQ_9-DQ_{16}. $\overline{BW_3}$ controls DQ_{17}-DQ_{24}. $\overline{BW_4}$ controls DQ_{25}-DQ_{32}. The Byte Write controls interact with Global Write and Byte Write Enable. See the Write Operation Truth Table.
87	$\overline{BWE}$	Input	When active LOW, $\overline{BWE}$ allows individual Byte Write operations. When inactive HIGH, only Global Write operations are allowed using the $\overline{GW}$ control.
88	$\overline{GW}$	Input	When active, a Write operation is selected for all bytes, with the $\overline{BW}$ controls and the $\overline{BWE}$ control all 'Don't Care.' When inactive HIGH, the control of Write operations reverts to the combination of the $\overline{BW}$ controls and the $\overline{BWE}$ control.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new base address is loaded.
92, 97	$\overline{CE_2}$, CE_2	Input	Synchronous Chip Enables: These inputs are used to enable the device. These inputs are sampled only when a new base address is loaded.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the Data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the initial address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causes a new external address to be latched and a read performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon the Chip Enables.

PIN DESCRIPTIONS (cont'd)

PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input, when $\overline{ADSP}$ is HIGH, interrupts any ongoing burst, causes a new external address to be latched, and performs a read or write using the new address dependent upon the Chip Enables. When $\overline{ADSC}$ and $\overline{ADSP}$ are both LOW, a new address is latched and a Read operation is performed on that address.
1, 14, 16, 30, 38, 39, 42, 43, 49, 50, 51, 64, 66, 80	NC	–	No Connect: These signals are not internally connected.
2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79	DQ_1-DQ_{32}	Input/Output	SRAM Data I/O: Byte 1 is DQ_1-DQ_8; Byte 2 is DQ_9-DQ_{16}; Byte 3 is DQ_{17}-DQ_{24}; Byte 4 is DQ_{25}-DQ_{32}. Input data must meet setup and hold times around the rising edge of CLK.
15, 41, 65, 91	V_{CC}	Supply	Power Supply: +3.3 V ±5%
17, 40, 67, 90	V_{SS}	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	V_{CCQ}	Supply	Output Buffer Supply: +3.3 V ±5%
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	Supply	Output Buffer Ground: GND

PASS-THROUGH TRUTH TABLE [1]

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WRITE}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All Bytes	Initiate READ cycle Register A(n), Q = D (n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All Bytes	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All Bytes	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One Byte	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTES:

1. Previous cycle may be either BURST or NONBURST cycle.
2. See the Write Operation Truth Table.

BURST SEQUENCE TABLE
Interleaved Burst (MODE = NC or V_{CC})

OPERATION	ADDRESS USED		
	A_{14}-A_2	A_1	A_0
First access, latch external address	A_{14}-A_2	A_1	A_0
Second access (first burst address)	Latched A_{14}-A_2	Latched A_1	Latched $\overline{A}_0$
Third access (second burst address)	Latched A_{14}-A_2	Latched $\overline{A}_1$	Latched A_0
Fourth access (third burst address)	Latched A_{14}-A_2	Latched $\overline{A}_1$	Latched $\overline{A}_0$

NOTE:
The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE
Interleaved Burst (MODE = NC or V_{CC})

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

BURST ADDRESS TABLE
Linear Burst (MODE = V_{SS})

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

WRITE OPERATION TRUTH TABLE

GW	$\overline{BWE}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	$\overline{BW}_4$	OPERATION
H	H	X	X	X	X	No Write, Read Cycle
L	X	X	X	X	X	Global Write
H	L	L	X	X	X	Write Byte 1
H	L	X	L	X	X	Write Byte 2
H	L	X	X	L	X	Write Byte 3
H	L	X	X	X	L	Write Byte 4
H	L	–	–	–	–	Tie $\overline{GW}$ HIGH and $\overline{BWE}$ LOW for Backwards Compatibility ($\overline{BW}_1$-$\overline{BW}_4$ Control Write Operations)

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE_2}$	CE_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTES:

1. X means 'don't care.' H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means that either: one or more of the byte write enable signals are active LOW ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$ or $\overline{BW_4}$) AND $\overline{BWE}$ is active LOW, $\overline{GW}$ is active LOW.
2. $\overline{BW_1}$ enables writes to Byte 1 (DQ_1-DQ_8). $\overline{BW_2}$ enables writes to Byte 2 (DQ_9-DQ_{16}). $\overline{BW_3}$ enables writes to Byte 3 (DQ_{17}-DQ_{24}). $\overline{BW_4}$ enables writes to Byte 4 (DQ_{25}-DQ_{32}).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This is device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is any Write operation, either byte, combination of bytes, or word. (For details, see the Write Operation Truth Table). Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Voltage on V_{CC} Supply Relative to V_{SS}	−0.5 V to +4.6 V
V_{IN}	−0.5 V to V_{CC} + 0.5 V
Storage Temperature (Plastic)	−55°C to +150°C
Junction Temperature	+150°C
Power Dissipation	1.6 W
Short Circuit Output Current [2]	100 mA

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. One output at a time, one second maximum duration.

ELECTRICAL CHARACTERISTICS
($0°C \le T_A \le 70°C$; $T_C \le 110°C$; V_{CC} = 3.3 V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC} + 0.3 V	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	−0.3	0.8	V	1, 2
Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$	I_{LI}	−1	1	µA	
Output Leakage Current	Output(s) Disabled, $0 V \le V_{OUT} \le V_{CC}$	I_{LO}	−1	1	µA	
Output High Voltage	I_{OH} = −8.0 mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

NOTES:

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \le V_{CC}$ + 2.0 V for 10 ns. Undershoot: $V_{IL} \ge$ −2.0 V for 10 ns.

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3 V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	MAX.		UNITS	NOTES
				–15	–17		
Power Supply Current: Operating	Device Selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} min; V_{CC} = MAX; outputs open	I_{CC}	150	250	220	mA	1, 2, 3
Power Supply Current: Idle	Device Selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BW}$s ≥ V_{IH}; all inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V; V_{CC} = MAX; cycle time ≥ t_{KC} min, Outputs Open	I_{CC1}	20	35	30	mA	2, 3
CMOS Standby	Device Deselected; V_{CC} = MAX; all inputs ≤ V_{SS} + 0.2 or ≥ V_{CC} – 0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	mA	2, 3
TTL Standby	Device Deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	mA	2, 3
Clock Running	Device Deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ t_{KC} min	I_{SB4}	20	35	30	mA	2, 3

NOTES:

1. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
2. 'Device Deselected' means device is in POWER-DOWN mode as defined in the truth table. 'Device Selected' means device is active (not in POWER-DOWN mode).
3. Typical values are measured at 3.3 V, 25°C and 15 ns cycle time.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 3.3 V	C_I	3	4	pF	1
Input/Output Capacitance (DQ)		C_O	6	7	pF	1

NOTE:

1. This parameter is sampled.

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance – Junction to Ambient	Still Air	θ_{JA}	42	°C/W	
Thermal Resistance – Junction to Case		θ_{JC}	TBD		
Maximum Case Temperature		TC	110	°C	1

NOTE:

1. Sharp does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1]
(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3 V ±5%)

DESCRIPTION	SYMBOL	–15		–17		UNITS	NOTES
		MIN	MAX	MIN	MAX		
CLOCK							
Clock Cycle Time	t_{KC}	15		16.7		ns	
Clock HIGH Time	t_{KH}	5		6		ns	
Clock LOW Time	t_{KL}	5		6		ns	
OUTPUT TIMES							
Clock to Output Valid	t_{KQ}		8		9	ns	
Clock to Output Invalid	t_{KQX}	3		3		ns	
Clock to Output in Low-Z	t_{KQLZ}	5		5		ns	2, 3
Clock to Output in High-Z	t_{KQHZ}		5		6	ns	2, 3
OE to Output Valid	t_{OEQ}		5		5	ns	4
OE to Output in Low-Z	t_{OELZ}	0		0		ns	2, 3
OE to Output in High-Z	t_{OEHZ}		5		5	ns	2, 3
SETUP TIMES							
Address	t_{AS}	2.5		2.5		ns	5
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSS}	2.5		2.5		ns	5
Address Advance ($\overline{ADV}$)	t_{AAS}	2.5		2.5		ns	5
Byte Write Enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$), Global Write ($\overline{GW}$), Byte Write Enable ($\overline{BWE}$)	t_{WS}	2.5		2.5		ns	5
Data In	t_{DS}	2.5		2.5		ns	5
Chip Enables ($\overline{CE}$, $\overline{CE_2}$, CE_2)	t_{CES}	2.5		2.5		ns	5
HOLD TIMES							
Address	t_{AH}	0.5		0.5		ns	5
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSH}	0.5		0.5		ns	5
Address Advance ($\overline{ADV}$)	t_{AAH}	0.5		0.5		ns	5
Byte Write Enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$), Global Write ($\overline{GW}$), Byte Write Enable ($\overline{BWE}$)	t_{WH}	0.5		0.5		ns	5
Data In	t_{DH}	0.5		0.5		ns	5
Chip Enables ($\overline{CE}$, $\overline{CE_2}$, CE_2)	t_{CEH}	0.5		0.5		ns	5

NOTES:

1. Test conditions as specified with the output loading as shown in Figure 3 unless otherwise noted.
2. Output loading is specified with CL = 5 pF as in Figure 4. Transition is measured ±500 mV from steady state voltage.
3. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
4. $\overline{OE}$ is a 'don't care' when a byte write enable is sampled LOW.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3.0 V
Input Rise and Fall Times	1.5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 3 and 4

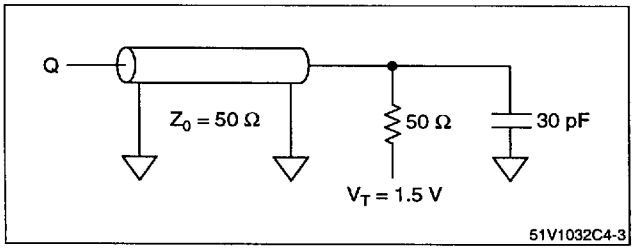


Figure 3. Output Load Equivalent

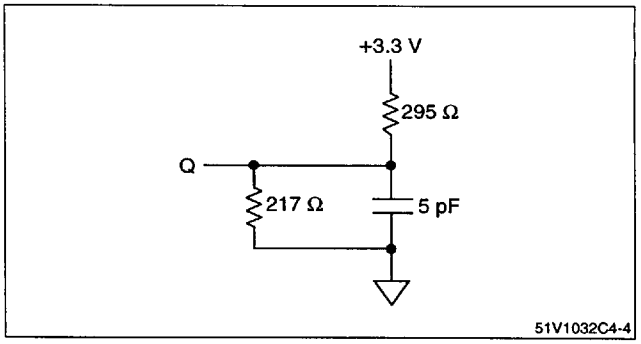
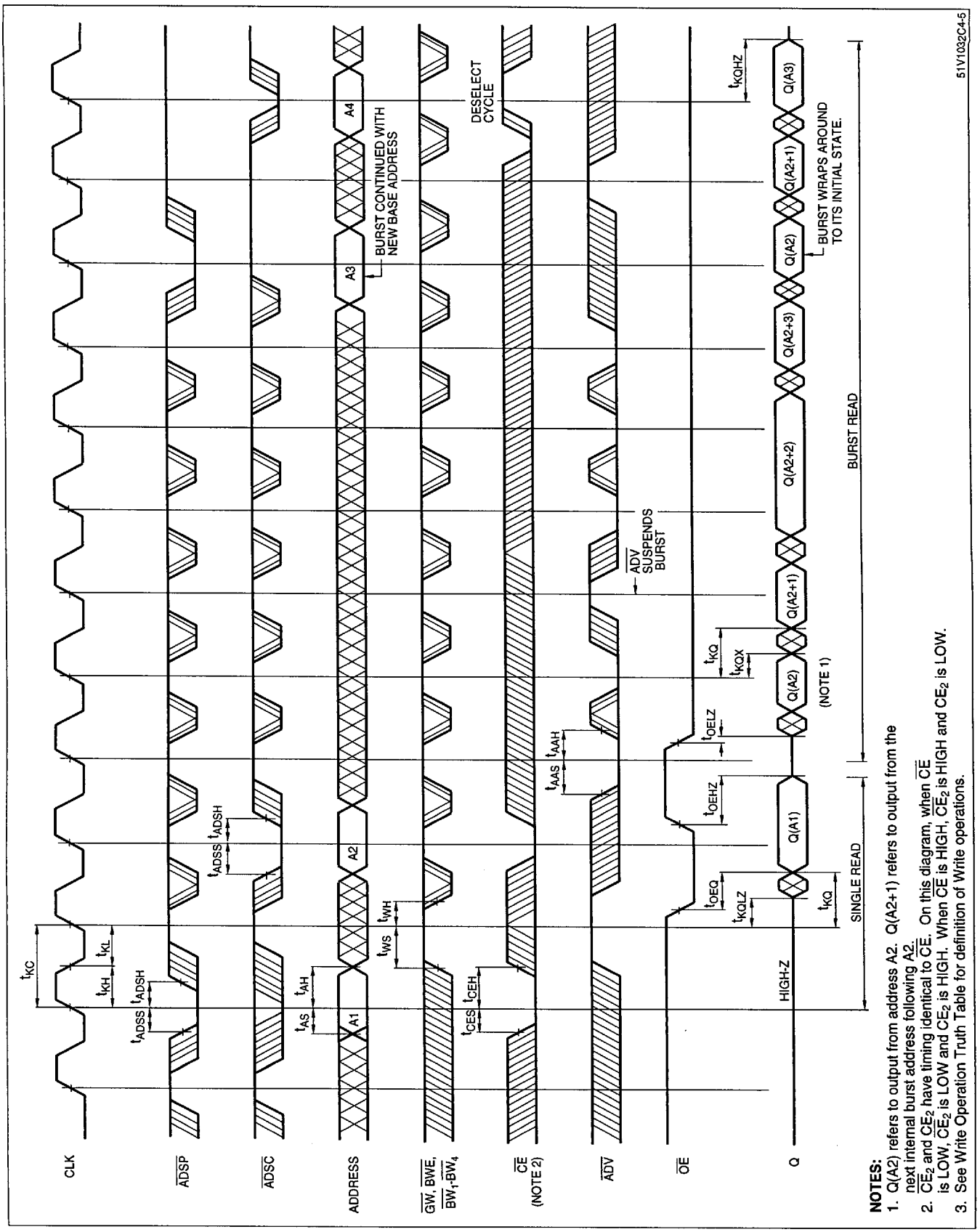
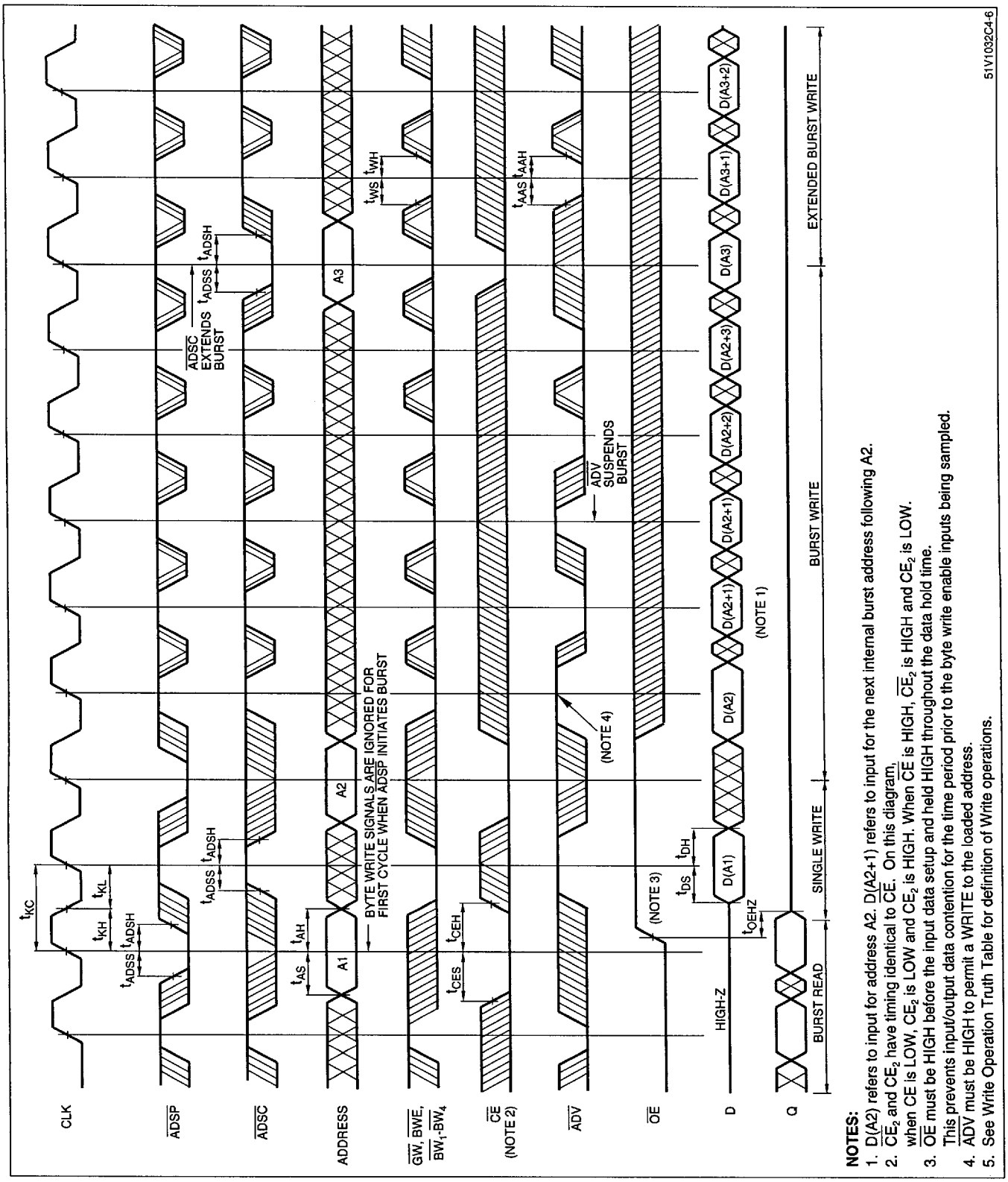


Figure 4. Output Load Equivalent



NOTES:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE}_2$ and $\overline{CE}_2$ have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.
3. See Write Operation Truth Table for definition of Write operations.

Figure 5. Read Timing



NOTES:
1. D(A2) refers to input for address A2. D(A2+1) refers to input for the next internal burst address following A2.
2. $\overline{CE}_2$ and CE_2 have timing identical to $\overline{CE}$. On this diagram, when CE is LOW, CE_2 is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. See Write Operation Truth Table for definition of Write operations.

Figure 6. Write Timing

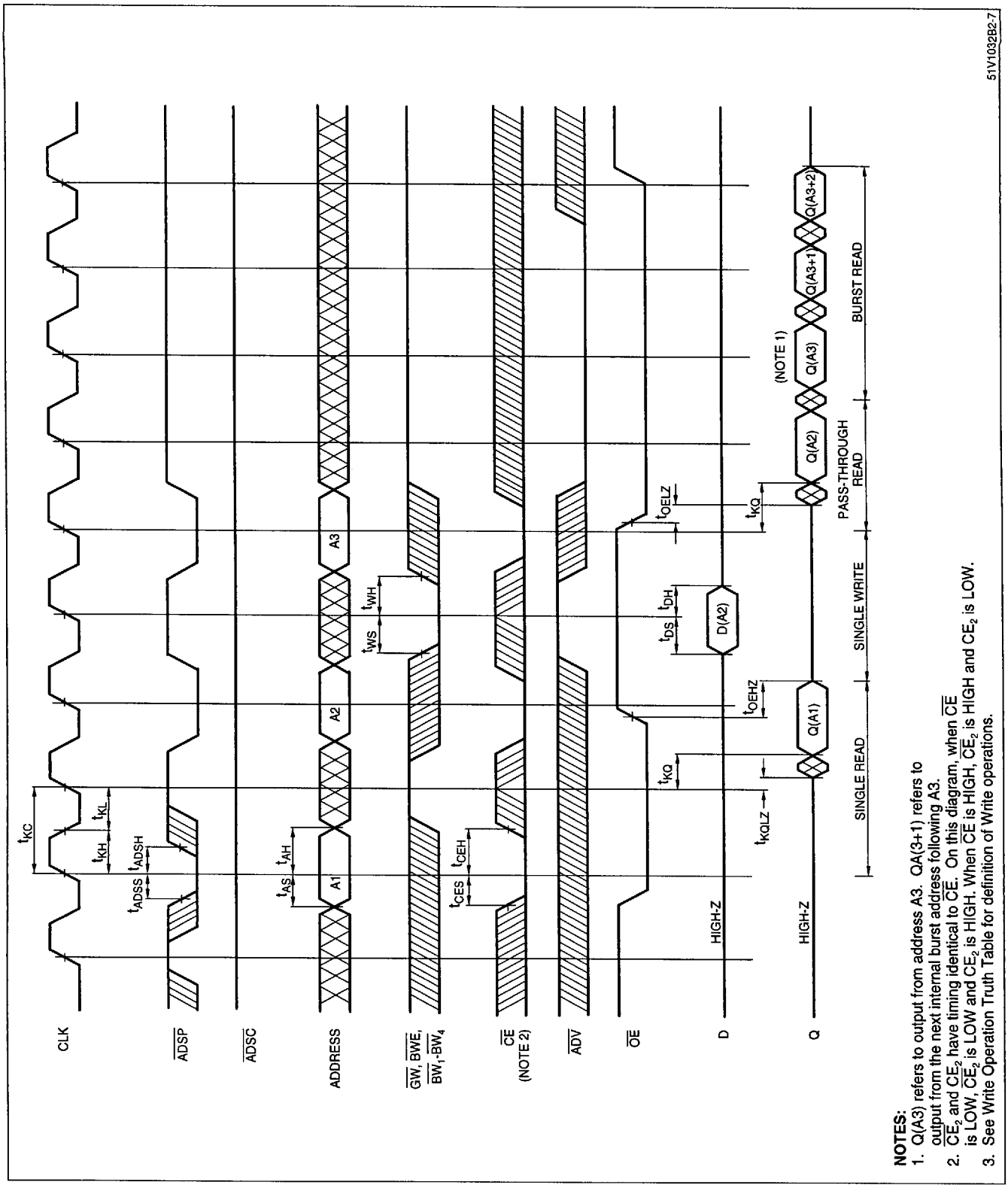


Figure 7. Read/Write Timing

APPLICATION INFORMATION

Load Derating Curves

The Sharp 32K × 32 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30 pF. Access time changes with load capacitance as follows:

$Dt_{KQ} = 0.03$ ns/pF × ΔC_L pF

NOTE: this is preliminary information subject to change.

For example, if the SRAM loading is 22 pF, ΔC_L is −8 pF (8 pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.03 × 8 = 0.24 ns.

Consult the factory for copies of I/O current versus voltage curves and SPICE models.

Depth Expansion

The Sharp 32K × 32 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 8.

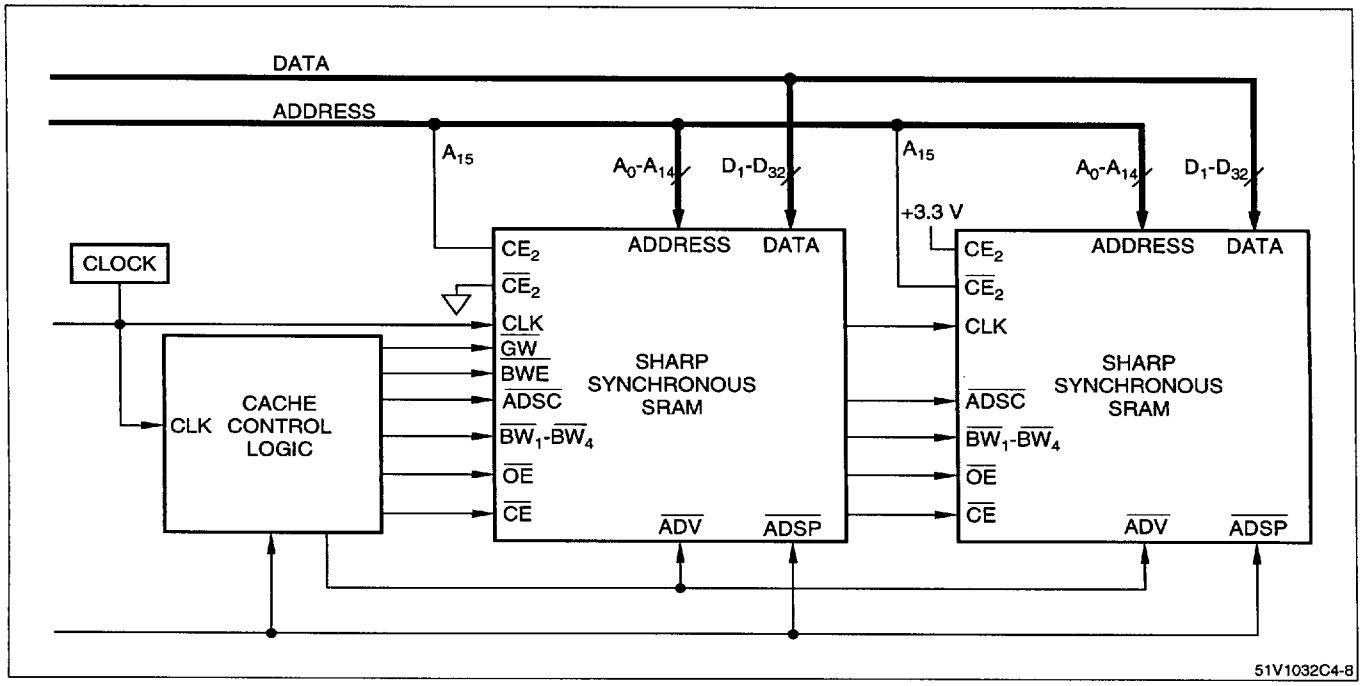


Figure 8. Depth Expansion from 32K x 32 to 64K x 32

APPLICATION EXAMPLES

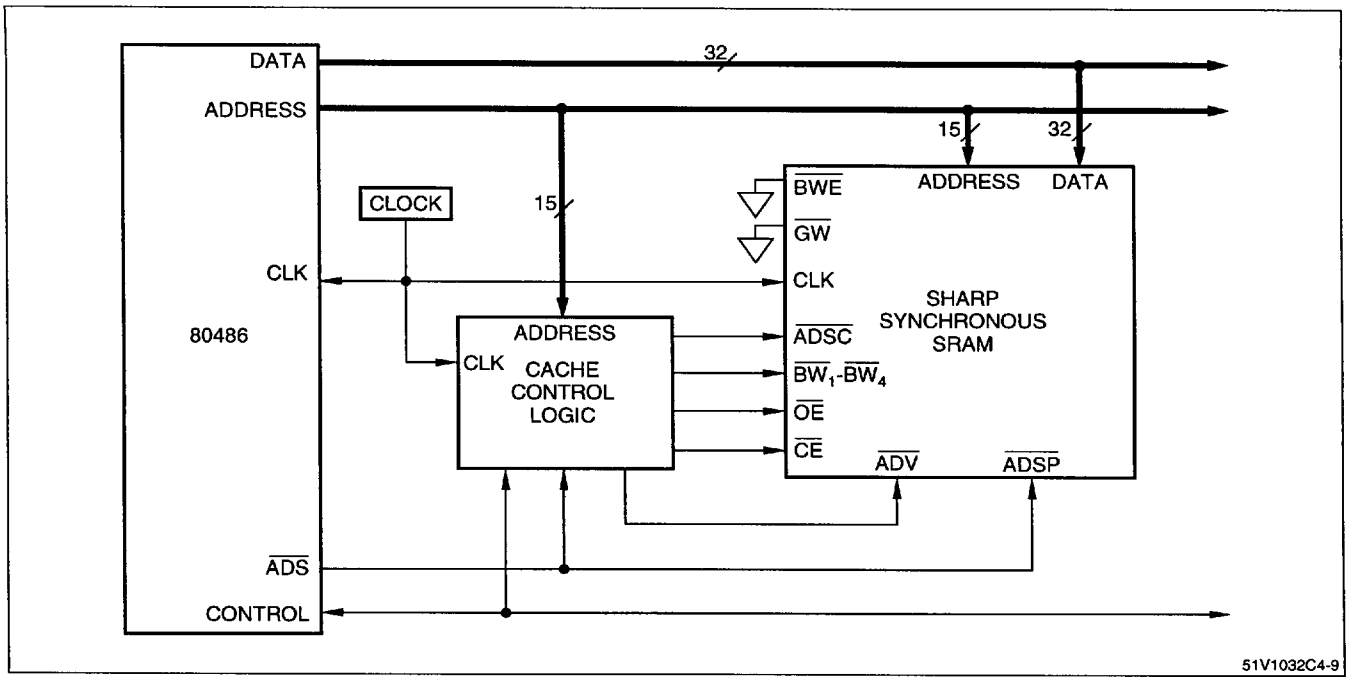


Figure 9. 128K Byte Secondary Burst Mode Cache for 486 Using One LH51V1032 Synchronous SRAM

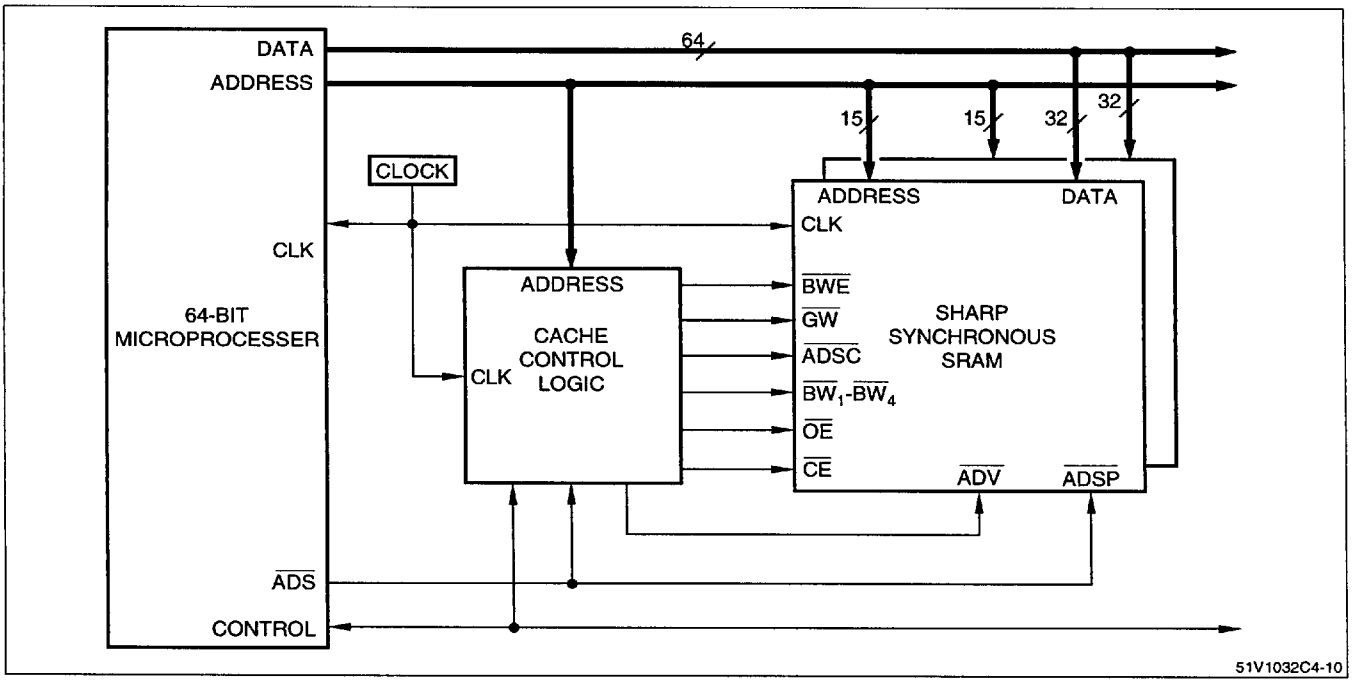
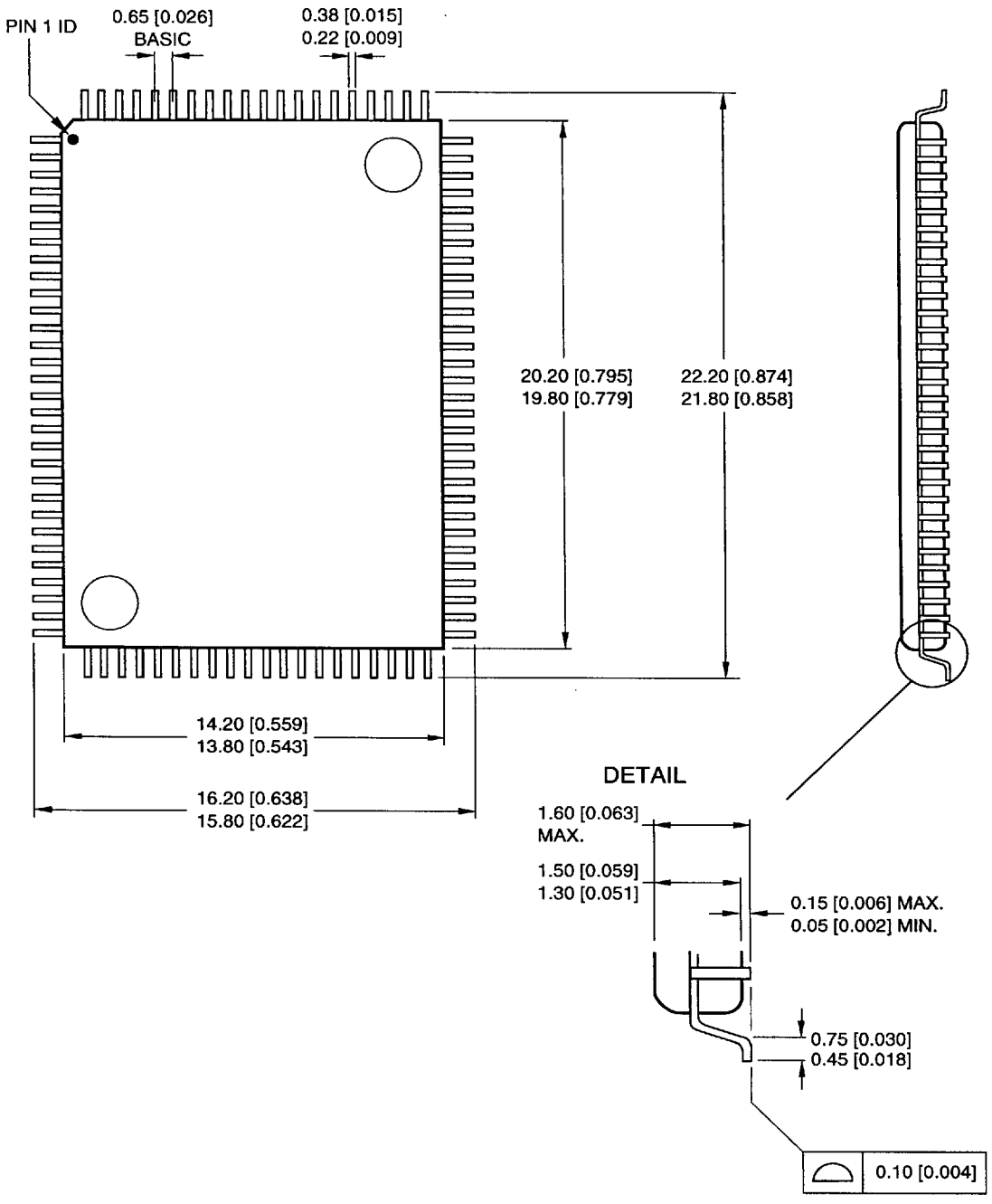


Figure 10. 256K Byte Secondary Burst Mode Cache for Pentium Microprocessor Using Two LH51V1032 Synchronous SRAMs

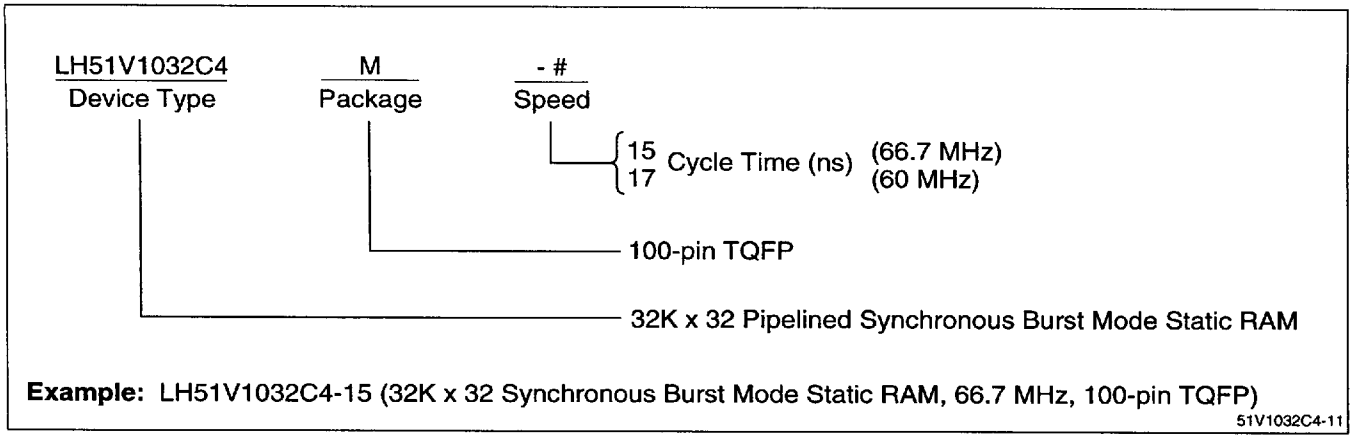
PACKAGE DIAGRAM

100TQFP (TQFP-100-P-1420)



100-pin TQFP

ORDERING INFORMATION



Example: LH51V1032C4-15 (32K x 32 Synchronous Burst Mode Static RAM, 66.7 MHz, 100-pin TQFP)

51V1032C4-11