LH521007A

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 17/20/25 ns
- Two Chip Enable Controls
- Low-Power Standby When Deselected
- TTL Compatible I/O
- 5 V ±10% Supply
- Fully-Static Operation
- 2 V Data Retention
- Package: 32-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521007A is a high-speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enables ($\overline{E}_1$, E_2) permit Read and Write operations when active ($\overline{E}_1$ = LOW and E_2 = HIGH) or place the RAM in a low-power standby mode when inactive ($\overline{E}_1$ = HIGH or E_2 = LOW). Standby power drops to its lowest level when all inputs are stable and are at CMOS levels, while the chip is in standby mode.

Write cycles occur when both Chip Enables and Write Enable are active. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When both Chip Enables are active and $\overline{W}$ is inactive, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

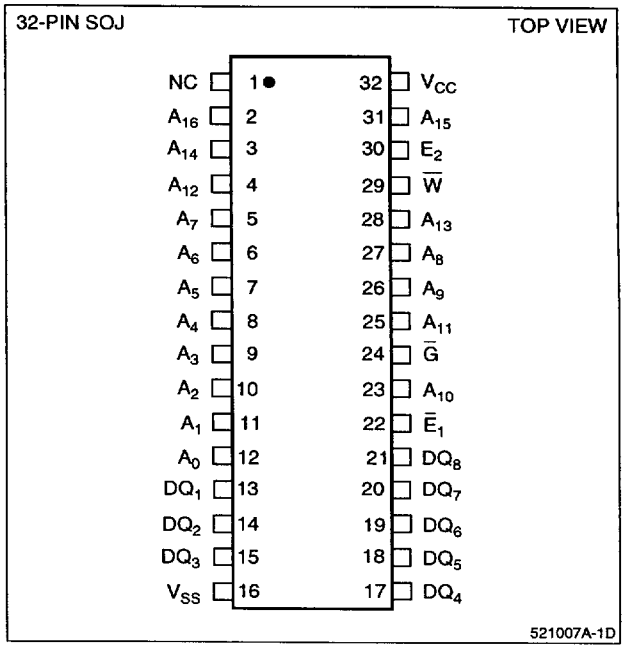


Figure 1. Pin Connections for SOJ Package

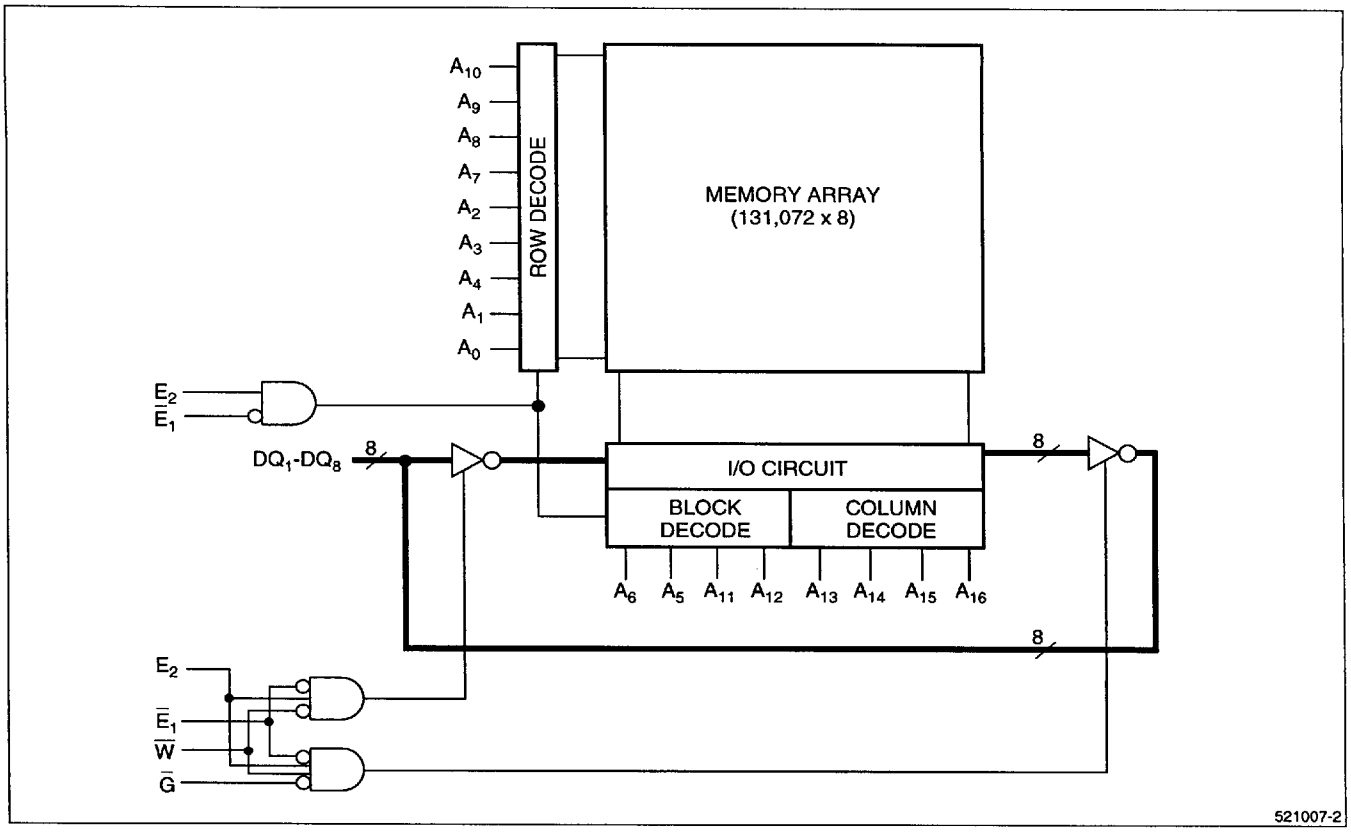


Figure 2. LH521007A Block Diagram

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	X	Standby	High-Z	Standby
X	L	X	X	Standby	High-Z	Standby
L	H	H	H	Read	High-Z	Active
L	H	L	H	Read	Data Out	Active
L	H	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_1 - DQ_8$	Data Inputs/Outputs
$\overline{E}_1$, E_2	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{CYCLE} = 17 ns		115	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 20 ns		105	175	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 25 ns		95	165	mA
I_{SB1}	Standby Current	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$ t_{CYC} = min, I_{OUT} = 0		12	25	mA
I_{SB2}	Standby Current	$\overline{E}_1 \geq V_{CC}$ − 0.2 V or $E_2 \leq$ 0.2 V, t_{CYC} = min, I_{OUT} = 0		0.5	2	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E}_1 \geq V_{CC}$ − 0.2 V and $E_2 \leq$ 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E}_1 \geq V_{CC}$ − 0.2 V and $E_2 \leq$ 0.2 V			500	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

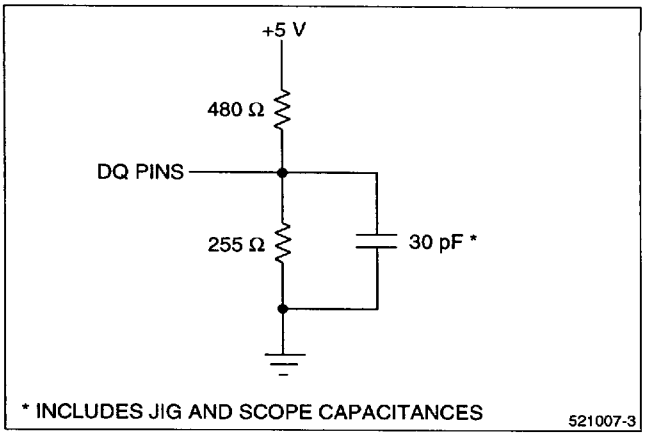


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

For data retention mode, either $\overline{E}_1 \geq V_{CC} - 0.2$ V or $E_2 \leq 0.2$ V. The other control signals must be at valid CMOS levels ($V_{CC} - 0.2$ V ≤ V_{IN} ≤ 0.2 V). The address and data buses are 'Don't Care.'

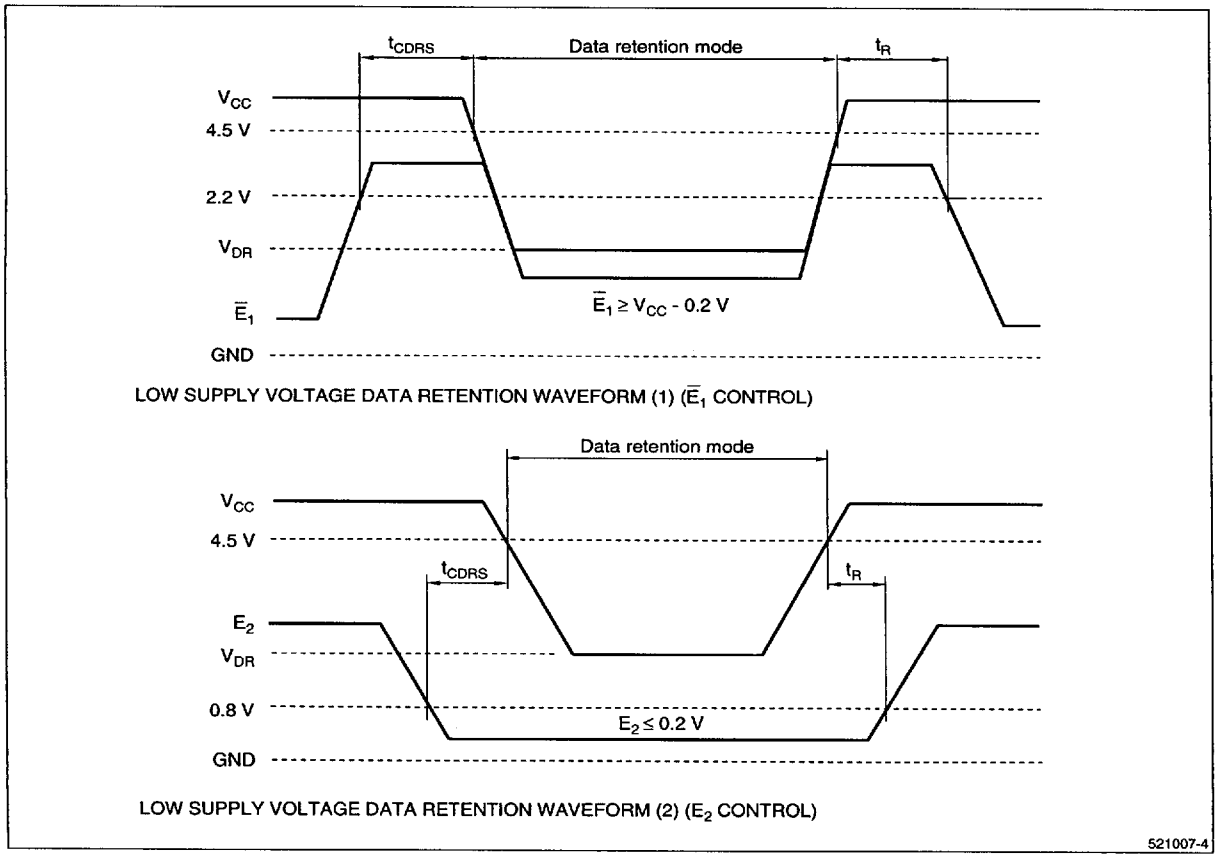


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-17		-20		-25		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	17		20		25		ns
t_{AA}	Address Access Time		17		20		25	ns
t_{OH}	Output Hold from Address Change	3		5		5		ns
t_{EA}	Chip Enable to Valid Data		17		20		25	ns
t_{ELZ}	Chip Enable to Output Active [2,3]	5		5		5		ns
t_{EHZ}	Chip Disable to Output High-Z [2,3]		7		8		10	ns
t_{GA}	$\overline{G}$ Low to Valid Data		6		7		8	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		5		8		10	ns
t_{PU}	Chip Enable to Power Up Time [4]	0		0		0		ns
t_{PD}	Chip Disable to Power Down Time [4]		17		20		25	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	17		20		25		ns
t_{EW}	Chip Enable to End of Write	12		13		15		ns
t_{AW}	Address Valid to End of Write	12		13		15		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		13		15		ns
t_{DW}	Input Data Setup Time	8		9		10		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	7	0	8	0	10	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		5		5		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Sample tested only.
4. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ and E_2 are HIGH, $\overline{E}_1$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}_1$ and E_2 are both active. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

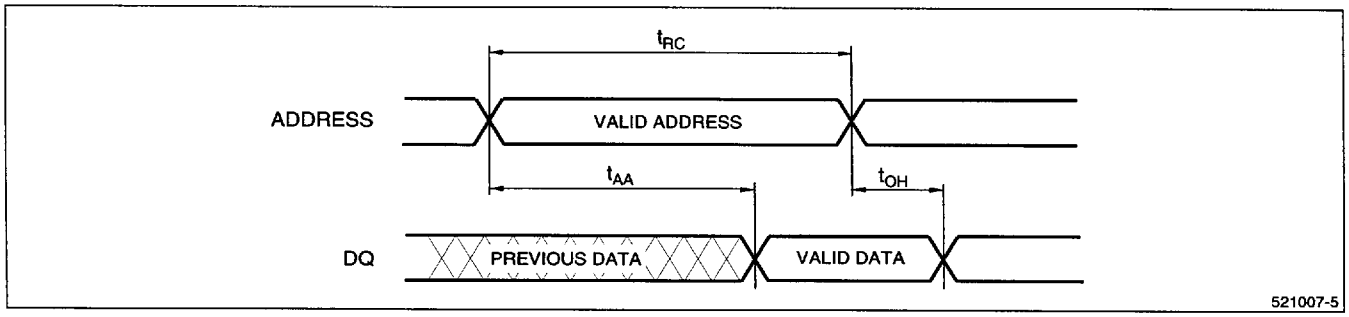


Figure 5. Read Cycle No. 1

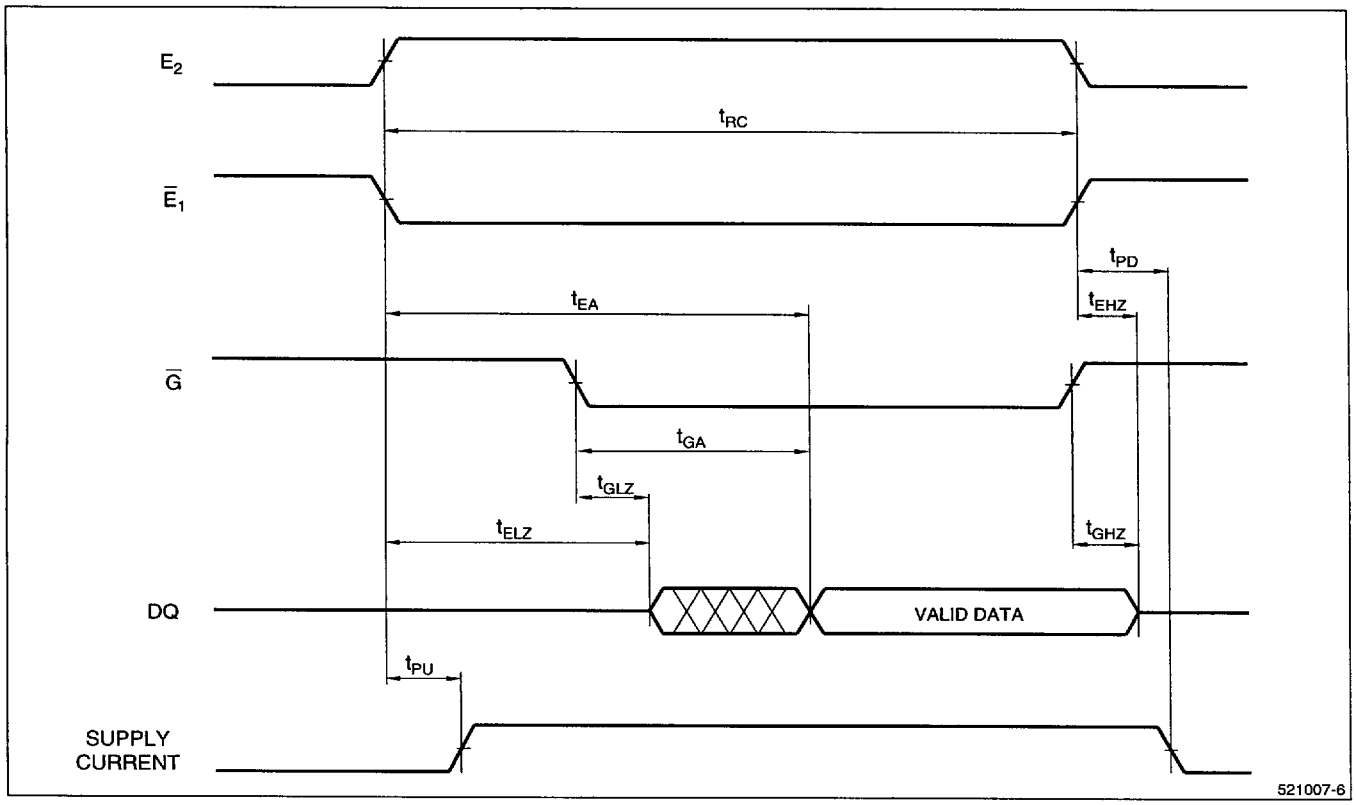


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when both $\overline{E}_1$ and E_2 are active. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}_1$ and $\overline{G}$ are LOW, E_2 is HIGH. Using only $\overline{W}$ to control Write cycles *may not offer the best* performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

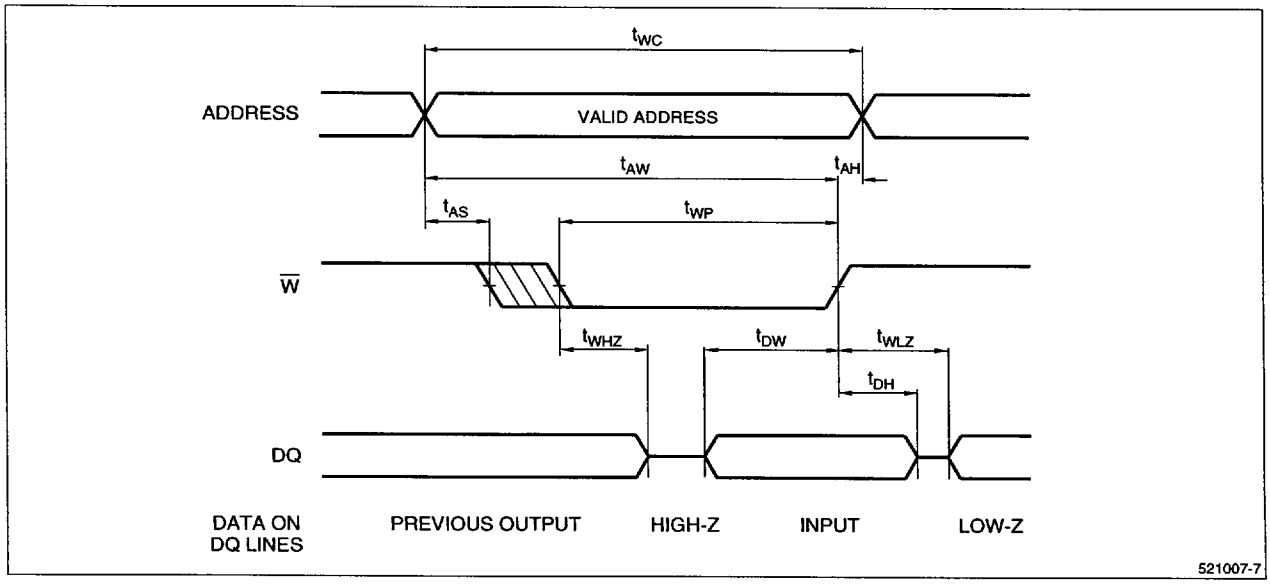


Figure 7. Write Cycle No. 1

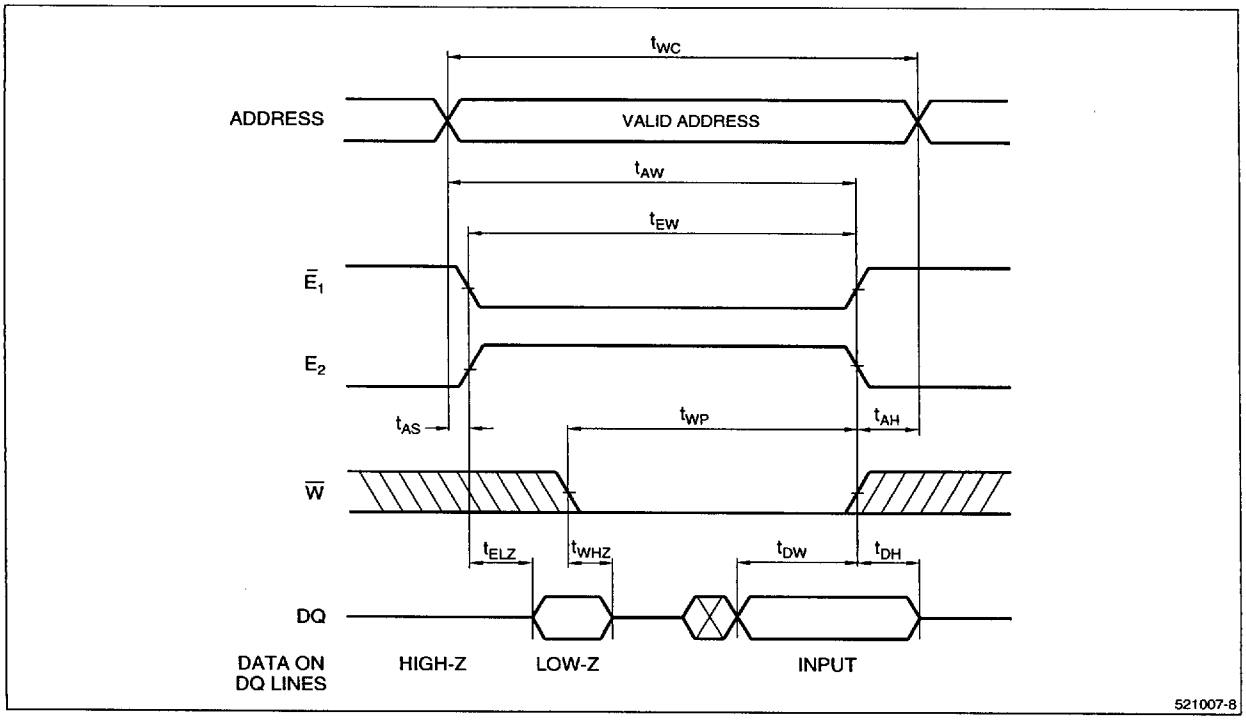
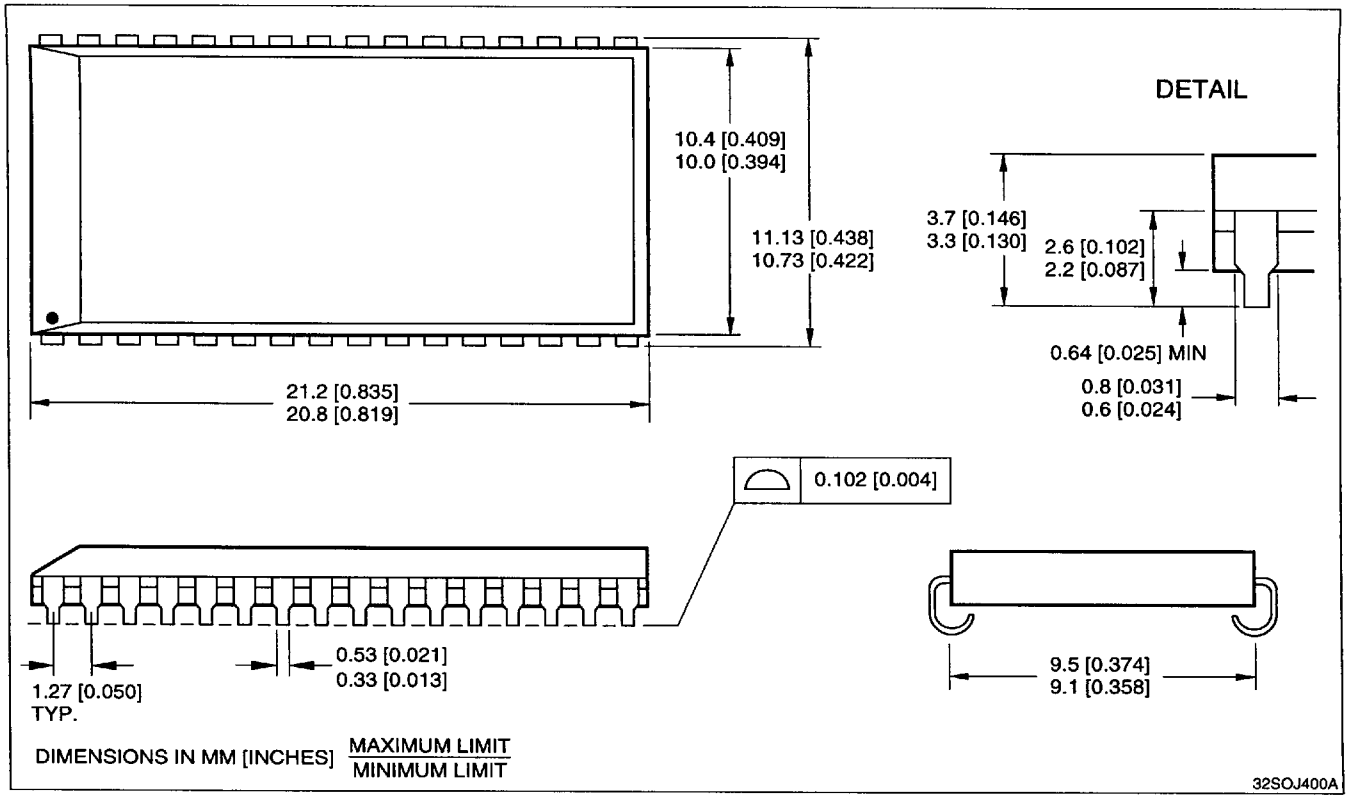


Figure 8. Write Cycle No. 2

PACKAGE DIAGRAM



32-pin, 400-mil SOJ

ORDERING INFORMATION