SIGNAL PROCESSING EXCELLENCE

DAC377-18 SERIES

COMPLETE BUFFERED 18-BIT DAC

T-51-09-90

FEATURES

- True 16-bit (0.0008%) linearity
- Complete with internal reference, input storage registers, output amplifier
- Low power
- Hermetic 28-pin DIP
- Available with MIL-STD-883 screening and testing

DESCRIPTION

The DAC377-18 is a complete 18-bit D/A converter with true 16-bit linearity. Complete with storage registers, internal reference and output amplifier, DAC377-18 provides the user with exceptional performance and self-contained operation. Input storage resisters are in two 8-bit and one 2-bit segments with independent latching — a system compatible with most microprocessor data bus interfaces. A single proprietary[1] monolithic chip contains switches, storage registers and other electronics for high resolution and low linearity error.

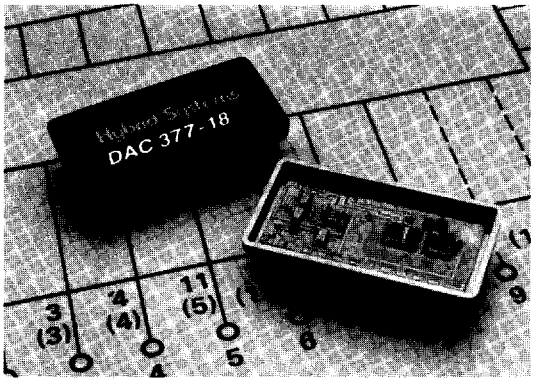
Outstanding features include:

True 16-Bit Linearity — 16-bit (±0.0008%) linearity with 18-bit resolution is unequaled. No other microcircuit converter does better.

Low Power — CMOS proprietary monolithic devices in a unique circuit configuration yield the lowest power dissipation (450 mW typ) of any complete 18-bit converter available.

Complete — No external components are required for 18-bit conversion.

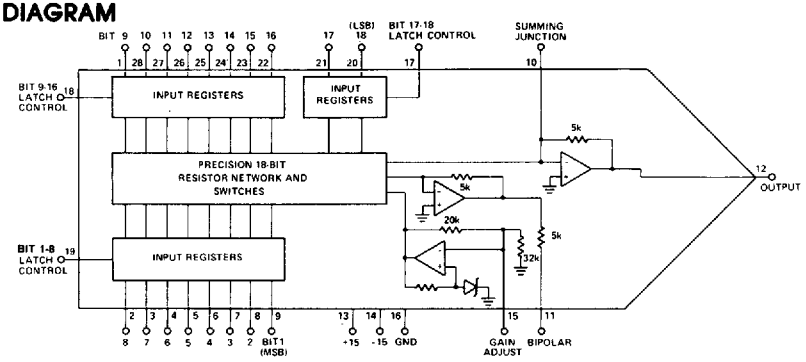
Input Storage Registers — Designed as two 8-bit and one 2-bit segments, the input storage registers provide data storage when latched, but are "transparent" when unlatched, allowing data conversion to be performed continuously or from stored data.



Reliability — Our 28 pin hermetically-sealed package performs reliably in adverse environments. Together with our own proprietary monolithic device and automatic wirebonding, DAC377-18 is one of the most reliable high resolution devices to date. Batch-processed precision thin-film resistor networks fabricated in our own facility are functionally laser-trimmed and glass passivated to assure proven performance in the toughest environments. Continuously monitored during assembly and test, each production lot is screened 100% to assure reliable performance to all specifications. DAC377B-18 models are fully screened and tested to MIL-STD-883 Rev. C, Levels B or S.

Advanced designs, proven processes and continuous monitoring during all production operations by our quality control organization are combined with rigorous AQL screening to provide the most dependable converter possible.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @ +25° C nominal power supply, no load, unless otherwise noted)

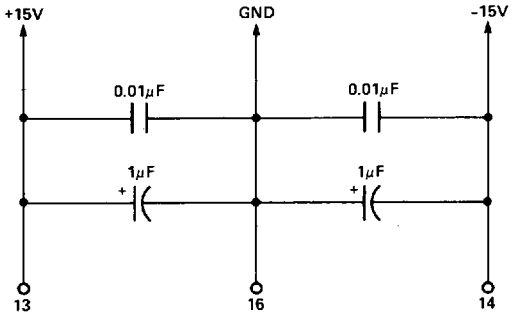
MODEL	DAC377-18
TYPE	Latched Inputs, Voltage Output
DIGITAL INPUT	
Resolution	18-Bits
Unipolar Coding	Binary
Bipolar Coding	Offset Binary
Logic Compatibility[1]	DTL, TTL, CMOS
Input Leakage Current	±1μA (max), 0.4V>V_{LOGIC}>3.2V
Latch Control Width	250nS (min)
Data Set-up Time[2]	500nS (min)
Data Hold Time[3]	0nS (min)
ANALOG OUTPUT	
Scale Factor[4]	±0.15% F.S.R. (max)
Initial Offset[4]	
Unipolar	±0.05% F.S.R. (max)
Bipolar	±0.05% F.S.R. (max)
Voltage Range	
Unipolar	0 to +10V
Bipolar	±10V
Current Compliance	±5 mA
Output Impedance	< 1Ω
Noise	
PP-noise (wideband)	0.0005% F.S.R.
REFERENCE	
Internal[5]	
STATIC PERFORMANCE	
Integral Linearity[6]	±0.0008% F.S.R. (typ) ±0.0015% F.S.R. (max)
Differential Linearity[7]	±0.0004% F.S.R. (typ) ±0.0015% F.S.R. (max)
Monotonicity	Guaranteed to 16-bits
DYNAMIC PERFORMANCE	
Major Code Transition Settling to 0.006% F.S.R. (strobed)	20μS
Slew Rate	0.20 v/μS
STABILITY (Over Specified Temp. Range)	
Scale Factor	2ppm/°C F.S.R. (typ), 8ppm/°C (max)
Linearity	1ppm/°C F.S.R. (max)
Differential Linearity	1ppm/°C F.S.R. (max)
Linearity	±0.0115% max @ +125°C ±0.095% max @ −55°C
Differential Linearity	±0.0115% max @ +125°C ±0.095% max @ −55°C
Offset Drift	
Unipolar	1ppm/°C F.S.R.
Bipolar	5ppm/°C F.S.R.
POWER SUPPLY	
Requirements	+15V ±5% @ 15mA (max) −15V ±5% @ 25mA (max)
Rejection Ratio	0.001%/%
Power Dissipation	400mW (typ), 600mW (max)
TEMPERATURE RANGE	
Operating - B option	−55°C to +125°C
Operating - C option	0°C to +70°C
Storage	−65° to +150°C
MECHANICAL	
Case Style	28-pin hermetic double-DIP

NOTES:
1. Digital Input voltage must not exceed supply voltage, or go below −0.5V. "0"<0.8 volts, "1">2.4 volts.
2. Time, data must be stable after Latch Control goes to "1".
3. Time, data must be stable after Latch Control goes to "0".
4. See APPLICATIONS INFORMATION for calibration procedure.
5. See APPLICATION NOTES.
6. Integral Linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
7. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.

CAUTION:
UNUSED INPUTS MUST BE GROUNDED!

APPLICATIONS INFORMATION

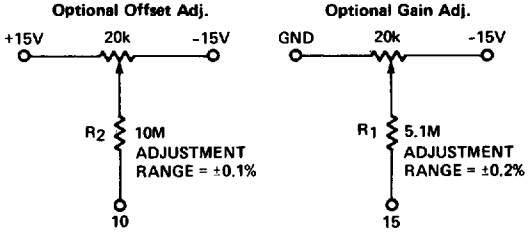
RECOMMENDED BYPASS CIRCUIT



PIN CONNECTIONS

1. UNIPOLAR OUTPUT: Ground pin 11
   BIPOLAR OUTPUT: Connect pin 11 to pin 10
2. Unused bit pins should be grounded. If bits 17 and 18 are not used, the latch control (pin 17) must be tied to either +5V or to +15V.

OPTIONAL GAIN & OFFSET ADJUSTMENT CIRCUIT



Values of R_1 & R_2 can be changed to increase or decrease the sensitivity of the adjustment. This adjustment should not be greater than ±1% around the nominal value for best performance.

CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment

Unipolar operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for F.S. -1 LSB.

Bipolar operation:
1. Apply a 100 . . . 0 input code and set the OFFSET ADJ pot for 0V output
2. Apply a 000 . . . 0 input code and set the GAIN ADJ pot for -F.S.

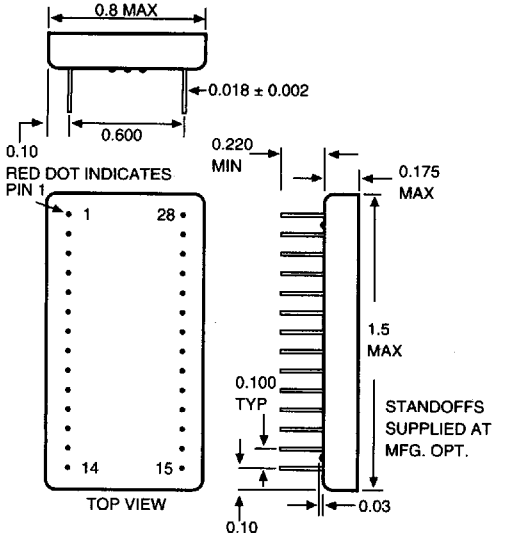
TRANSFER CHARACTERISTICS

Unipolar Operation

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. − 1 LSB
100...000	+F.S./2
011...111	+F.S./2 − 1 LSB
000...000	0V

Bipolar Operation

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. − 1 LSB
100...000	0V
011...111	− 1 LSB
000...000	−F.S.

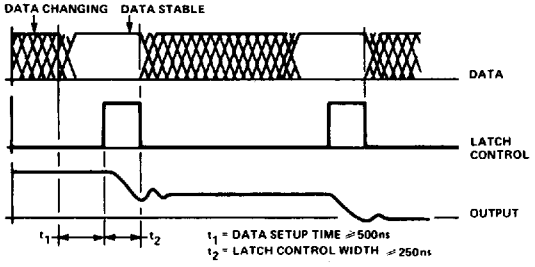


PIN	FUNCTION	PIN	FUNCTION
1	BIT 9	28	BIT 10
2	BIT 8	27	BIT 11
3	BIT 7	26	BIT 12
4	BIT 6	25	BIT 13
5	BIT 5	24	BIT 14
6	BIT 4	23	BIT 15
7	BIT 3	22	BIT 16
8	BIT 2	21	BIT 17
9	BIT 1, MSB	20	BIT 18, LSB
10	SUMMING JCT	19	2^{-1}-2^{-8} LATCH
11	BIPOLAR	18	2^{-9}-2^{-16} LATCH
12	OUTPUT	17	2^{-17}-2^{-18} LATCH
13	+15	16	GND
14	−15	15	GAIN ADJUST

TIMING DIAGRAM

LATCH CONTROL

Latch Strobe Input	Function
0	data latched (held)
1	data changing (transfer)



When loading the DAC from an 8-bit computer bus, optimum dynamic response will be obtained when the MSB segment is loaded first, followed by the LSB segments. This sequence allows the MSB's to settle while loading the LSB's.

Note that this loading sequence is necessary only when the processor cycle time is longer than the DAC settling time. If the processor cycle time is shorter than the DAC settling time, the bits may be loaded in any sequence.

APPLICATION NOTES

INTERNAL REFERENCE (NOTE 4)

Buffered bootstrap design of the reference voltage is totally internal. A temperature compensated -6.2 volt planar-zener diode minimizes temperature drift. The voltage can be monitored with a high impedance digital voltmeter at pin 15 (GAIN ADJUST).

OUTPUT NOISE

Noticeable amounts of noise at both low and high input levels can be prevented through output noise filtering. Care must be taken in choosing an output filter network that will not slow down the operating speed beyond what is desired.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, DAC377-18 should be allowed sufficient warmup time (5 min).
2. Due to the small bit weight (38μV), noise becomes a noticeable factor; if sockets are used, gold-plated ones are recommended to minimize contact resistance.
3. When changing output/gain range, a resistor (connected between pins 10 and 12) with a temperature coefficient between 0 and 10 ppm/°C is required to keep the DAC377-18 within guaranteed specifications.
4. Power supplies should come up before, or at the same time as the digital input supply.

SETTLING TIME

The DAC377-18 incorporates input buffering circuits whose propagation time introduces a skewing of the digital data reaching the bit switches. The skewing results in the bit switches not operating synchronously with each data change, producing an increase in the settling time (1 to 2 microseconds) and large "glitches". The dynamic performance of the DAC377-18 can be greatly improved by using the internal latches which are available on these units. The latches are located after the input buffer circuits and just before the bit switches. When correctly strobed the latches present a data change to the bit switches in a synchronous manner. The latches should be closed while the input data is changing and propagating through the buffers. After the digital data has settled the latch is loaded and the "new" data is transfered to the switches snychronously. The latch is then closed and is ready for the next data update.

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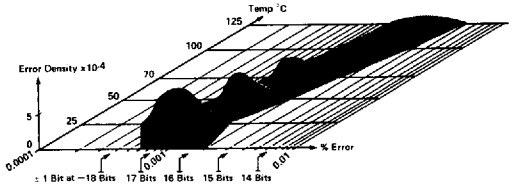
LINEARITY VS TEMPERATURE

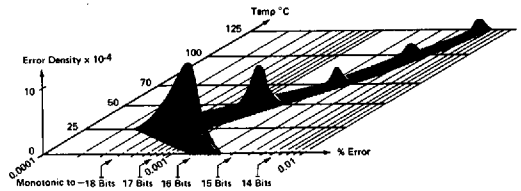
The plots below show the distribution of the maximum error of a unit in a typical lot of DAC377-18's.

INTEGRAL



Integral Linearity is a measurement of the deviation of the DAC377-18 transfer function from a straight line through the end points. It is expressed in the number of bits as well as the percent error.

DIFFERENTIAL



Differential Linearity is a measurement of the maximum deviation of any one LSB step change in the transfer function of the DAC377-18 from its ideal weight (38μV). It is expressed in terms of the number of bits as well as the percent error.

LONGTERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 2.5μV for the first 1000 hrs and 1μV per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain adjustment circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm/1000 hrs.

IMPORTANT NOTICE TO THE USER: When measuring the stability of the DAC377-18, care should be taken so that the drift of the measurement instruments can be separated from the drift factors mentioned above, and the measurements are taken at identical temperatures.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC377B-18	18-Bit Complete DAC, MIL-STD-883 Screening
DAC377C-18	18-Bit Complete DAC, Commercial

Specifications subject to change without notice.