

LH52256AV

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times (MAX.):
 - 200 ns ($2.7 \leq V_{CC} < 3.0$ V)
 - 150 ns ($3.0 \text{ V} \leq V_{CC} \leq 5.5$ V)
- Supply current:
 - Operating: 165 mW (MAX.)
 - Standby: 220 μ W (MAX.)
 - Data retention:
 - 3 μ W ($V_{CCDR} = 3$ V, $t_A = 25^\circ\text{C}$)
- Wide operating voltage range:
 - 2.7 V to 5.5 V
- Fully-static operation
- Three-state outputs
- Packages:
 - 28-pin, 450-mil SOP
 - 28-pin, 8×13 mm² TSOP (Type I)

DESCRIPTION

The LH52256AV is a static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

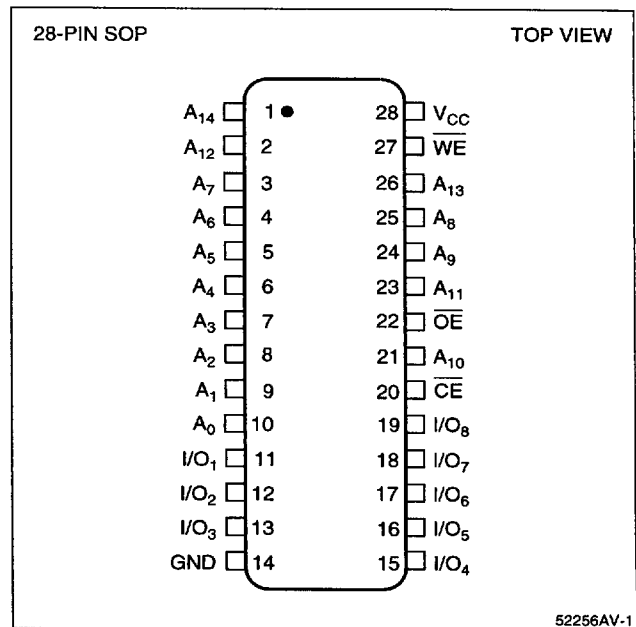


Figure 1. Pin Connections for SOP Package

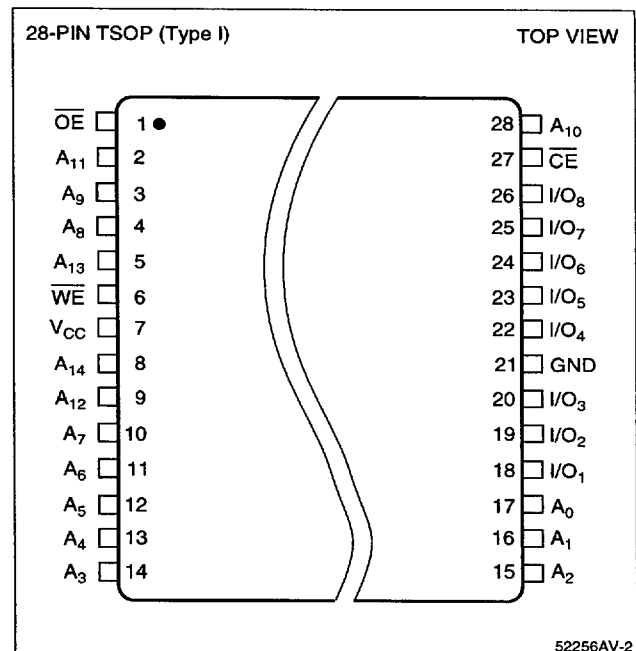


Figure 2. Pin Connections for TSOP Package

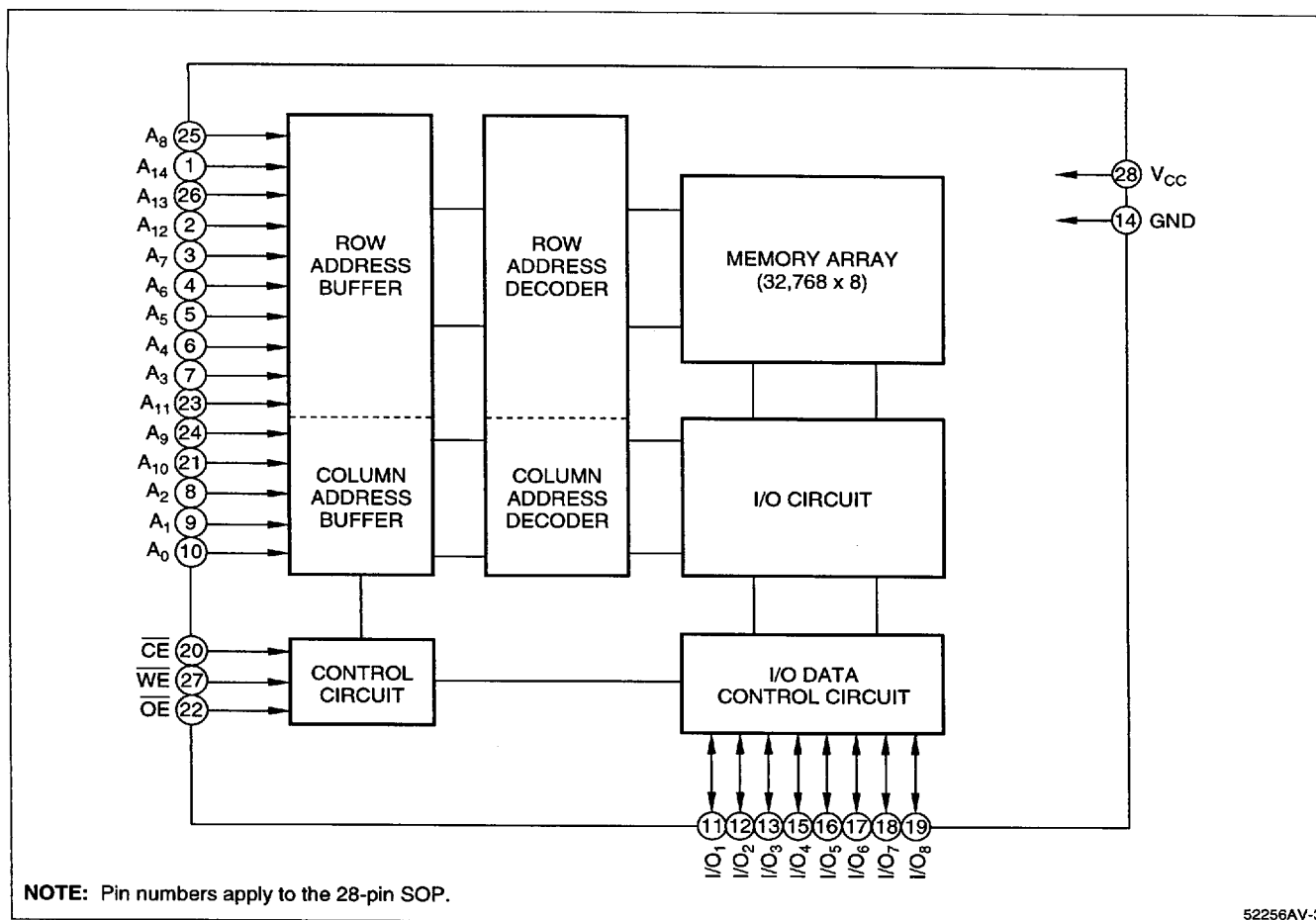


Figure 3. LH52256AV Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₄	Address inputs
$\overline{\text{CE}}$	Chip Enable input
$\overline{\text{WE}}$	Write Enable input
$\overline{\text{OE}}$	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data inputs and outputs
V _{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
H	X	X	Standby	High-Z	Standby (I _{SB})	1
L	L	X	Write	D _{IN}	Operating (I _{CC})	1
L	H	L	Read	D _{OUT}	Operating (I _{CC})	
L	H	H	Output disable	High-Z	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V	1, 2
Operating temperature	T _{opr}	-10 to +70	°C	
Storage temperature	T _{stg}	-65 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = -3.0 V for pulse width ≤ 50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -10°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{CC}	2.7		5.5	V	
Input voltage (V _{CC} = 2.7 V to 5.5 V)	V _{IH}	V _{CC} - 0.3		V _{CC} + 0.3	V	
	V _{IL}	-0.3		0.2	V	1
Input voltage (V _{CC} = 3.0 V to 3.6 V)	V _{IH}	2.0		V _{CC} + 0.3	V	
	V _{IL}	-0.3		0.6	V	1

NOTE:

1. V_{IN} (MIN.) = -3.0 V for pulse width ≤ 50 ns.

DC CHARACTERISTICS ($V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $T_A = -10^\circ\text{C to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = 0\text{ V to }V_{CC}$	-1.0	1.0	μA
Output leakage current	I_{LO}	$\overline{CE} = V_{IH}$ or $OE = V_{IH}$ $V_{IO} = 0\text{ V to }V_{CC}$	-1.0	1.0	μA
Operating supply current	I_{CC}	Minimum cycle, $V_{IN} = V_{IL}$ or V_{IH} $I_{IO} = 0\text{ mA}$, $CE = V_{IL}$		30	mA
		$t_{RC}, t_{WC} = 1.0\text{ }\mu\text{s}$, $V_{IN} = V_{IL}$ or V_{IH} , $I_{IO} = 0\text{ mA}$, $CE = V_{IL}$		10	
		Minimum cycle, $V_{IN} = V_{IL}$ or V_{IH} $I_{IO} = 0\text{ mA}$, $CE = V_{IL}$, $V_{CC} = 3.6\text{ V}$		15	
		$t_{RC}, t_{WC} = 1.0\text{ }\mu\text{s}$, $V_{IN} = V_{IL}$ or V_{IH} , $I_{IO} = 0\text{ mA}$, $CE = V_{IL}$, $V_{CC} = 3.6\text{ V}$		5.0	
Standby supply current	I_{SB}	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$		40	μA
	I_{SB1}	$\overline{CE} = V_{IH}$		3.0	mA
Output voltage	V_{OL}	$I_{OL} = 0.5\text{ mA}$		0.5	V
		$I_{OL} = 2.1\text{ mA}$, $V_{CC} = 3.0\text{ V to }5.5\text{ V}$		0.4	
	V_{OH}	$I_{OH} = -0.5\text{ mA}$	$V_{CC} - 0.5$		V
		$I_{OH} = -1.0\text{ mA}$, $V_{CC} = 3.0\text{ V to }5.5\text{ V}$	2.4		

READ CYCLE ($T_A = -10^\circ\text{C to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	$2.7\text{ V} \leq V_{CC} < 3.0\text{ V}$		$3.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	200		150		ns	
Address access time	t_{AA}		200		150	ns	
Chip enable access time	t_{ACE}		200		150	ns	
Output enable access time	t_{OE}		100		70	ns	
Output hold time	t_{OH}	10		10		ns	
CE Low to output in Low-Z	t_{LZ}	10		10		ns	1
OE Low to output in Low-Z	t_{OLZ}	10		10		ns	1
CE High to output in High-Z	t_{HZ}	0	60	0	60	ns	1
OE High to output in High-Z	t_{OHZ}	0	60	0	60	ns	1

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 200\text{ mV}$ transition from steady state levels into the test load.

WRITE CYCLE ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	$2.7\text{ V} \leq V_{CC} < 3.0\text{ V}$		$3.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	200		150		ns	
CE Low to end of write	t_{CW}	120		100		ns	
Address valid to end of write	t_{AW}	120		100		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	100		70		ns	
Write recovery time	t_{WR}	0		0		ns	
Input data setup time	t_{DW}	60		50		ns	
Input data hold time	t_{DH}	0		0		ns	
WE High to output in Low-Z	t_{OW}	10		10		ns	1
WE Low to output in High-Z	t_{WZ}	0	60	0	60	ns	1
OE High to output in High-Z	t_{OHZ}	0	60	0	60	ns	1

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 200\text{ mV}$ transition from steady state levels into the test load.

TEST CONDITIONS

PARAMETER	MODE	NOTE
Input pulse levels	0 V to V_{CC}	
Input rise/fall times	10 ns	
Input/output timing levels	1.5 V	
Output load	C_L (100 pF)	1

NOTE:

- Includes scope and jig capacitance.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			7	pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF	1

NOTE:

- This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$CE \geq V_{CCDR} - 0.2\text{ V}$	2.0	5.5	V	
Data retention supply current	I_{CCDR}	$V_{CCDR} = 3.0\text{ V}$ $CE \geq V_{CCDR} - 0.2\text{ V}$		1	μA	
				3	μA	
				20	μA	
Chip enable setup time	t_{CDR}		0		ns	
Chip enable hold time	t_R		t_{RC}		ns	1

NOTE:

1. t_{RC} = Read cycle time.

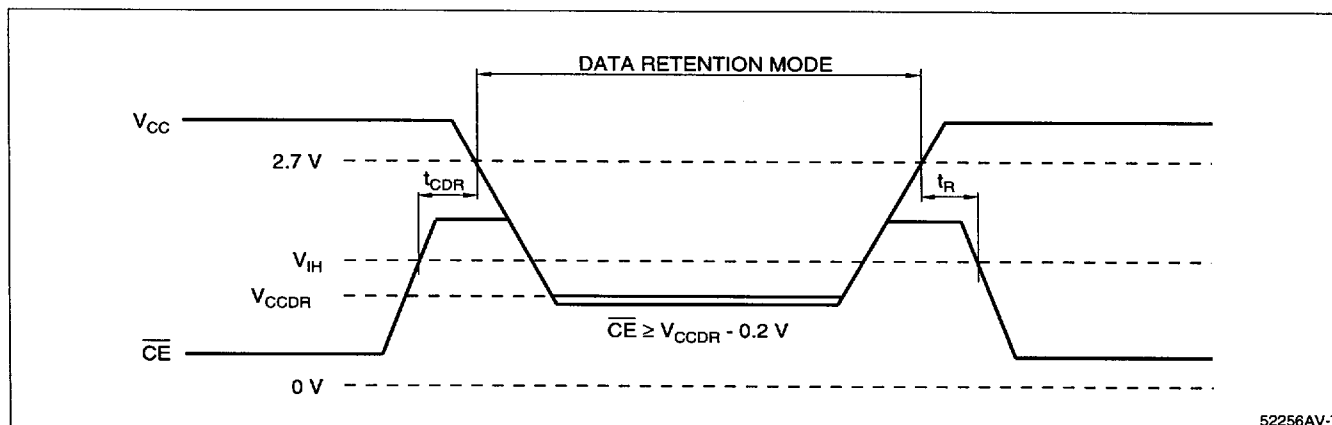
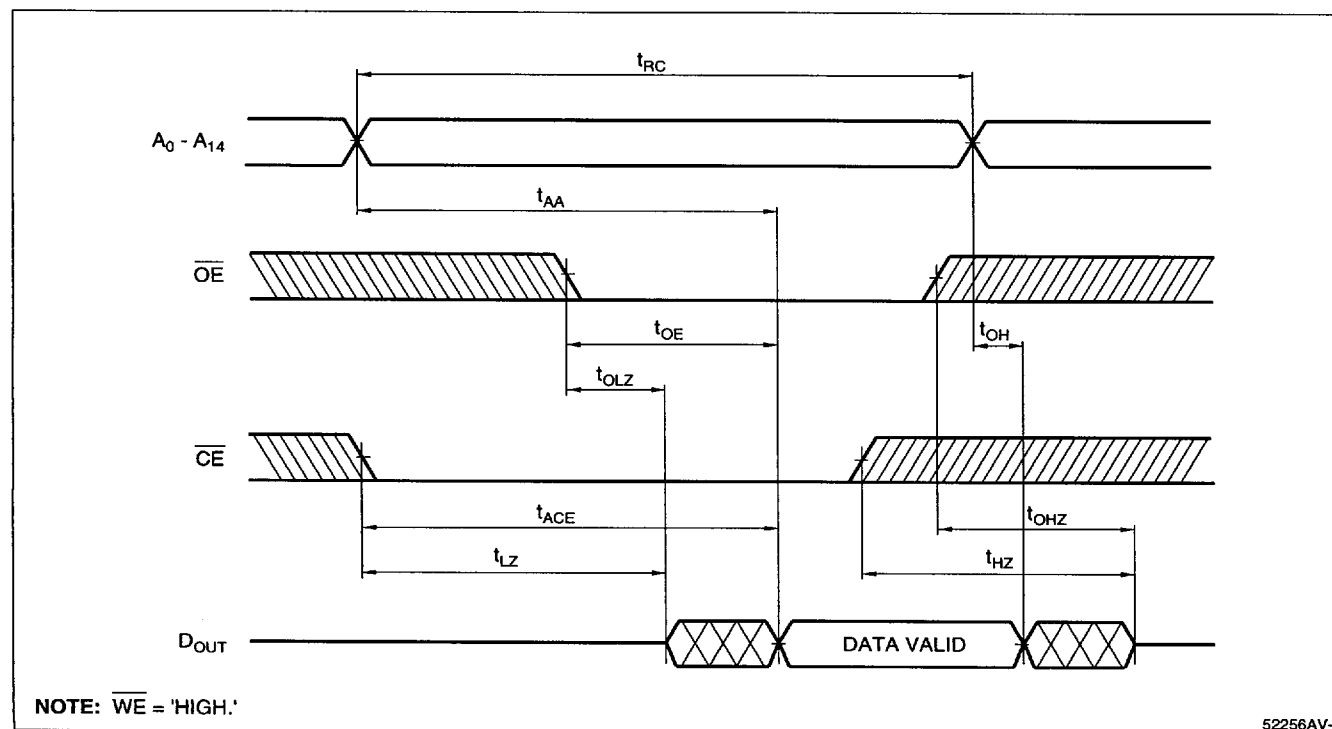
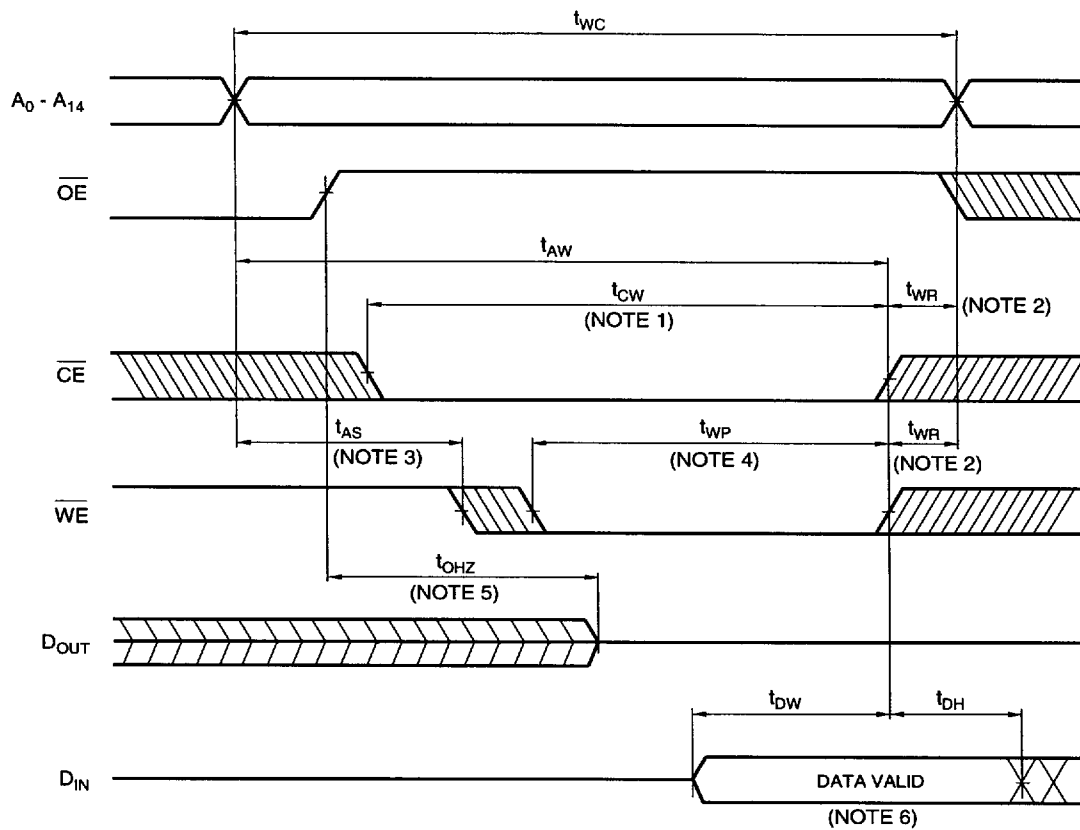


Figure 4. Low Voltage Data Retention



NOTE: WE = 'HIGH.'

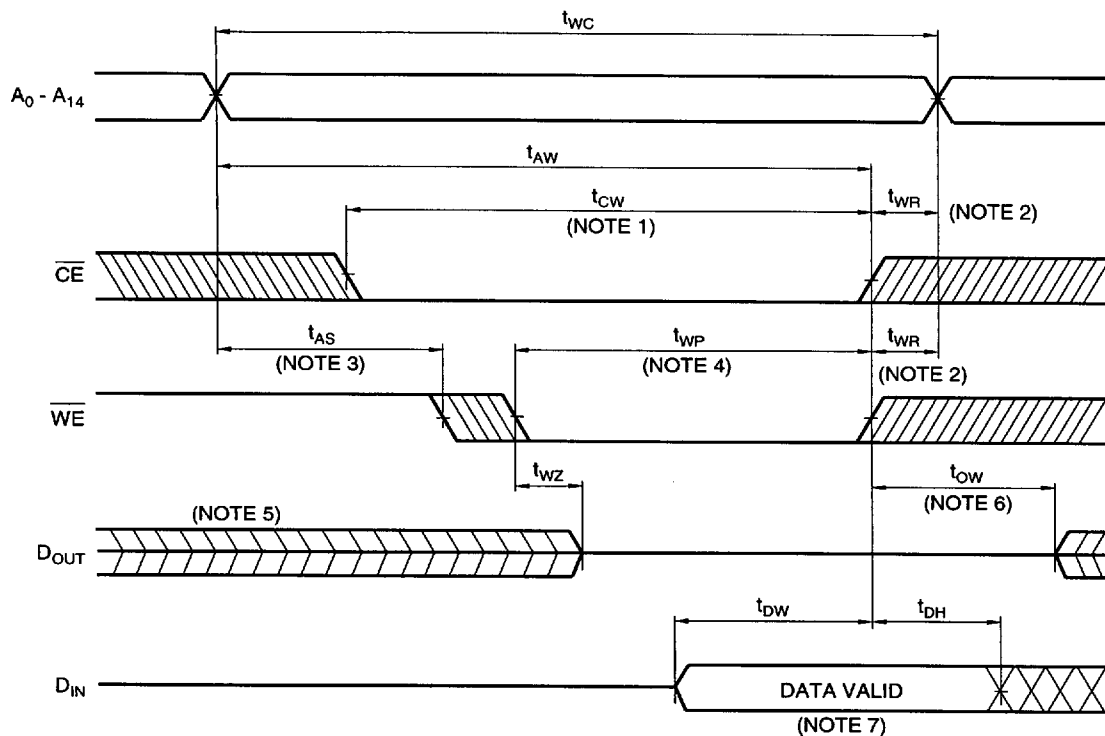
Figure 5. Read Cycle

**NOTES:**

1. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
2. t_{WR} is defined as the time from the end of writing to address change.
3. t_{AS} is defined as the time from address change to the start of writing.
4. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW' and $\overline{WE}$ = 'LOW' (t_{WP}).
5. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 6. Write Cycle ($\overline{OE}$ Controlled)

**NOTES:**

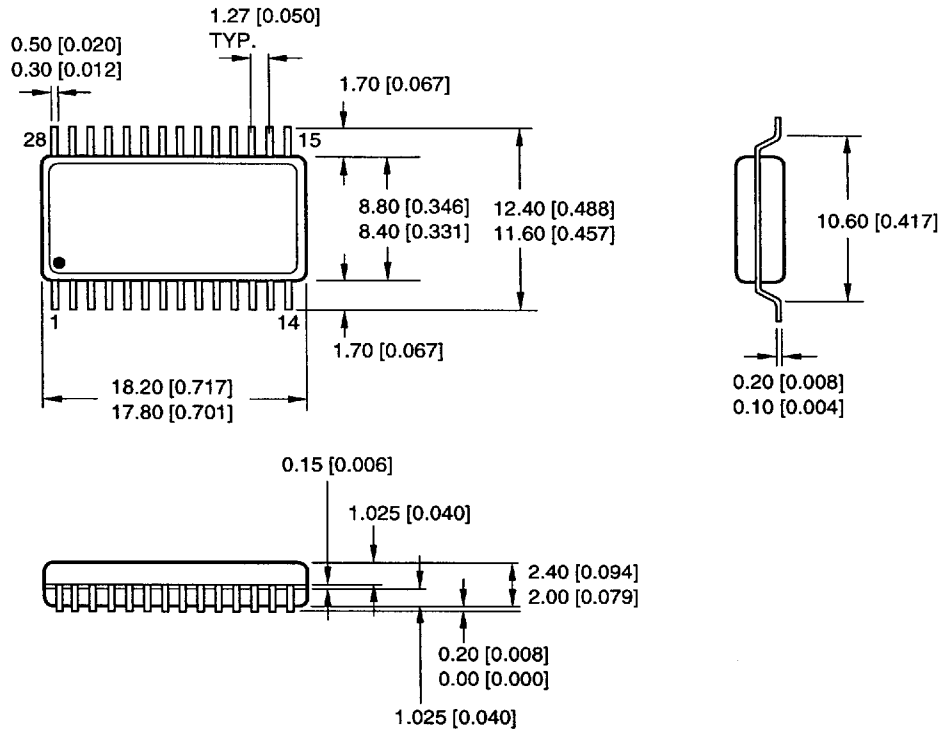
1. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
2. t_{WR} is defined as the time from the end of writing to address change.
3. t_{AS} is defined as the time from address change to the start of writing.
4. The writing occurs during an overlapping period of $\overline{CE} = \text{'LOW'}$ and $\overline{WE} = \text{'LOW'}$ (t_{WP}).
5. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. If $\overline{CE}$ HIGH transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 7. Write Cycle ($\overline{OE}$ Low Fixed)

PACKAGE DIAGRAMS

28SOP (SOP028-P-0450)

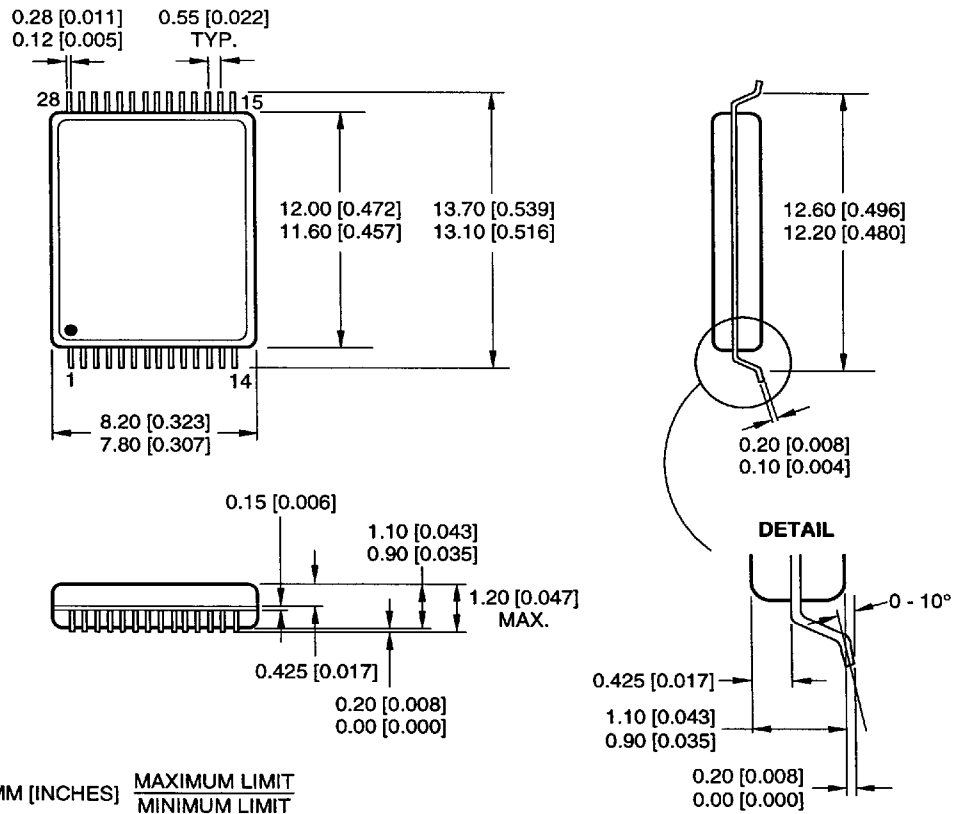


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

28SOP

28-pin, 450-mil SOP

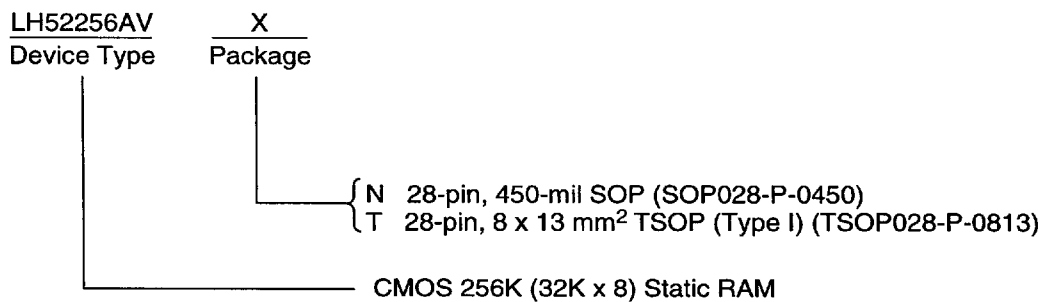
28TSOP (TSOP028-P-0813)



28TSOP

28-pin, 8 × 13 mm² TSOP (Type I)

ORDERING INFORMATION



Example: LH52256AVN (CMOS 256K (32K x 8) Static RAM, 28-pin, 450-mil SOP)

52256AV-8

SHARP

■ 8180798 0015696 990 ■

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