

T-46-23-13

LH52256LL

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time:
90 ns (MAX.)
- Low power consumption:
Operating: 385 mW (MAX.)
Standby: 220 μ W (MAX.)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
28-pin, 600-mil DIP
28-pin, 450-mil SOP

DESCRIPTION

The LH52256LL is an ultra-low power CMOS-periphery static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

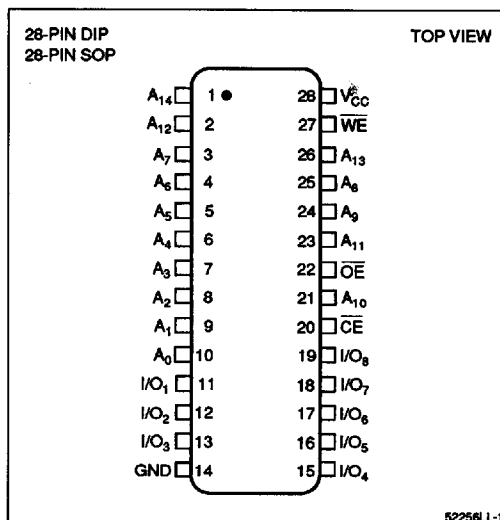


Figure 1. Pin Connections for DIP and SOP Packages

SHARP CORP

51E D ■ 8180798 0006185 59T ■ SRPJ

T-46-23-13

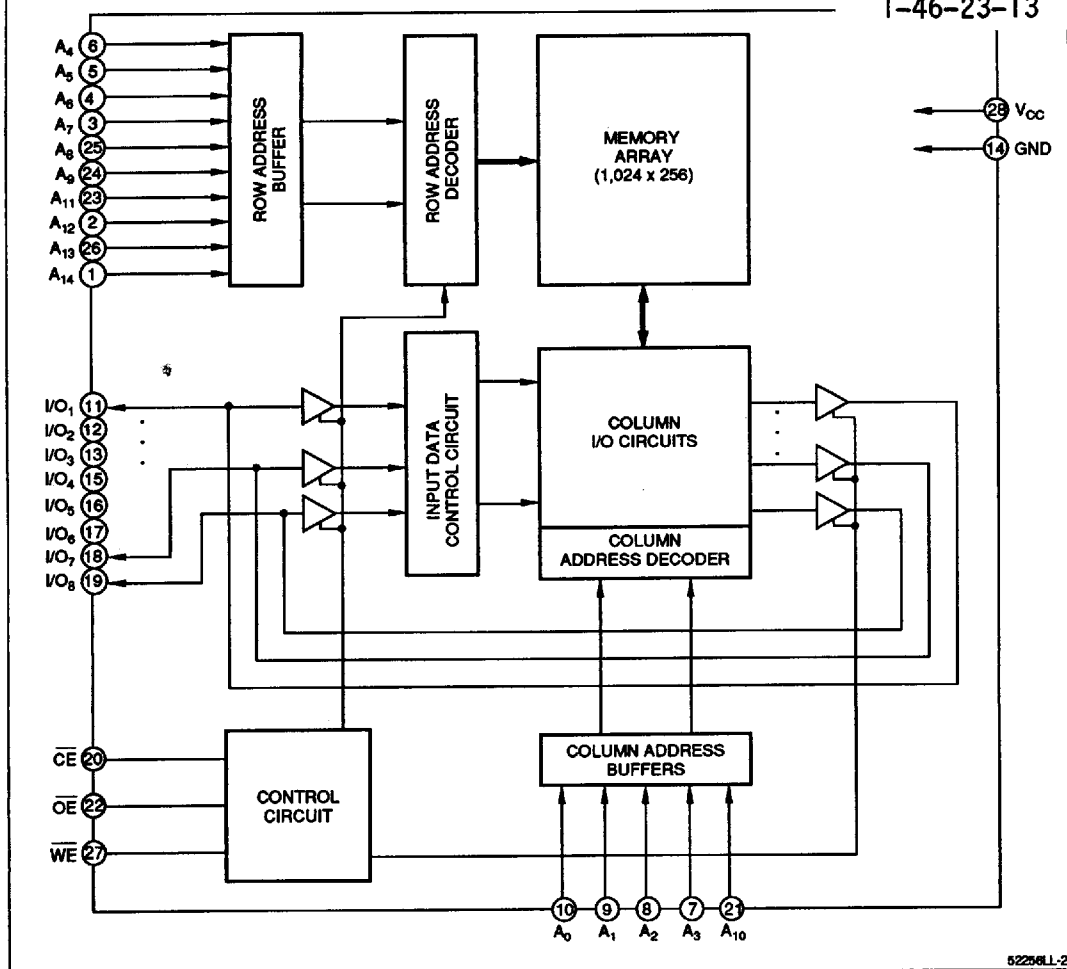


Figure 2. LH52256LL Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
$A_0 - A_{14}$	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input

SIGNAL	PIN NAME
$I/O_1 - I/O_8$	Data Inputs and outputs
V_{CC}	Power supply
GND	Ground

SHARP CORP

51E D ■ 8180798 0006186 426 ■ SRPJ

TRUTH TABLE

T-46-23-13

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	$IO_1 - IO_8$	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	Read	DO _{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	
L	L	X	Write	DI _{IN}	Operating (I_{CC})	1

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	T_{opr}	0 to +70	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	3.5	$V_{CC} + 0.3$	V
	V_{IL}	-0.3		+0.8	V

DC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$ I_{LI} $	$V_{CC} = 5.5$ $V_{IN} = 0$ to V_{CC}			1	μA
Output leakage current	$ I_{LO} $	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, $V_{IO} = 0$ to V_{CC}			1	μA
Operating current	I_{CC}	$\overline{CE} = V_{IL}$, Outputs open			70	mA
	I_{CC1}	$V_{IH} = 3.5\text{ V}$, $V_{IL} = 0.6\text{ V}$ Outputs open			65	mA
	I_{CC2}	$V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$ Outputs open			70	mA
Standby current	I_{SB1}	$\overline{CE} = V_{IH}$			3	mA
	I_{SB}	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$		2	40	μA
Output voltage	V_{OL}	$I_{OL} = 2\text{ mA}$			0.4	V
	V_{OH}	$I_{OH} = -1.0\text{ mA}$	2.4			V

T-46-23-13

AC CHARACTERISTICS

(1) READ CYCLE ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	90		ns	
Address access time	t_{AA}		90	ns	
Chip enable access time	t_{ACE}		90	ns	
Output enable access time	t_{OE}		50	ns	
Output hold from address change	t_{OH}	10		ns	
Chip enable Low to output in Low-Z	t_{LZ}	5		ns	1
Output enable Low to output in Low-Z	t_{OLZ}	5		ns	1
Chip disable to output in High-Z	t_{HZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	90		ns	
Chip enable to end of write	t_{CW}	55		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	55		ns	
Write recovery time	t_{WR}	5		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	5		ns	1
Write Low to output in High-Z	t_{WZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a $\pm 500\text{ mV}$ transition from steady state levels into the test load. $C_{LOAD} = 5\text{ pF}$.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	1.0 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, $C_L = 100\text{ pF}$ (includes scope and jig capacitance)

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

T-46-23-13

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V _{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2 \text{ V}$	2.0			V
Data retention current	I _{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2 \text{ V}$, $V_{CCDR} = 3.0 \text{ V}$	T _A = 25°C		1	μA
			T _A = 0 to 40°C		3	
			T _A = 0 to 70°C		20	
Chip disable to data retention	t _{CDR}		0			ns
Recovery time	t _R		t _{RC} *			ns

* t_{RC} = Read cycle time

CAPACITANCE¹ (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$		8	pF
Input/output capacitance	C_{IO}	$V_{IO} = 0\text{ V}$		10	pF

NOTE:

1. This parameter is sampled and not production tested.

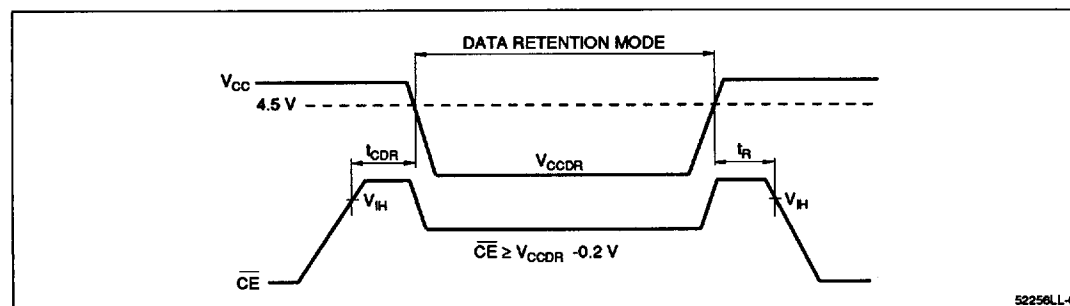


Figure 3. Low Voltage Data Retention

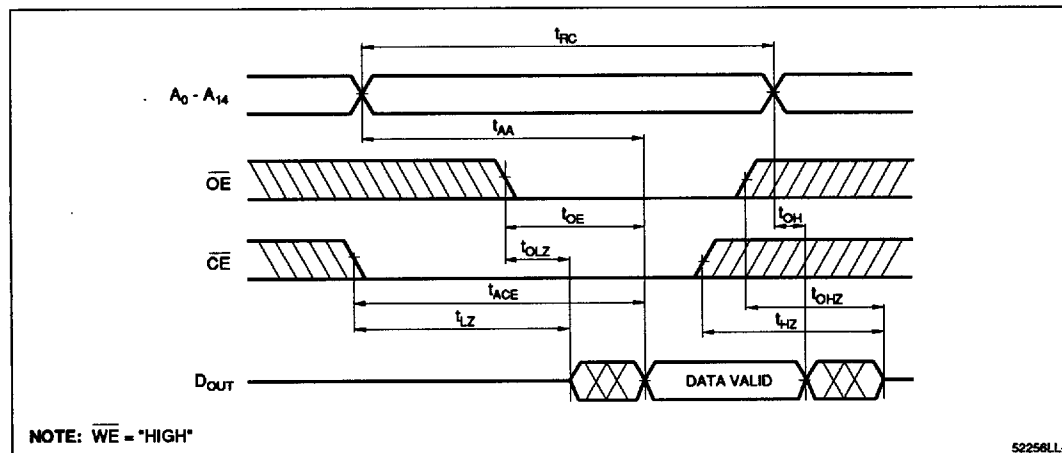


Figure 4. Read Cycle

T-46-23-13

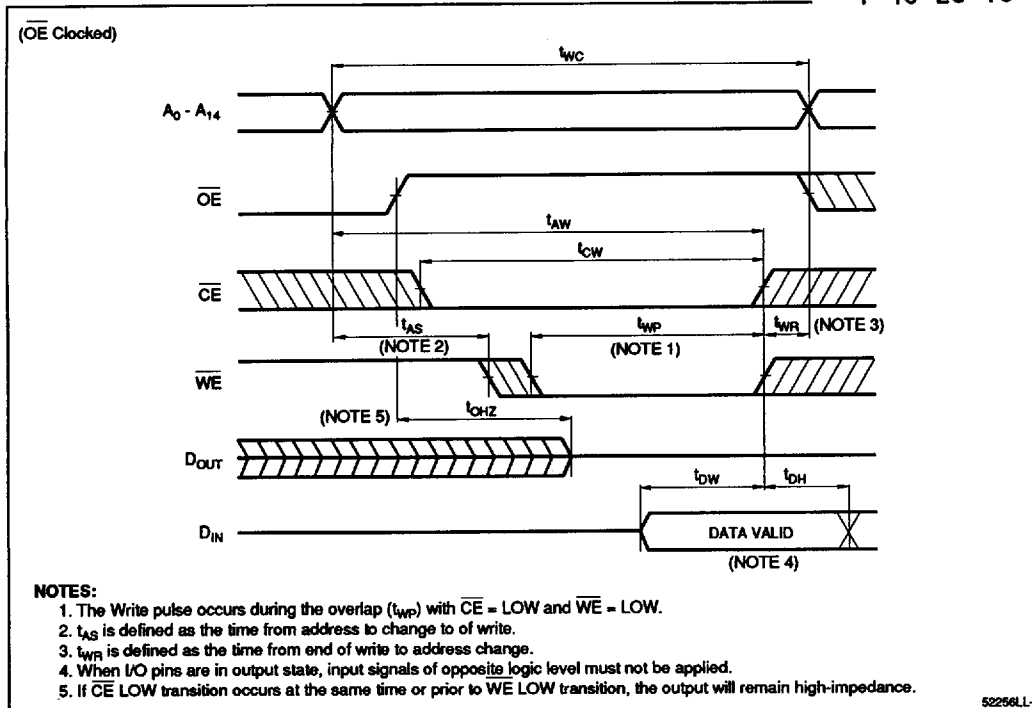


Figure 5. Write Cycle 1

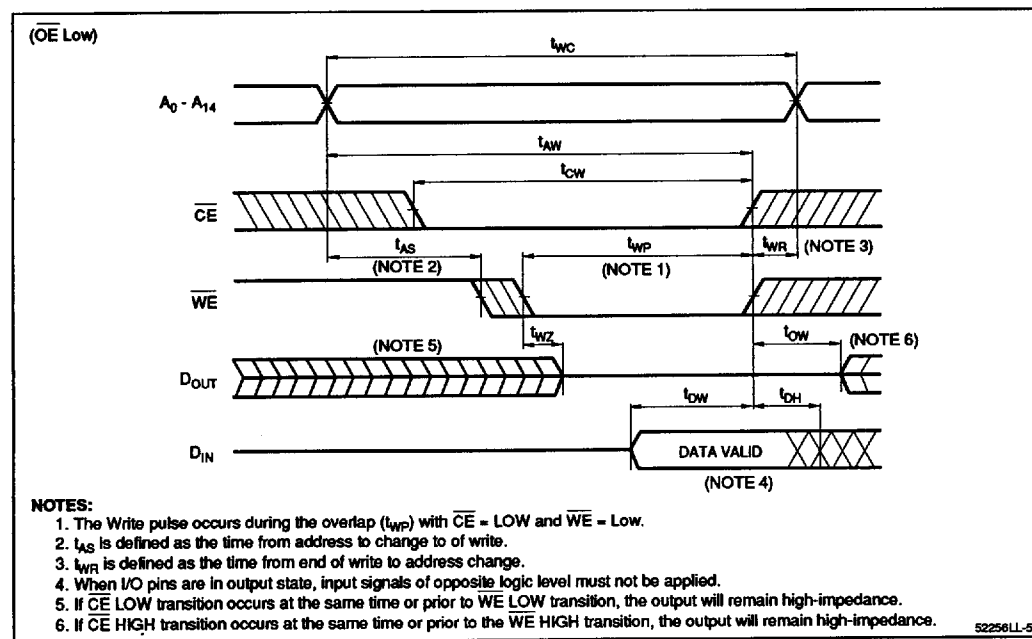


Figure 6. Write Cycle 2

ORDERING INFORMATION

T-46-23-13

