

LH532000B-1

CMOS 2M (256K × 8/128K × 16) MROM

FEATURES

- 262,144 words × 8 bit organization (Byte mode)
131,072 words × 16 bit organization (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
Operating: 275 mW (MAX.)
Standby: 550 μW (MAX.)
- Mask-programmable control pin (for 40-pin DIP/40-pin SOP):
Pin 1 = OE₁/OE₁/DC
Pin 12 = OE/OE
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
40-pin, 600-mil DIP
40-pin, 525-mil SOP
48-pin, 12 × 18 mm² TSOP (Type I)

DESCRIPTION

The LH532000B-1 is a CMOS 2M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

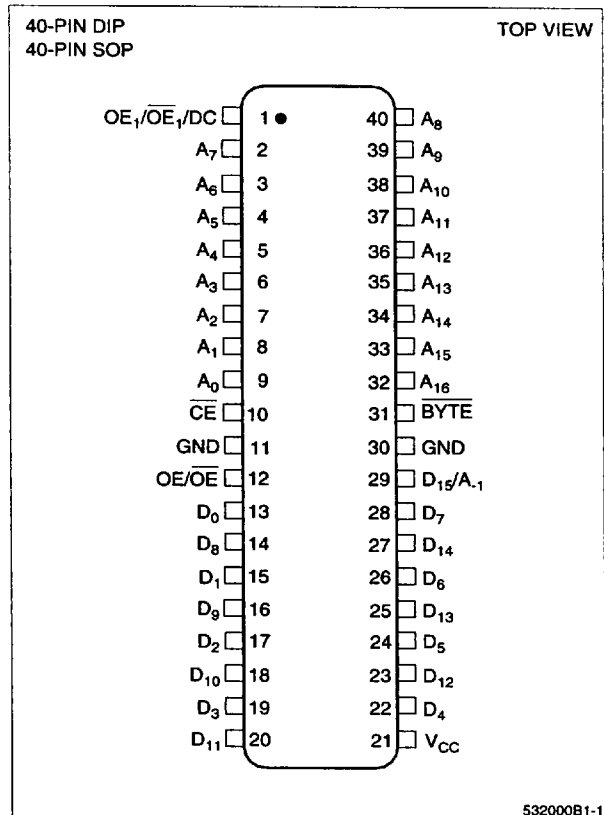


Figure 1. Pin Connections for DIP and SOP Packages

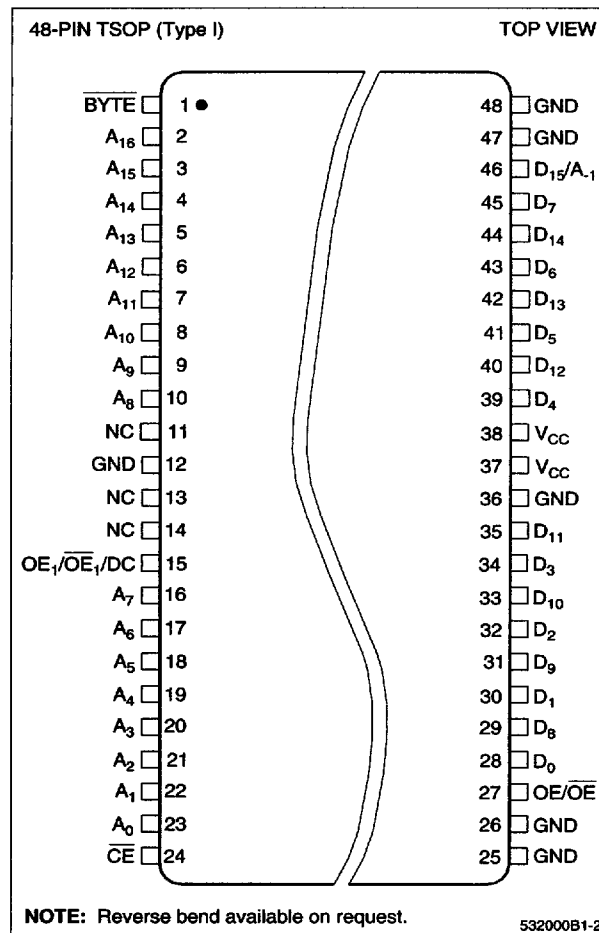


Figure 2. Pin Connections for TSOP Package

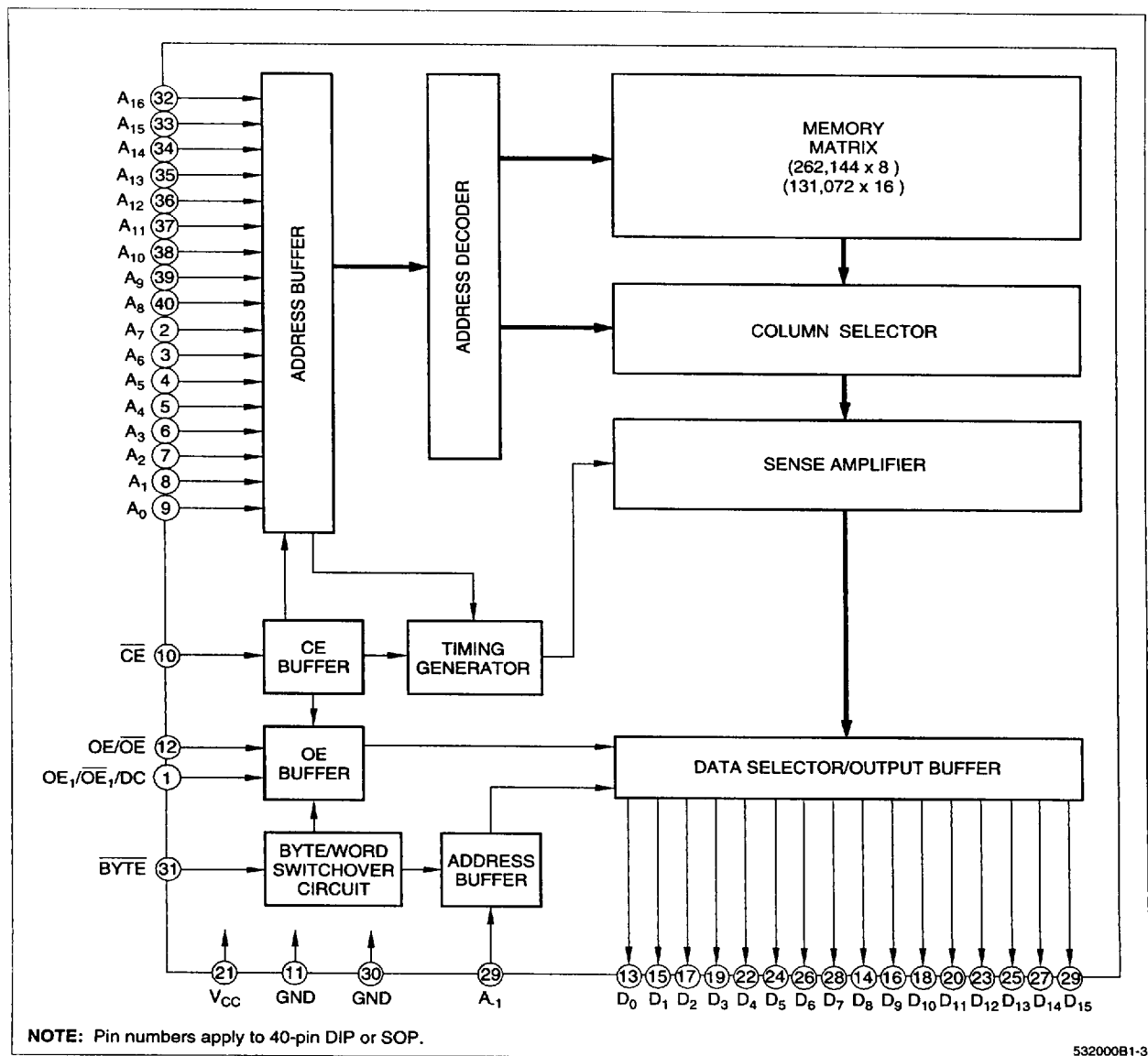


Figure 3. LH532000B-1 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE	SIGNAL	PIN NAME	NOTE
A ₁ – A ₁₆	Address input	1	OE/OE	Output enable input	2
D ₀ – D ₁₅	Data output	1	OE ₁ /OE ₁ /DC	Output enable input	2
BYTE	Byte/word mode switch	1	V _{CC}	Power supply (+5 V)	
CE	Chip enable input		GND	Ground	

NOTES:

1. D₁₅/A₁ pin becomes LSB address input (A₁) when the BYTE pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.
2. The active levels of OE/OE and OE₁/OE₁/DC are mask-programmable.

TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}$	$OE_1/\overline{OE}_1$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	—	—	Standby (I_{SB})
L	L/H	X	X	X	High-Z	High-Z	—	—	Operating (I_{CC})
L	X	L/H	X	X	High-Z	High-Z	—	—	Operating (I_{CC})
L	H/L	H/L	H	—	$D_0 - D_7$	$D_8 - D_{15}$	A_0	A_{16}	Operating (I_{CC})
L	H/L	H/L	L	L	$D_0 - D_7$	High-Z	A_{-1}	A_{16}	Operating (I_{CC})
L	H/L	H/L	L	H	$D_8 - D_{15}$	High-Z	A_{-1}	A_{16}	Operating (I_{CC})

NOTE:

1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		$V_{CC} + 0.3$	V	
Output 'Low' voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$			0.4	V	
Output 'High' voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4			V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{CC}$			10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$			10	μA	1
Operating current	I_{CC1}	$t_{RC} = 120\text{ ns}$			50	mA	2
	I_{CC2}	$t_{RC} = 1\text{ }\mu\text{s}$			45	mA	2
	I_{CC3}	$t_{RC} = 120\text{ ns}$			45	mA	3
	I_{CC4}	$t_{RC} = 1\text{ }\mu\text{s}$			40	mA	3
Standby current	I_{SB1}	$CE = V_{IH}$			3	mA	
	I_{SB2}	$CE = V_{CC} - 0.2\text{ V}$			100	μA	
Input capacitance	C_{IN}	$f = 1\text{ MHz}$			10	pF	
Output capacitance	C_{OUT}	$T_A = 25^\circ\text{C}$			10	pF	

NOTES:

- $CE/OE/OE_1 = V_{IH}$, $OE/OE_1 = V_{IL}$
- $V_{IN} = V_{IH}$ or V_{IL} , $CE = V_{IL}$, outputs open
- $V_{IN} = (V_{CC} - 0.2\text{ V})$ or 0.2 V , $CE = 0.2\text{ V}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable access time	t_{ACE}		120	ns	
Output enable delay time	t_{OE}		55	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		55	ns	1
OE to output in High-Z	t_{OHZ}		55	ns	

NOTE:

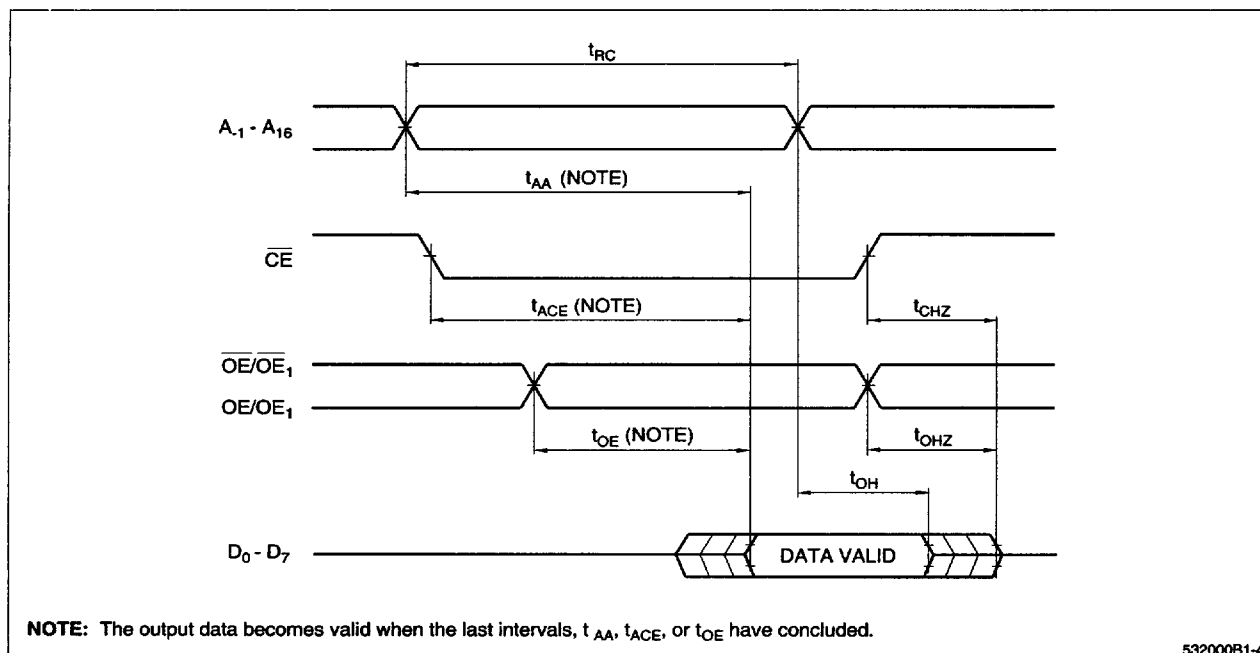
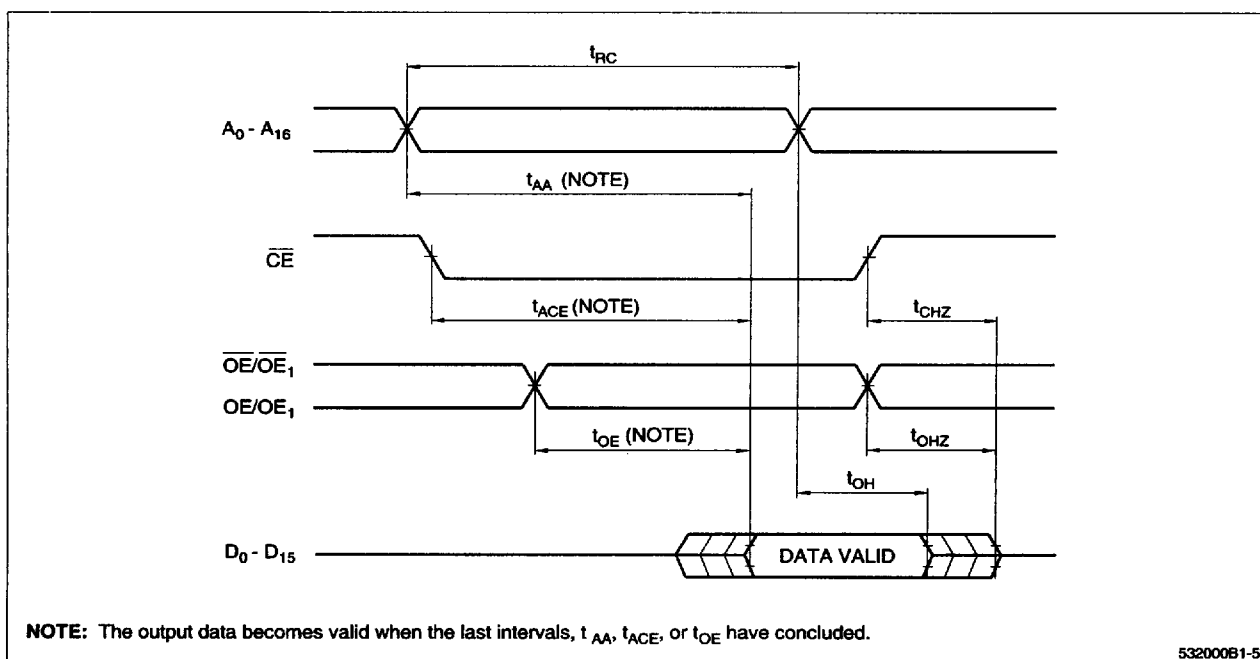
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

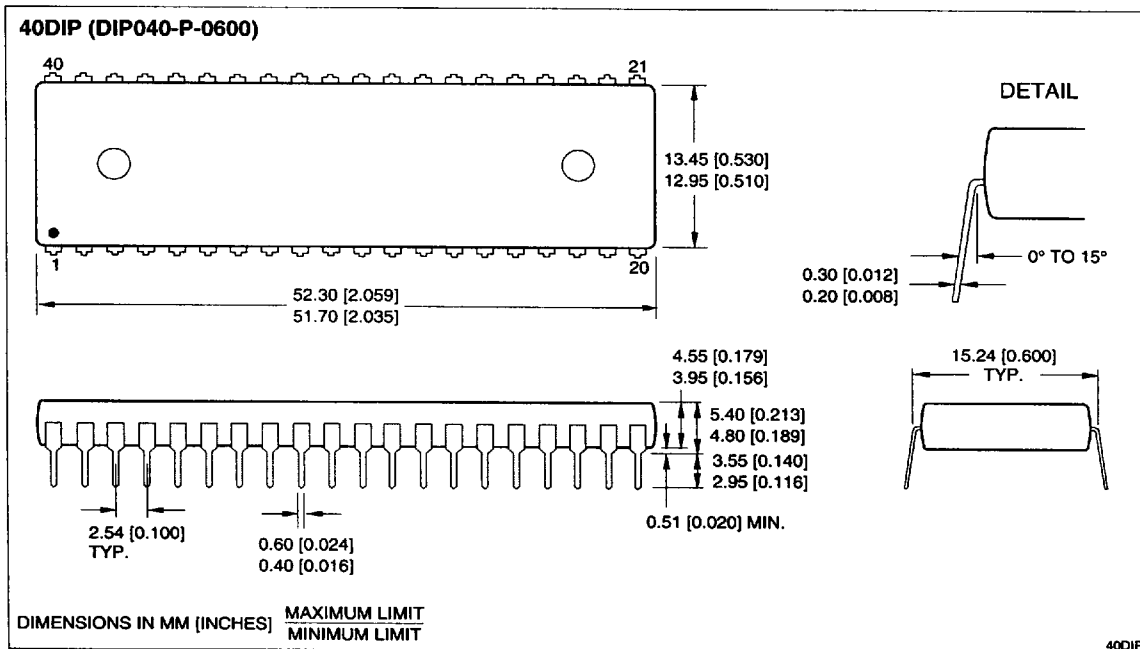
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1 TTL + 100 pF

CAUTION

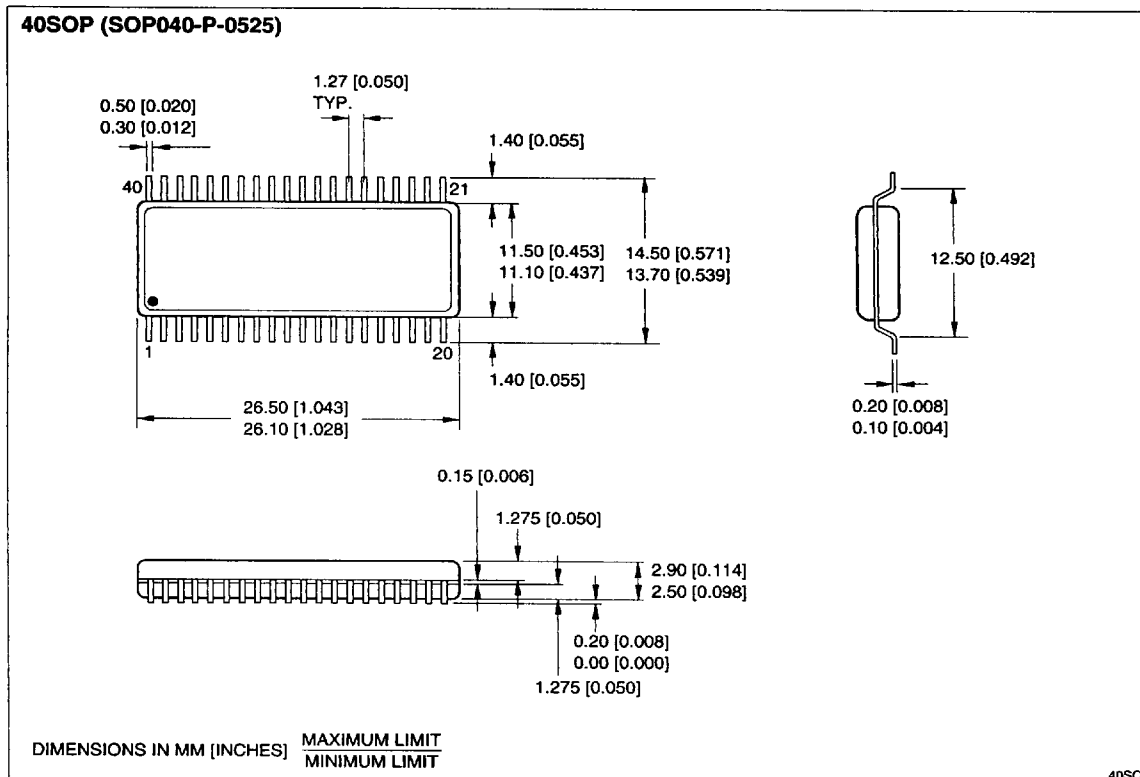
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

Figure 4. Byte Mode (BYTE = V_{IL})Figure 5. Word Mode (BYTE = V_{IH})

PACKAGE DIAGRAMS

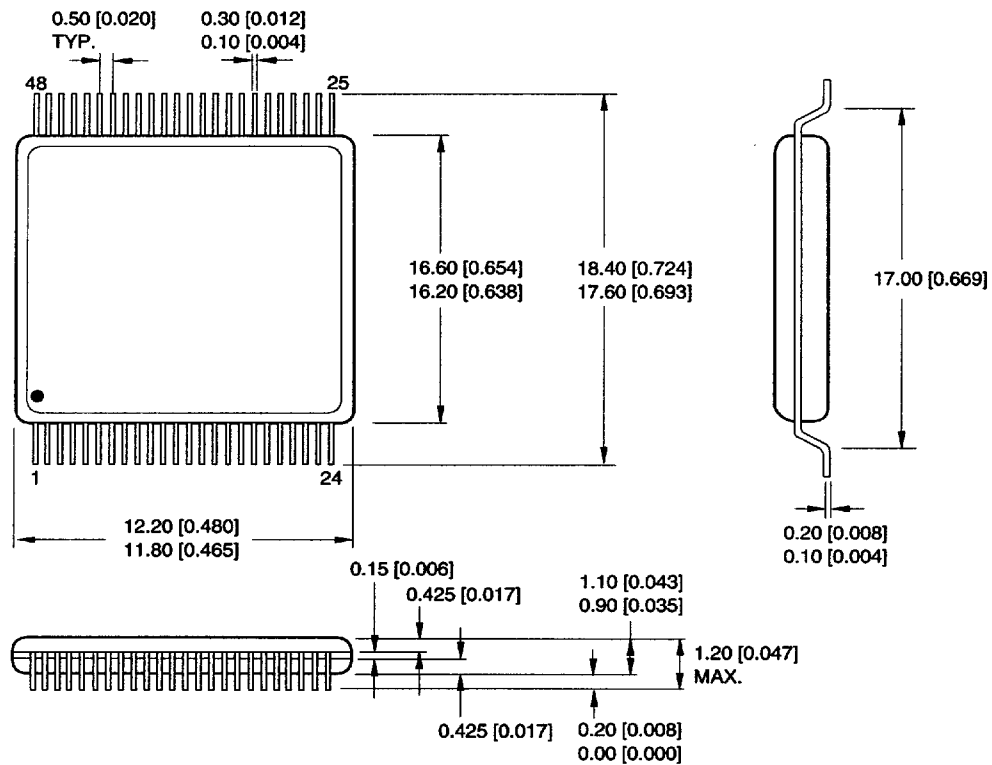


40-pin, 600-mil DIP



40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)



DIMENSIONS IN MM [INCHES]

MAXIMUM LIMIT	MINIMUM LIMIT

48TSOP

48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION

LH532000B	X	-1
Device Type	Package	120 ns Version
		{ D 40-pin, 600-mil DIP (DIP040-P-0600) N 40-pin, 525-mil SOP (SOP040-P-0525) T 48-pin, 12 x 18 mm ² TSOP (Type I) (TSOP048-P-1218) TR 48-pin, 12 x 18 mm ² TSOP (Type I) Reverse bend (TSOP048-P-1218)
		CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM
Example: LH532000BD-1 (CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM, 40-pin, 600-mil DIP)		

532000B1-6