LH532100B

CMOS 2M (256K × 8) MROM

FEATURES

- 262,144 words × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- Mask-programmable OE/OE and $OE_1/OE_1/DC$
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 450-mil QFJ (PLCC)
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  32-pin, 400-mil TSOP (Type II)
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH532100B is a 2M-bit mask-programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

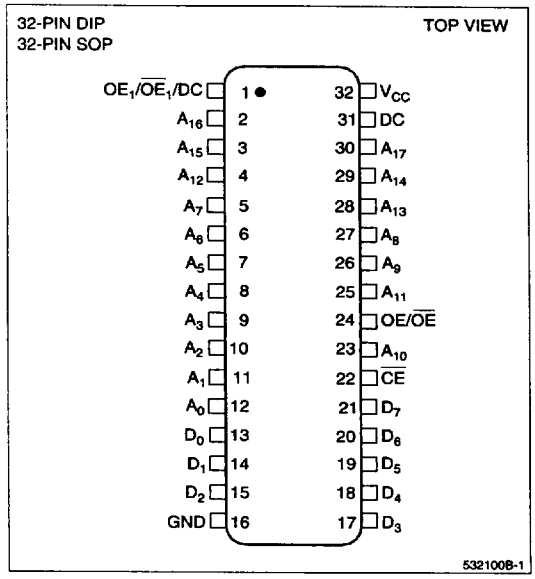


Figure 1. Pin Connections for DIP and SOP Packages

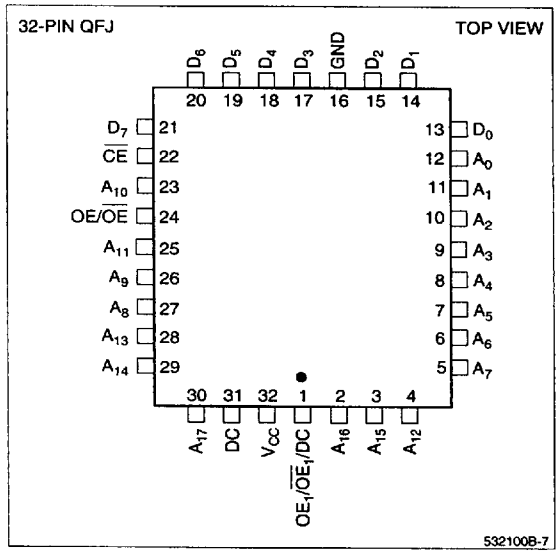


Figure 2. Pin Connections QFJ (PLCC) Package

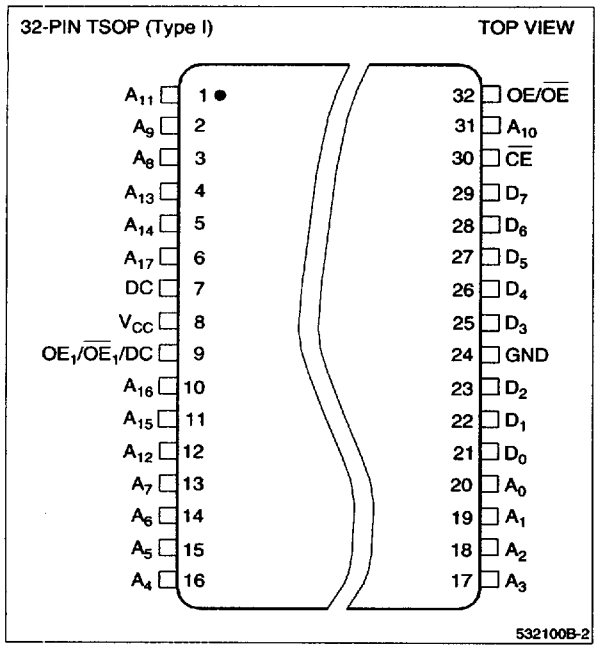


Figure 3. Pin Connections for TSOP (Type I) Package

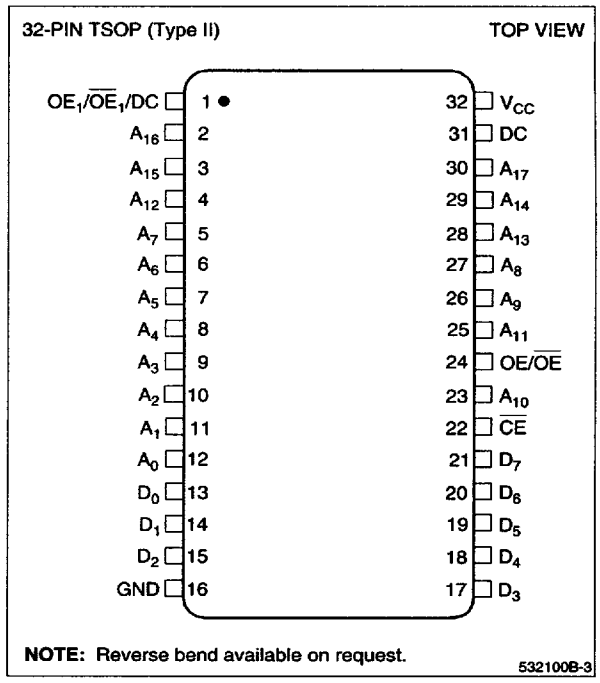


Figure 4. Pin Connections for TSOP (Type II) Packages

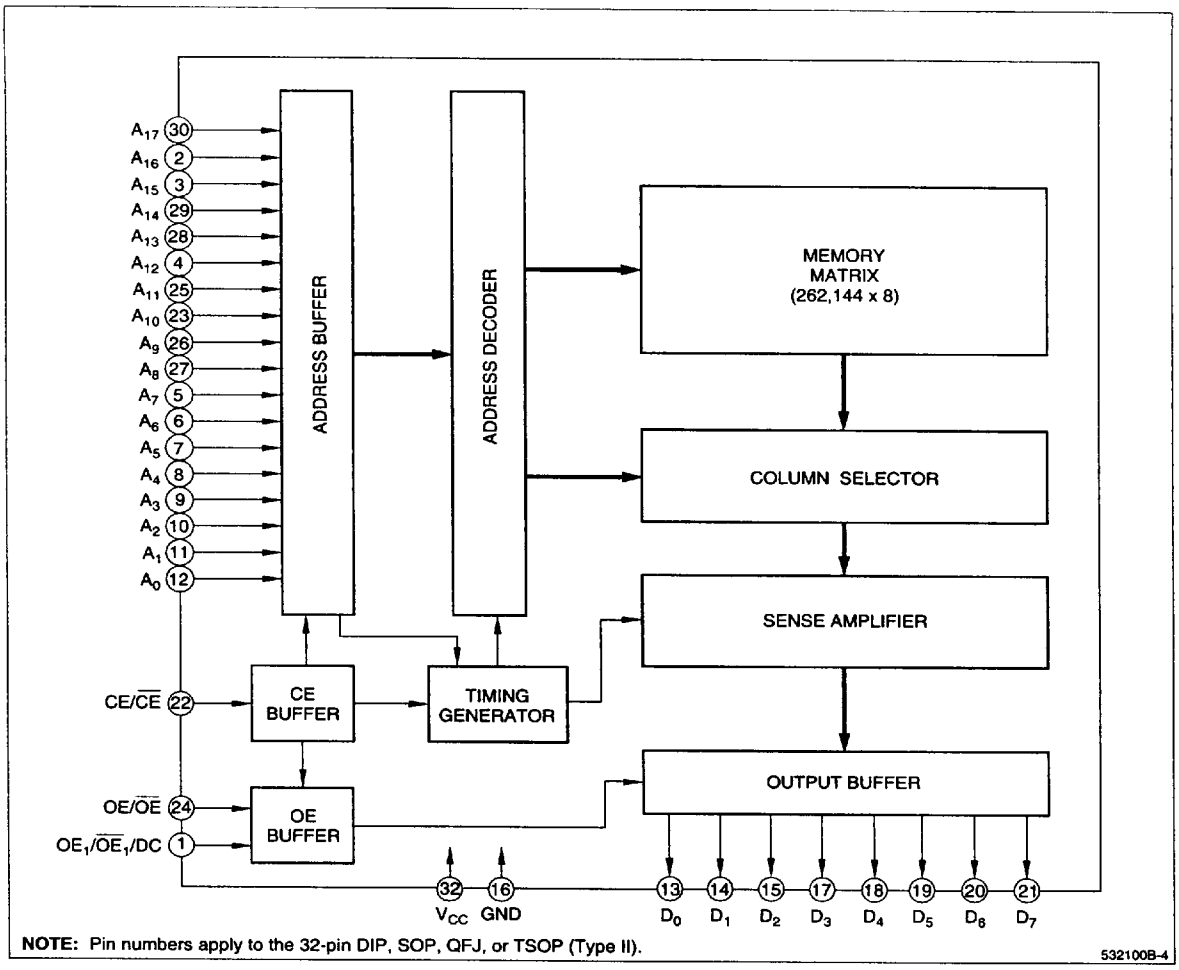


Figure 5. LH532100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE	SIGNAL	PIN NAME	NOTE
$A_0 - A_{17}$	Address input		$OE_1/OE_1/DC$	Output Enable input/ Don't Care connection	1
$D_0 - D_7$	Data output		V_{CC}	Power supply (+5 V)	
CE	Chip Enable input		GND	Ground	
OE/OE	Output Enable input	1			

NOTE:
1. Active levels of OE/OE and $OE_1/OE_1/DC$ are mask-programmable.
   Selecting DC allows the outputs to be active for both high and low levels applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	$D_0 - D_7$	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		−0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = −400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = t_{RC} (MIN.)			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = t_{RC} (MIN.)			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	CE = V_{IL}, CE = V_{IH}			3	mA	
	I_{SB2}	CE = 0.2 V, CE = V_{CC} − 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz			10	pF	
Output capacitance	C_{OUT}	T_A = 25°C			10	pF	

NOTES:
1. $CE/\overline{OE}/\overline{OE_1} = V_{IH}$, $\overline{OE}/\overline{OE_1} = V_{IL}$
2. $V_{IN} = V_{IH}$ or V_{IL}, $CE = V_{IL}$, outputs open
3. $V_{IN} = (V_{CC} - 0.2\ V)$ or 0.2 V, CE = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable access time	t_{ACE}		150	ns	
Output enable delay time	t_{OE}	10	70	ns	
Output hold time	t_{OH}	10		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

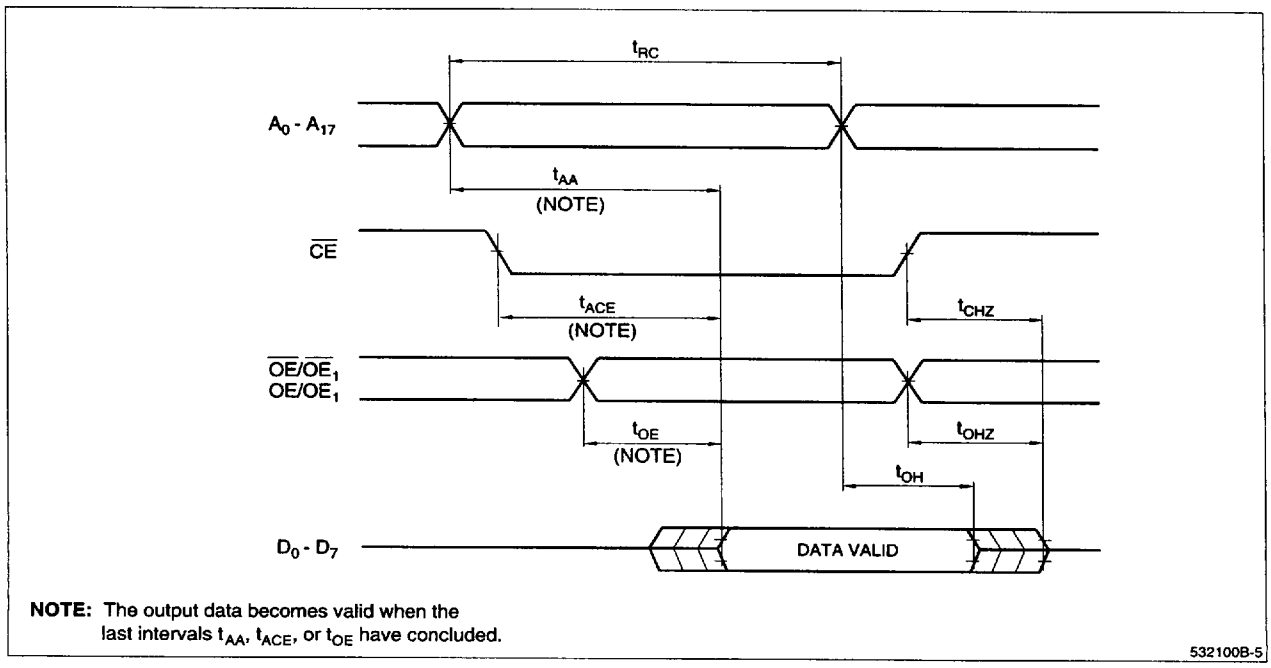
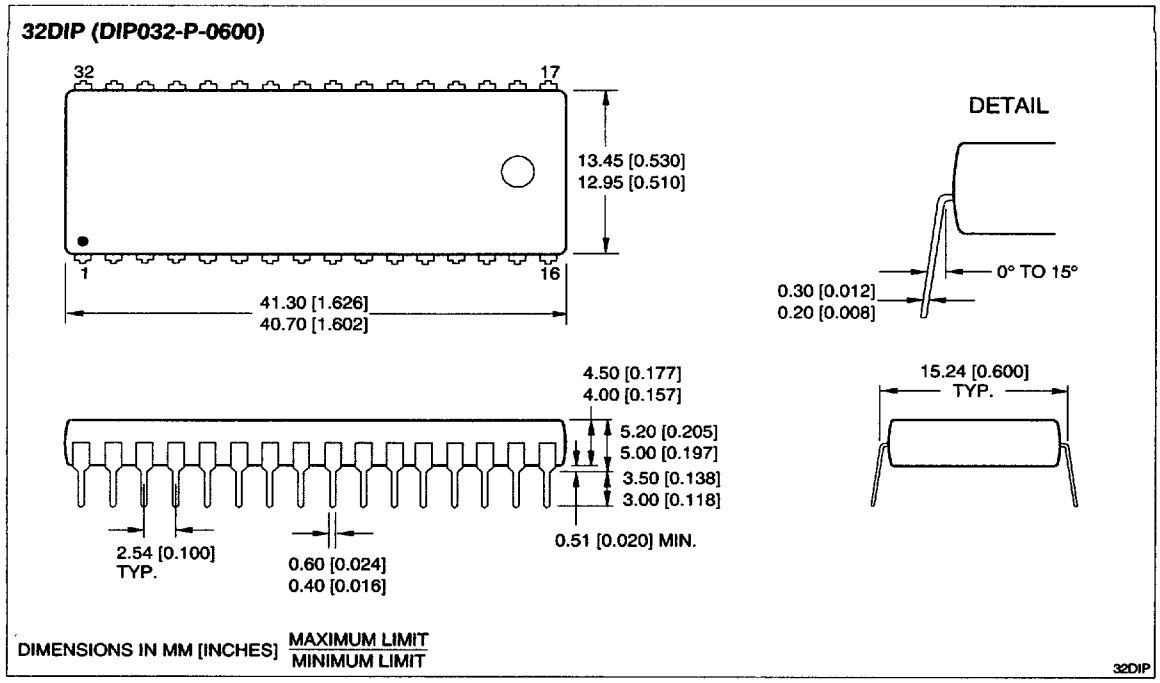
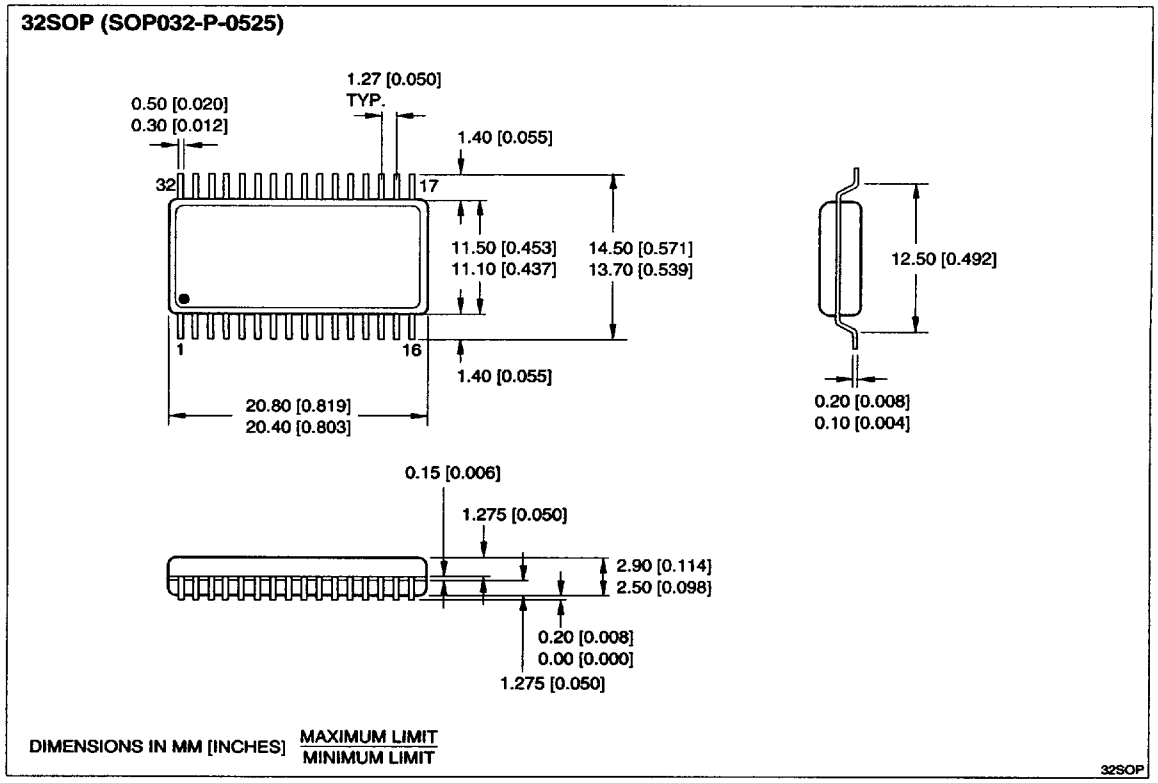


Figure 6. Timing Diagram

PACKAGE DIAGRAMS

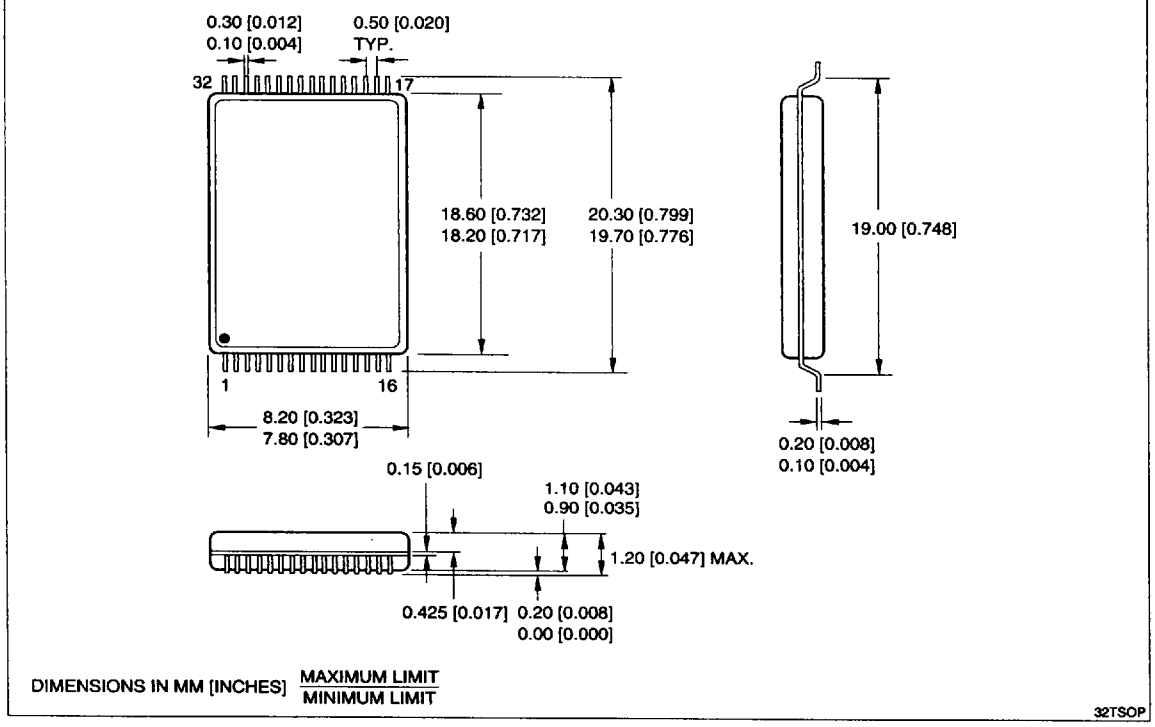


32-pin, 600-mil DIP



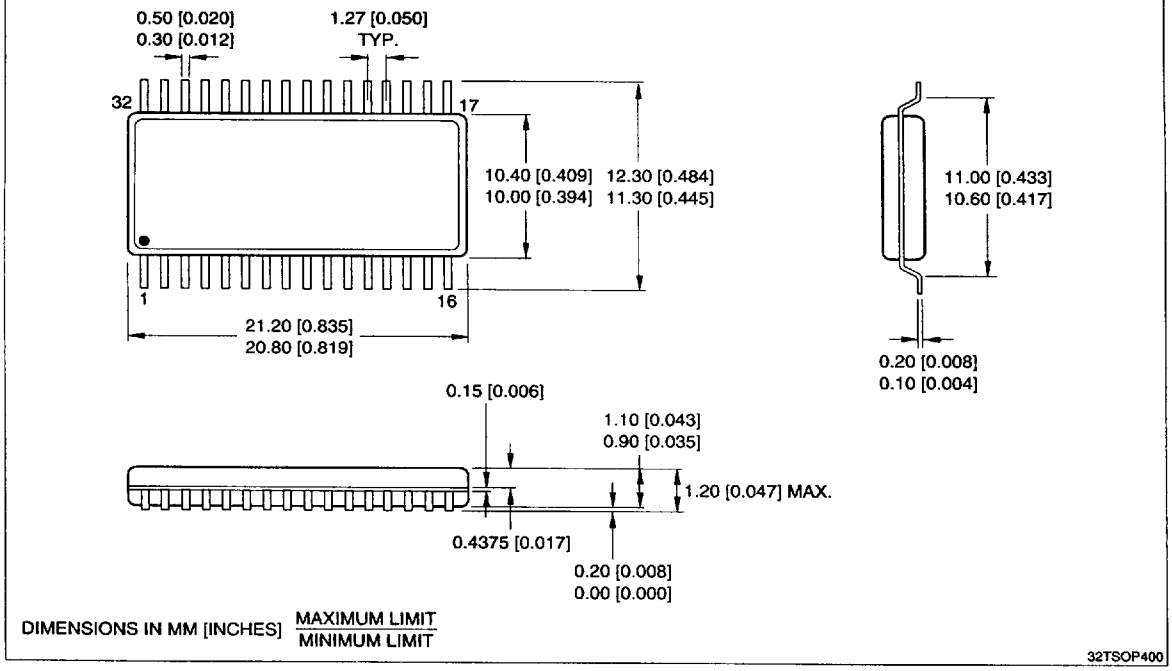
32-pin, 525-mil SOP

32TSOP (Type I) (TSOP032-P-0820)



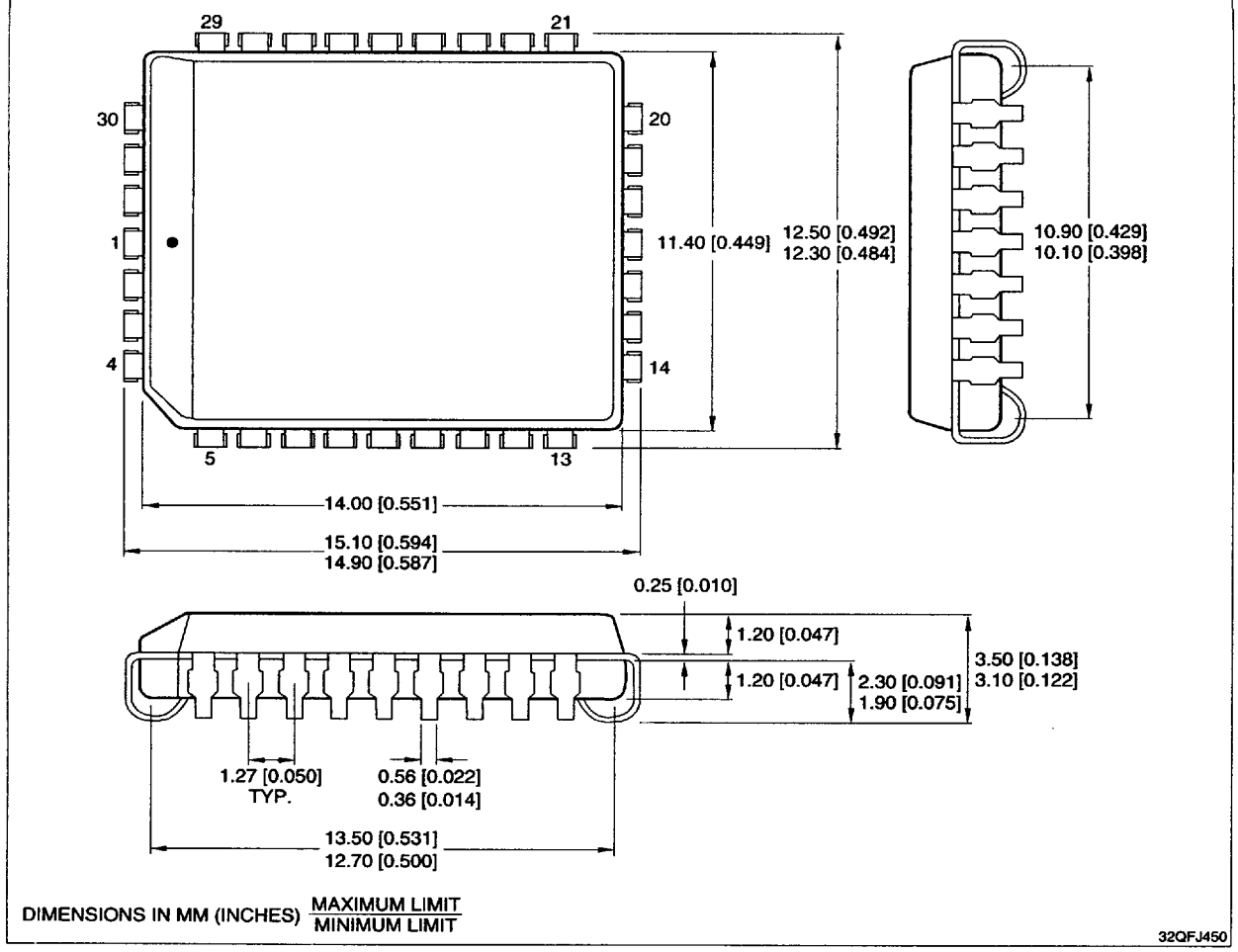
32-pin, 8 × 20 mm² TSOP (Type I)

32TSOP (Type II) (TSOP032-P-0400)



32-pin, 400-mil TSOP (Type II)

32QFJ (QFJ032-P-R450)



32-pin, 450-mil QFJ (PLCC)

ORDERING INFORMATION

LH532100B	X
Device Type	Package

- Package:
  - D 32-pin, 600-mil DIP (DIP032-P-0600)
  - N 32-pin, 525-mil SOP (SOP032-P-0525)
  - U 32-pin, 450-mil QFJ (PLCC) (QFJ032-P-R450)
  - T 32-pin, 8 x 20 mm^2 TSOP (Type I) (TSOP032-P-0820)
  - S 32-pin, 400-mil TSOP (Type II) (TSOP032-P-0400)
  - SR 32-pin, 400-mil TSOP (Type II) Reverse bend (TSOP032-P-0400)
- Device Type: CMOS 2M (256K x 8) Mask-Programmable ROM

Example: LH532100BD (CMOS 2M (256K x 8) Mask-Programmable ROM, 32-pin, 600-mil DIP)

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