

LH532600

CMOS 2M (256K × 8/128K × 16) MROM

FEATURES

- 262,144 words × 8 bit organization (Byte mode)
131,072 words × 16 bit organization (Word mode)
- Access time: 100 ns (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Power consumption:
Operating: 412.5 mW (MAX.)
Standby: 550 μ W (MAX.)
- Mask-programmable control pin:
Pin 1 = $\overline{OE}_1/\overline{OE}_1/\overline{DC}$
- Packages:
40-pin, 600-mil DIP
40-pin, 525-mil SOP
48-pin, 10 × 20 mm² TSOP (Type I)

DESCRIPTION

The LH532600 is a 2M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

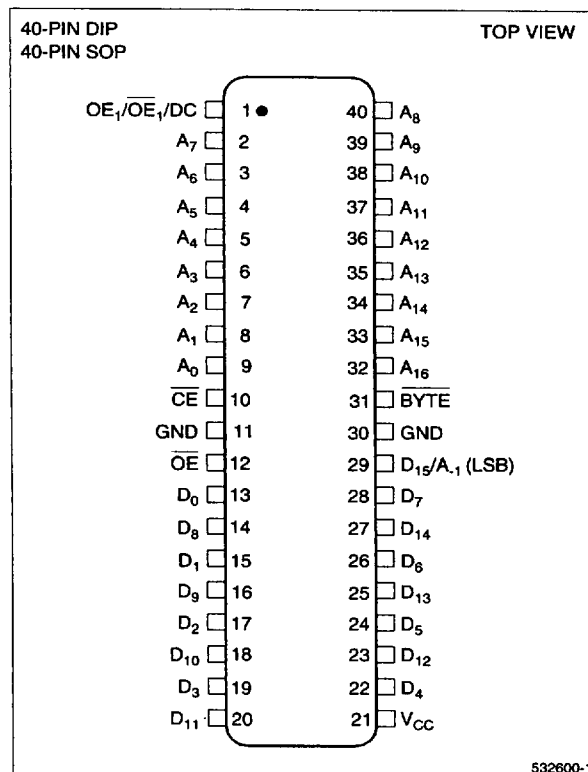


Figure 1. Pin Connections for DIP and SOP Packages

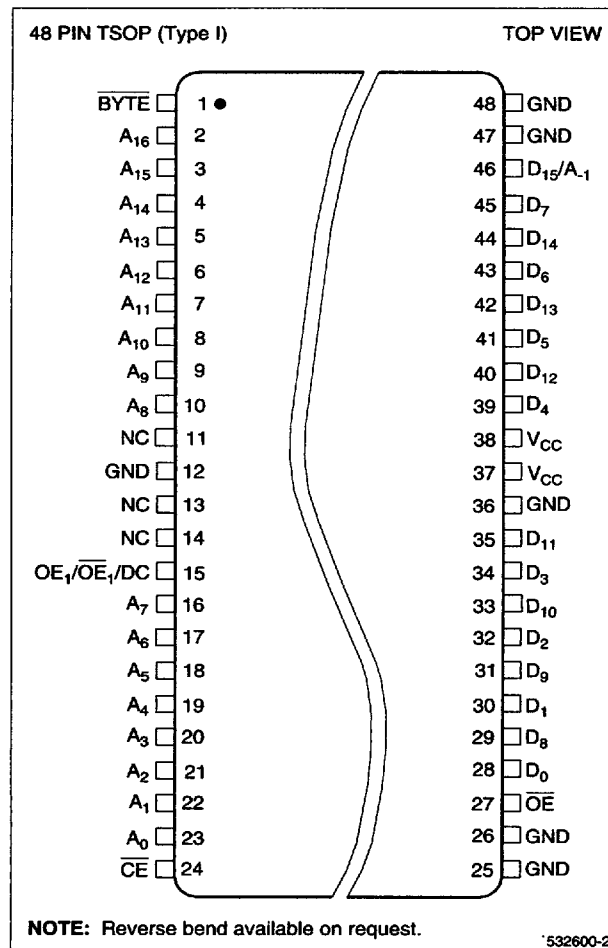


Figure 2. Pin Connections for TSOP Package

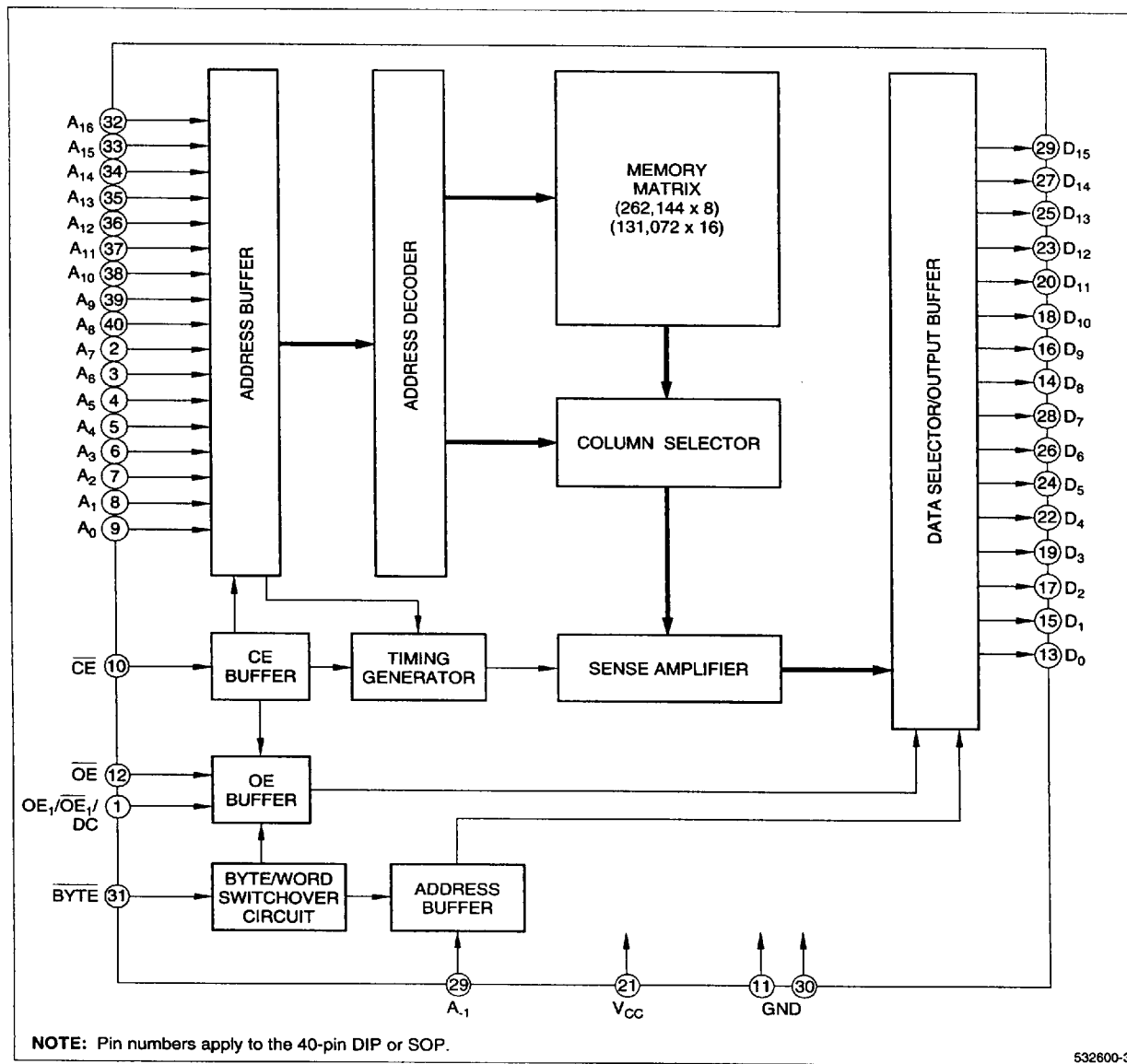


Figure 3. LH532600 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE	SIGNAL	PIN NAME	NOTE
A ₁ – A ₁₆	Address input	1	OE	Output enable input	
D ₀ – D ₁₅	Data output	1	OE ₁ /OE ₁ /DC	Output enable input	2, 3
BYTE	Byte/word mode switch	1	V _{CC}	Power supply (+5 V)	
CE	Chip enable input		GND	Ground	

NOTES:

1. The D₁₅/A₁ pin becomes LSB address input (A₁) when the BYTE pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.
2. Active levels of OE₁/OE₁/DC are mask-programmable. When DC is selected out of OE₁/OE₁/DC, it is fixed to an active level. Then it is recommended to apply either V_{IH} or V_{IL} to the DC pin.
3. DC = Don't care.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$OE_1/\overline{OE}_1$	BYTE	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	—	—	Standby
L	H	X	X	X	High-Z	High-Z	—	—	Operating
L	X	L/H	X	X	High-Z	High-Z	—	—	Operating
L	L	H/L	H	—	$D_0 - D_7$	$D_8 - D_{15}$	A_0	A_{16}	Operating
L	L	H/L	L	L	$D_0 - D_7$	High-Z	A_{-1}	A_{16}	Operating
L	L	H/L	L	H	$D_8 - D_{15}$	High-Z	A_{-1}	A_{16}	Operating

NOTE:

X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	$V_{CC} + 0.3$	V	
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Output 'High' voltage	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4		V	
Output 'Low' voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$		0.4	V	
Input leakage current	$ I_{II} $	$V_{IN} = 0\text{ V to } V_{CC}$		10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to } V_{CC}$		10	μA	1
Operating current	I_{CC1}	$t_{RC} = 100\text{ ns}$		75	mA	2
	I_{CC2}	$t_{RC} = 1\ \mu\text{s}$		65	mA	2
	I_{CC3}	$t_{RC} = 100\text{ ns}$		70	mA	3
	I_{CC4}	$t_{RC} = 1\ \mu\text{s}$		60	mA	3
Standby current	I_{SB1}	$CE = V_{IH}$		3	mA	
	I_{SB2}	$CE = V_{CC} - 0.2\text{ V}$		100	μA	
Input capacitance	C_{IN}	$f = 1\text{ MHz}$		10	pF	
Output capacitance	C_{OUT}	$T_A = 25^\circ\text{C}$		10	pF	

NOTES:

1. $CE/OE/OE_1 = V_{IH}$, $OE_1 = V_{IL}$
2. $V_{IN} = V_{IH}$ or V_{IL} , $CE = V_{IL}$, outputs open
3. $V_{IN} = (V_{CC} - 0.2\text{ V})$ or 0.2 V , $CE = 0.2\text{ V}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
Chip enable access time	t_{ACE}		100	ns	
Output enable delay time	t_{OE}		55	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		55	ns	1
OE to output in High-Z	t_{OHZ}				

NOTE:

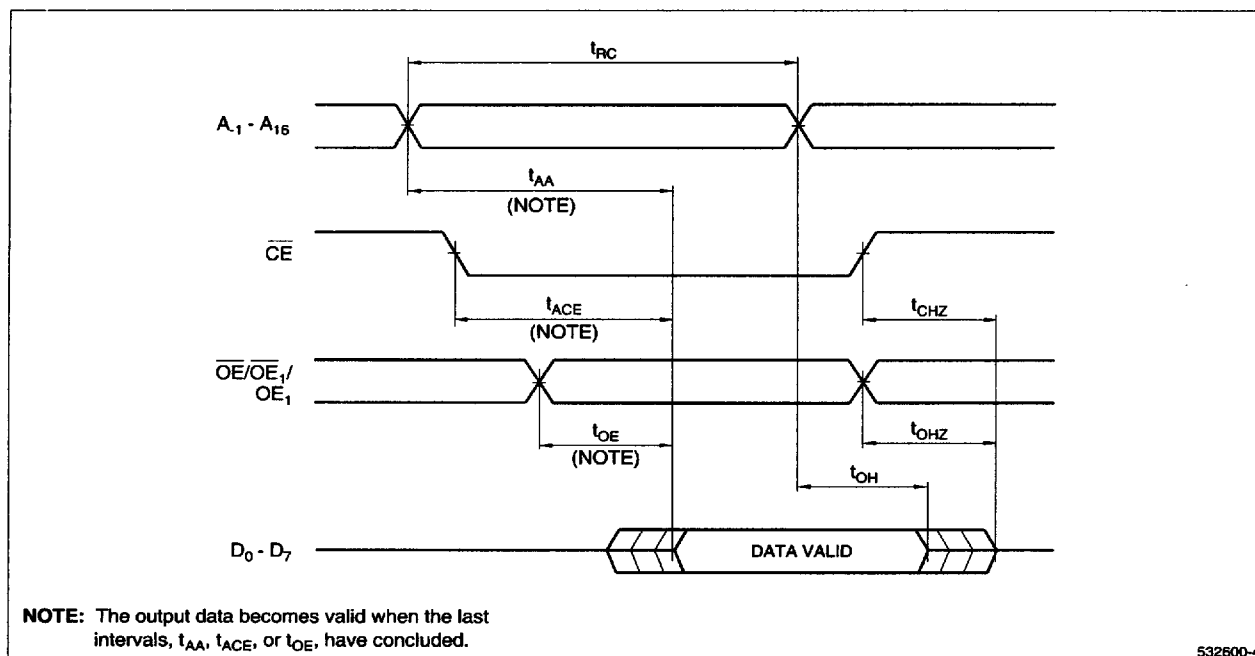
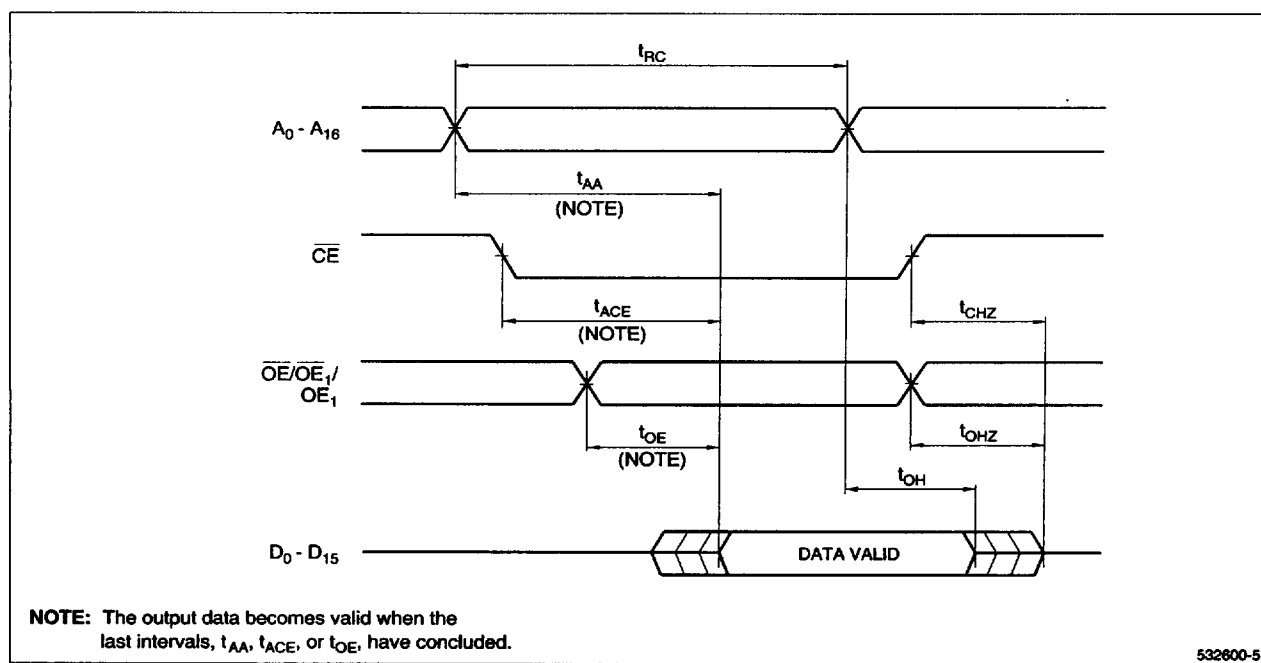
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

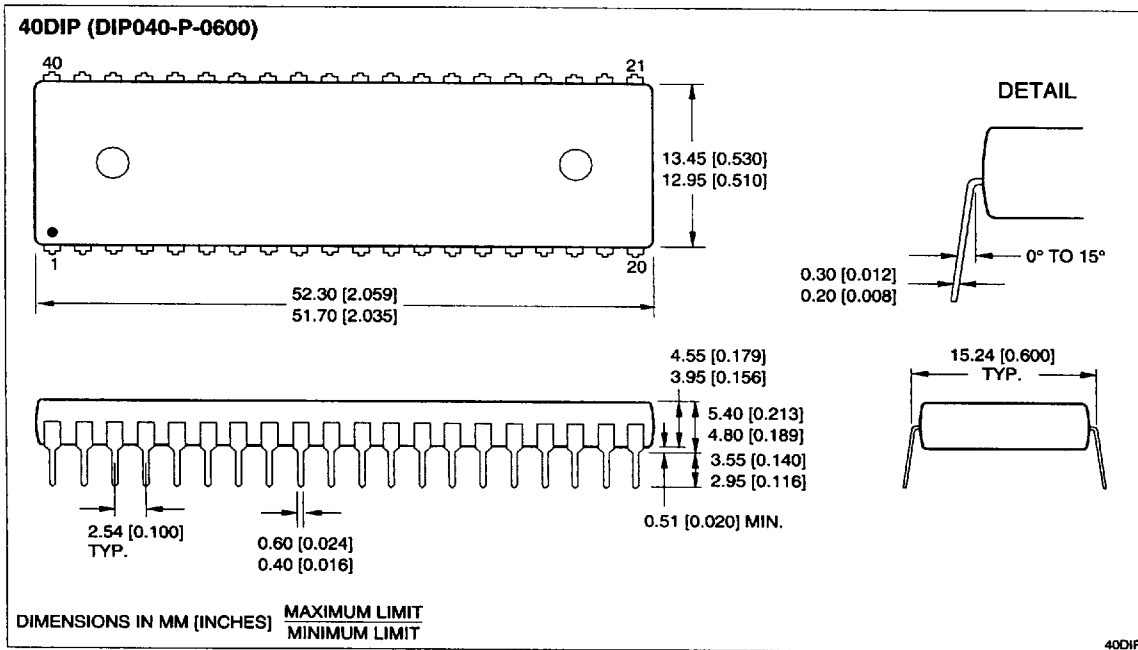
PARAMETER	RATING
Input voltage amplitude	0.4 to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

CAUTION

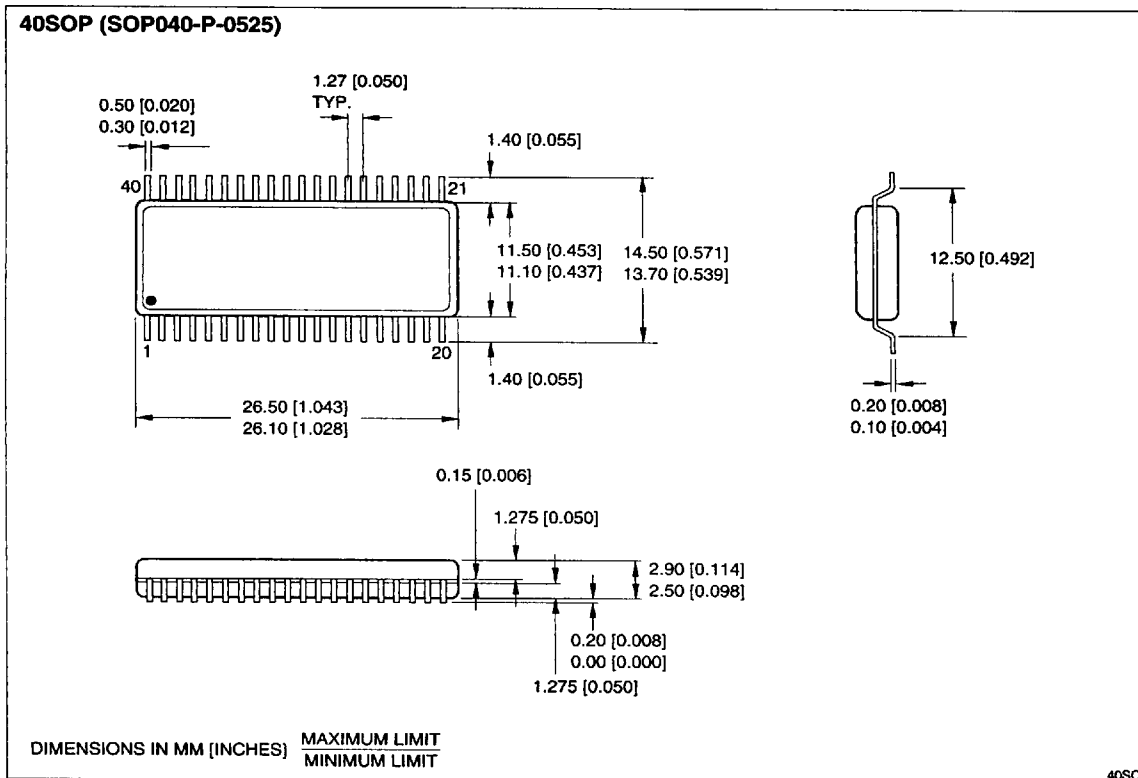
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

Figure 4. Byte Mode (BYTE = V_{IL})Figure 5. Word Mode (BYTE = V_{IH})

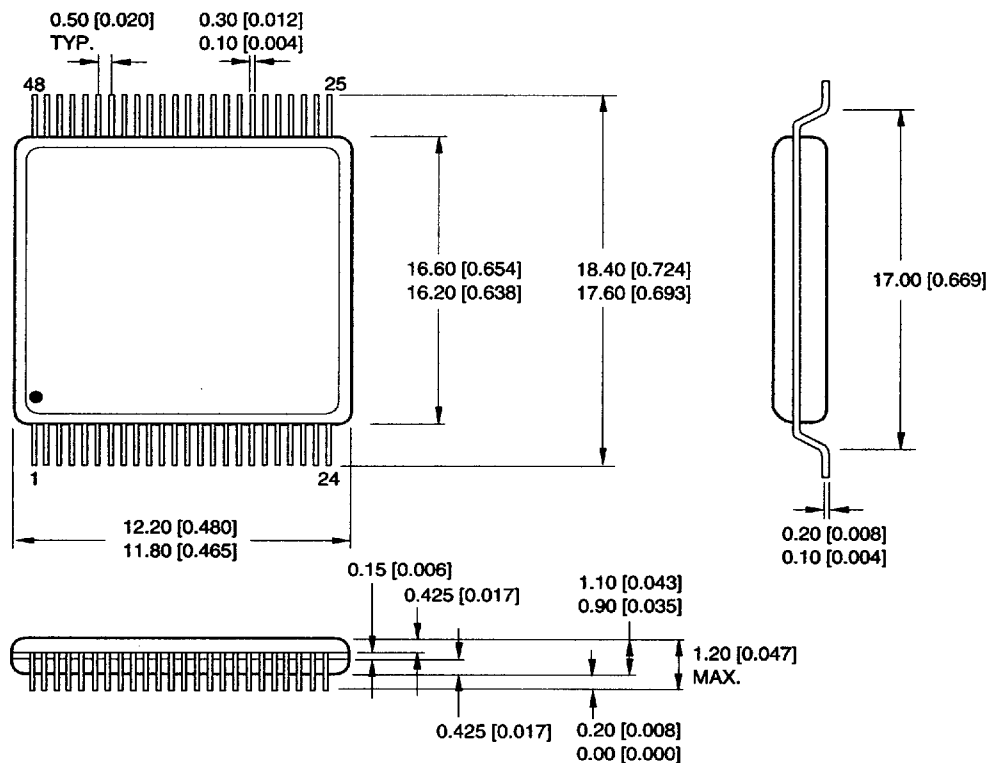
PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)

DIMENSIONS IN MM [INCHES]

MAXIMUM LIMIT
MINIMUM LIMIT

48TSOP

48-pin, 10 × 20 mm² TSOP (Type I)**ORDERING INFORMATION**

LH532600	X
Device Type	Package
	{ D 40-pin, 600-mil DIP (DIP040-P-0600) N 40-pin, 525-mil SOP (SOP040-P-0525) T 48-pin, 10 x 20 mm ² TSOP (Type I) (TSOP048-P-1020) TR 48-pin, 10 x 20 mm ² TSOP (Type I) Reverse bend (TSOP048-P-1020)
	CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM

Example: LH532600D (CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM, 40-pin, 600-mil DIP)

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