

LH534R00B

CMOS 4M (1M × 4) MROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 120 ns (MAX.)
- Supply current:
 - Operating: 65 mA (MAX.)
 - Standby: 100 μ A (MAX.)
- Three-state output
- Single +5 V Power supply
- Static operation
- Input/Output TTL compatible
- Packages:
 - 32-pin, 600-mil SOP
 - 32-pin, 600-mil DIP
- Mask-programmable control pin
 - Pin 1 = $OE_1/\overline{OE}_1/DC$
 - Pin 24 = $OE/\overline{OE}$
- Others:
 - Non programmable
 - Not designed or rated as radiation hardened
 - CMOS process (P type silicon substrate)

DESCRIPTION

The LH534R00B is a 4M-bit CMOS mask ROM (mask-programmable read-only memory) organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

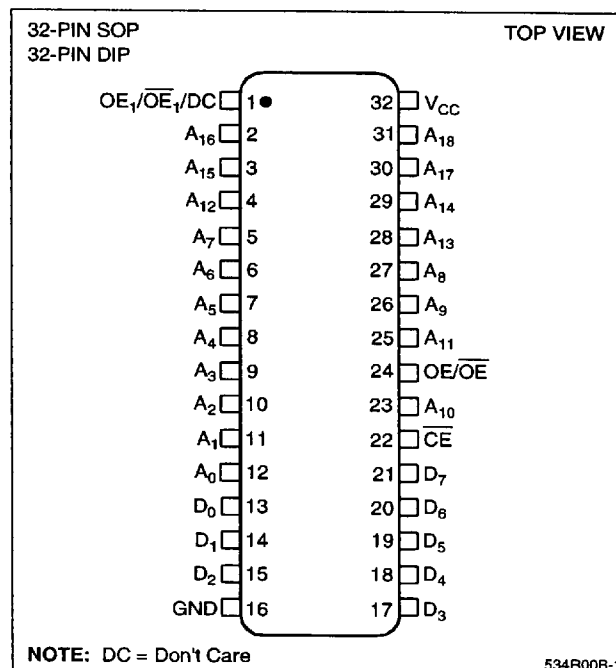


Figure 1. Pin Connections

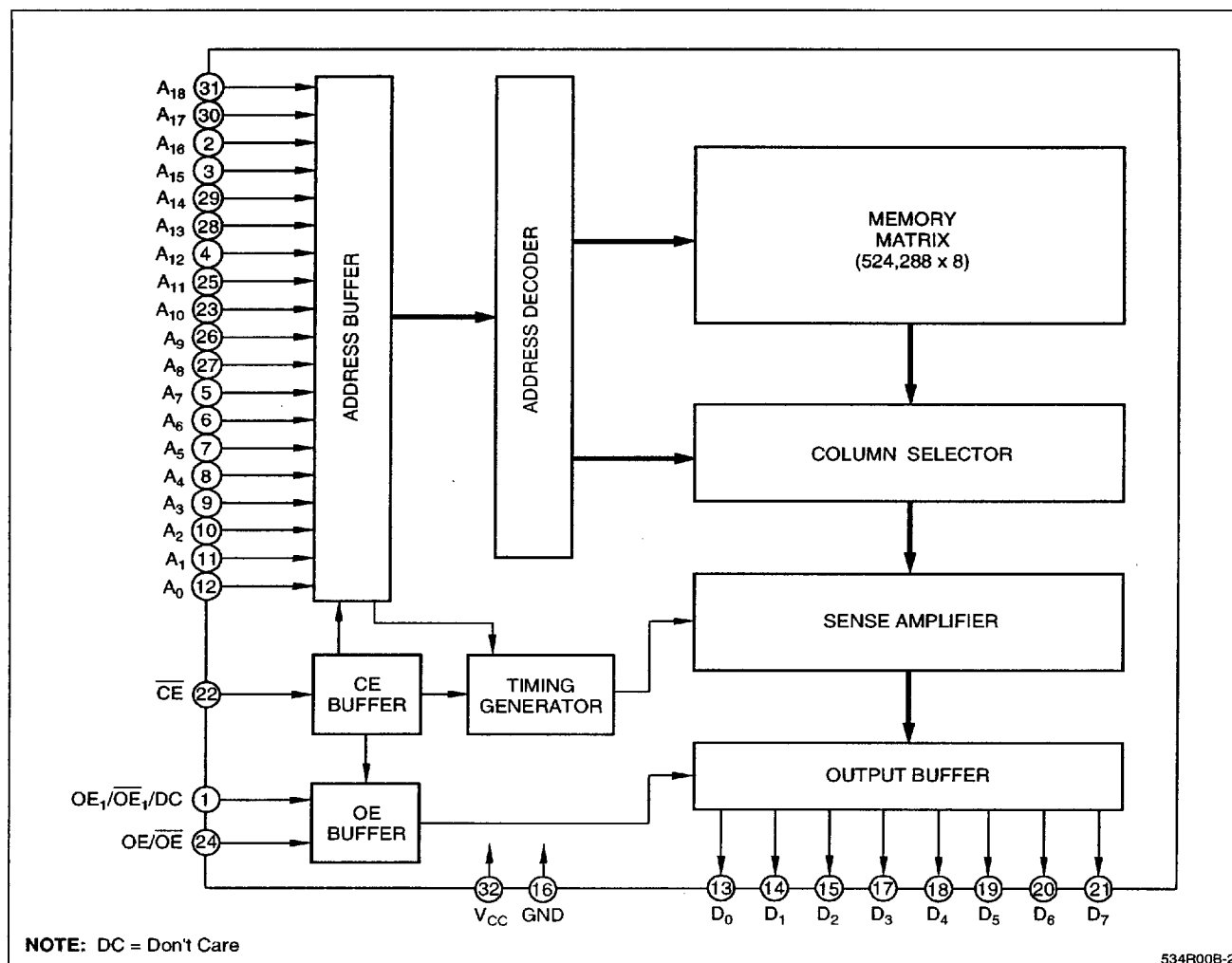


Figure 2. LH534R00B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₈	Address input
D ₀ - D ₇	Data output
$\overline{CE}$	Chip enable input
OE/ $\overline{OE}$	Output enable input

SIGNAL	PIN NAME
OE ₁ / $\overline{OE}_1$ /DC	Output enable input
V _{CC}	Power pin (+5 V)
GND	Ground

NOTES:

- Active levels of OE/ $\overline{OE}$ and OE₁/ $\overline{OE}_1$ /DC are programmable by mask. When the D.C. is selected out of OE₁/ $\overline{OE}_1$ /DC, it is fixed to an active level. (Then it is recommended to apply either "HIGH" or "LOW" to the DC pin.)

TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}_1$	$OE/\overline{OE}$	DATA OUTPUT	SUPPLY CURRENT
H	X	X	High impedance	Standby
L	L/H	X	High impedance	Operating
L	X	L/H	High impedance	Operating
L	H/L	H/L	Output	Operating

NOTE:

X = Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	2.2	$V_{CC} + 0.3$	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4	—	V	—
Output 'Low' voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$	—	0.4	V	—
Input leakage current	$ I_{LI} $	$V_{IN} = 0\text{ V to } V_{CC}$	—	10	μA	—
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to } V_{CC}$	—	10	μA	1
Operating current	I_{CC1}	$t_{RC} = 120\text{ ns}$	—	65	mA	2
	I_{CC2}	$t_{RC} = 1\text{ }\mu\text{s}$	—	50	mA	2
	I_{CC3}	$t_{RC} = 120\text{ ns}$	—	60	mA	3
	I_{CC4}	$t_{RC} = 1\text{ }\mu\text{s}$	—	45	mA	3
Standby current	I_{SB1}	$\overline{CE} = V_{IH}$	—	3	mA	—
	I_{SB2}	$\overline{CE} = V_{CC} - 0.2\text{ V}$	—	100	μA	—
Input capacitance	C_{IN}	$f = 1\text{ MHz, } T_A = 25^\circ\text{C}$	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:

- $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$ or $OE = V_{IL}$, $\overline{OE}_1 = V_{IH}$ or $OE_1 = V_{IL}$
- $V_{IN} = V_{IH}$ or V_{IL} , $\overline{CE} = V_{IL}$, output is open
- $V_{IN} = (V_{CC} - 0.2\text{ V})$ or 0.2 V , $\overline{CE} = 0.2\text{ V}$, output is open

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Output enable delay time	t_{OE}	—	60	ns	—
Output hold time	t_{OH}	0	—	ns	—
Output floating time	t_{CHZ}	—	60	ns	1
	t_{OHZ}	—	60	ns	

NOTE:

1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V - 2.6 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

NOTE:

It is recommended that a decoupling capacitor be connected between V_{CC} and GND pin.

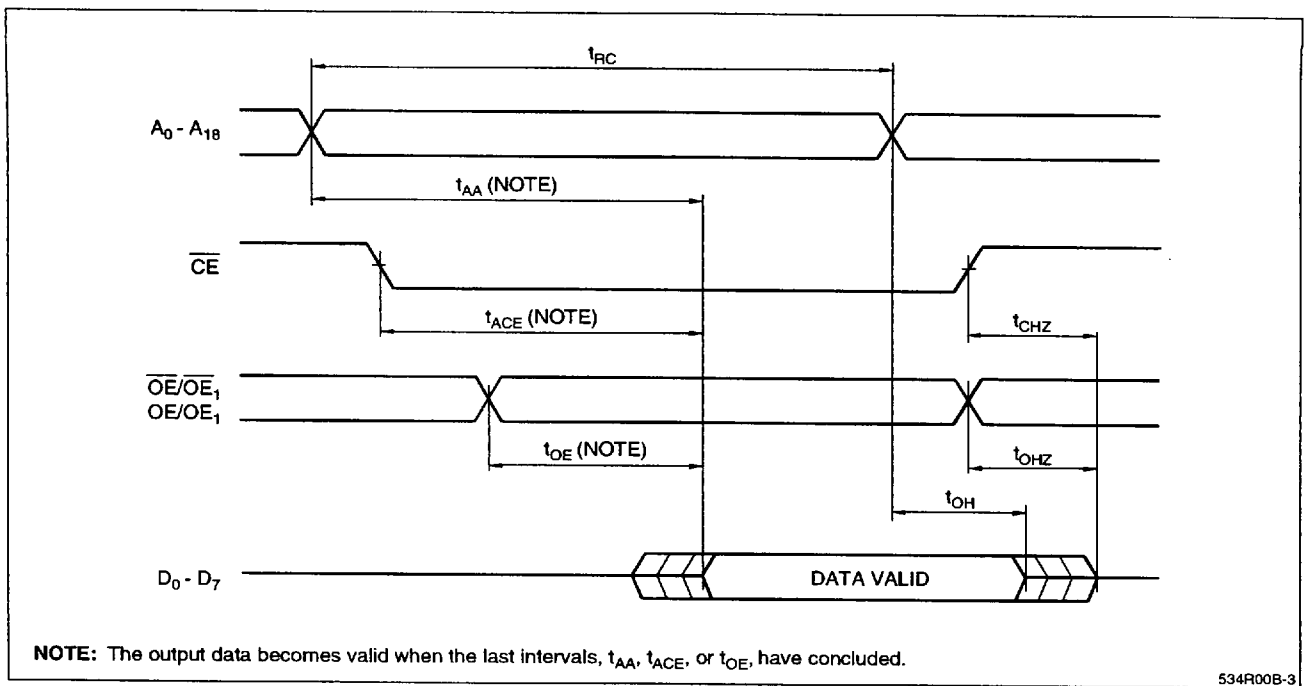
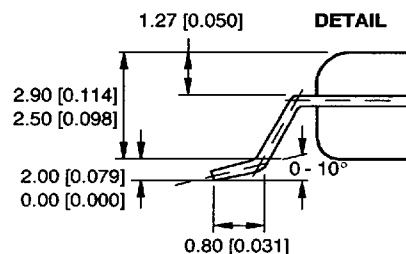
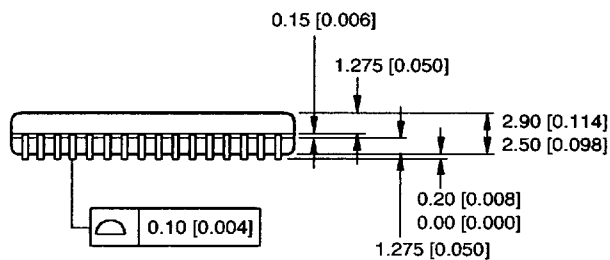
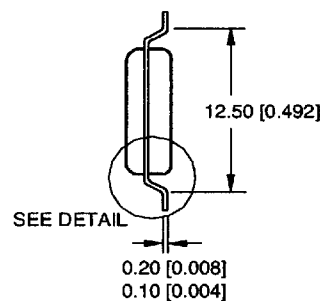
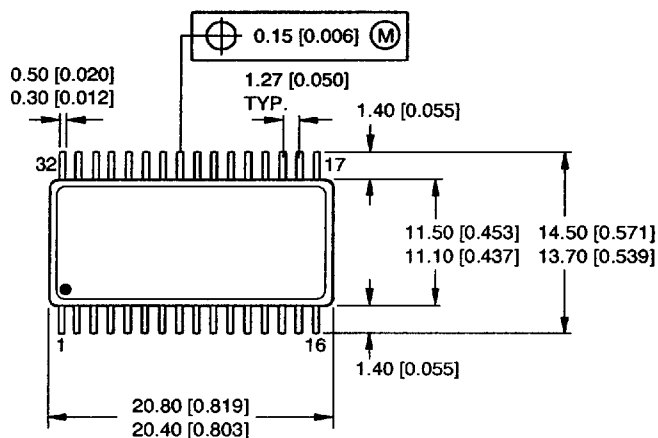


Figure 3. Timing Chart

PACKAGE DIAGRAM

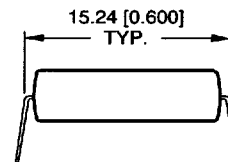
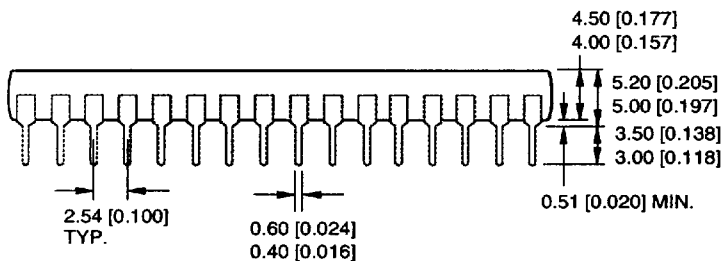
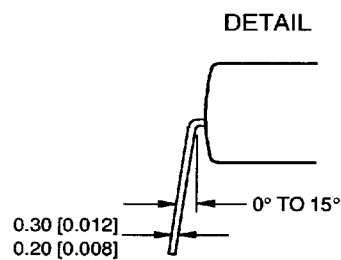
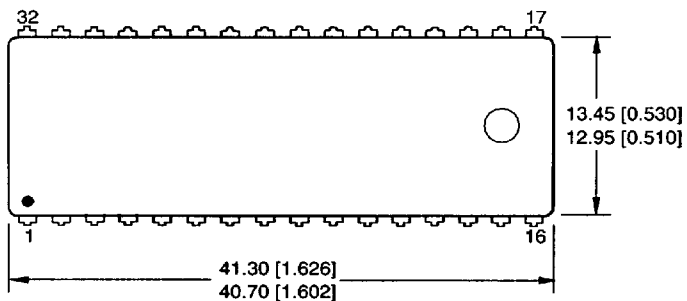
32SOP (SOP32-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

32SOP-2

32DIP (DIP032-P-0600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

32DIP

ORDERING INFORMATION

