LH53BV32R00

CMOS 32M (2M × 16/1M × 32) MROM

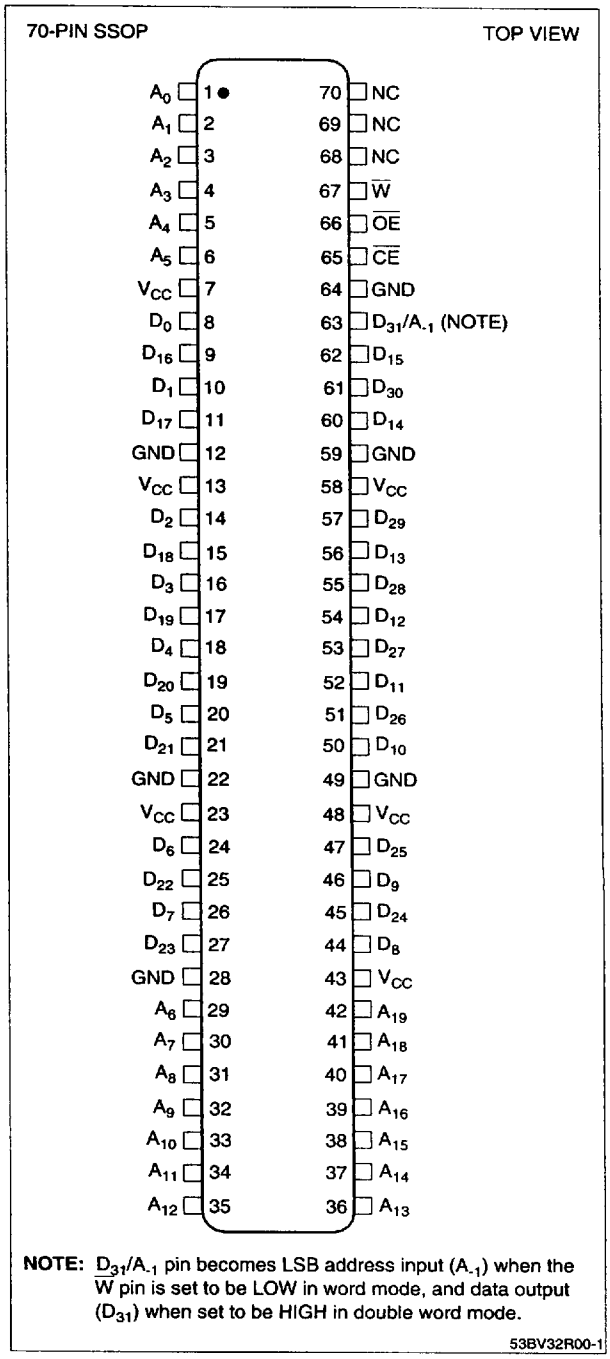
FEATURES

- 2,097,152 × 16 bit organization
  (Word mode: W = V_{IL})
  1,048,576 × 32 bit organization
  (Double Word mode: W = V_{IH})
- Access time: 120 ns (MAX.)
  Access time in page mode: 50 ns (MAX.)
- Supply current:
  - Operating: 100 mA (MAX.)
  - Standby: 150 µA (MAX.)
- Three-state output
- Input/Output TTL compatible
- Supply voltage: 3.3 V ±0.3 V
- Static operation
- Package:
  70 pin, 500-mil SSOP
- Addressable page: 4 Double words or 8 words
- Others:
  - Non programmable
  - Not designed or rated as radiation hardened
  - CMOS process (P type silicon substrate)

DESCRIPTION

The LH53BV32R00 is a 32M-bit mask-programmable ROM organized as 2,097,152 × 16 bits (Word mode) or 1,048,576 × 32 bits (Double Word mode). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS



NOTE: D_{31}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{W}$ pin is set to be LOW in word mode, and data output (D_{31}) when set to be HIGH in double word mode.

53BV32R00-1

Figure 1. Pin Connections

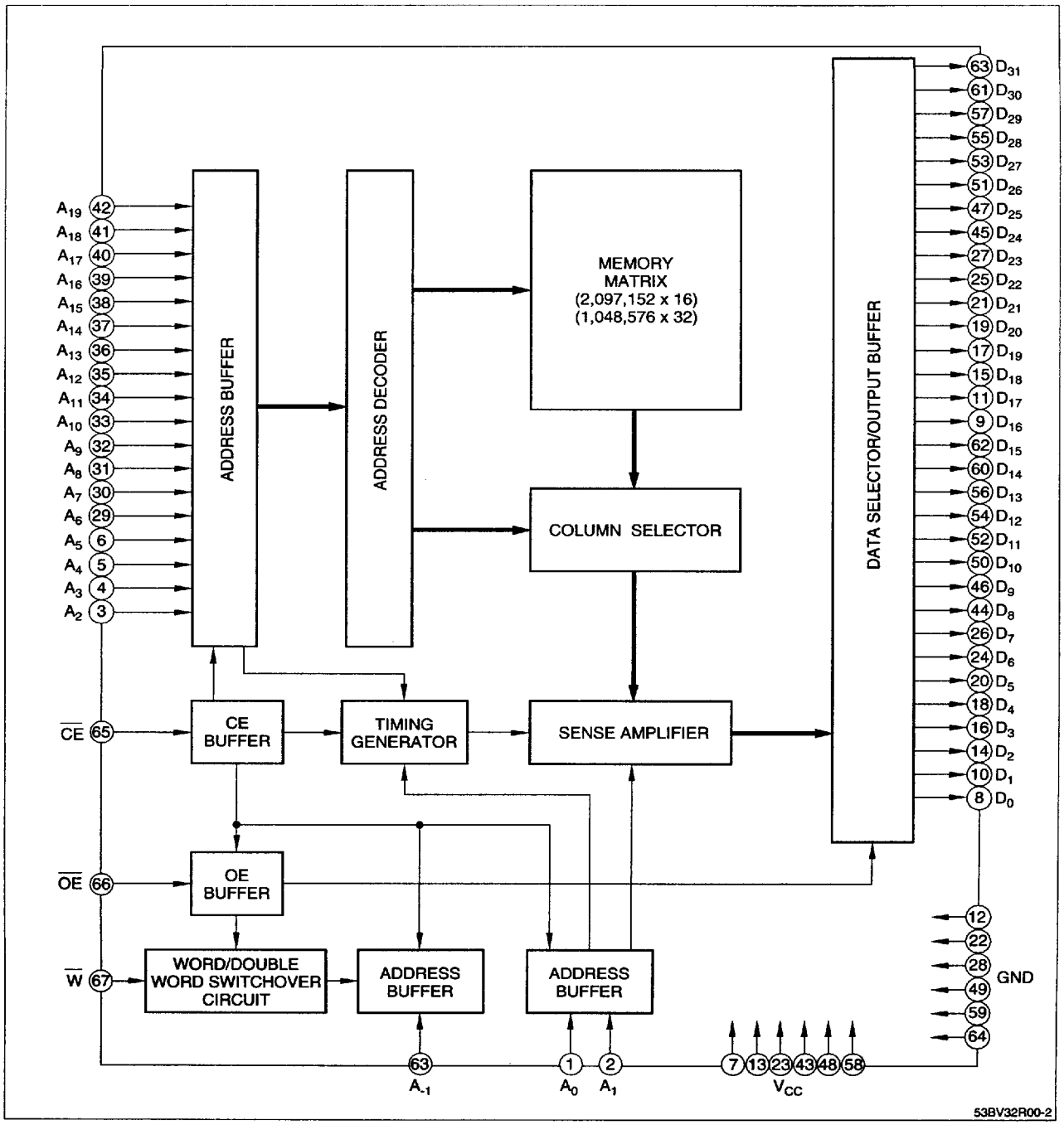


Figure 2. LH53BV32R00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_1	Address input (page mode operation)
A_2 - A_{19}	Address input
D_0 - D_{31}	Data output
W	×16bit/×32 bit (word/double word) mode select input

SIGNAL	PIN NAME
CE	Chip enable input
OE	Output enable input
V_{CC}	Power supply (+3.3 V)
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{W}$	A_{-1} (D_{31})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_{15}	D_{16} - D_{31}	LSB	MSB	
H	X	X	X	High-Z	High-Z	—	—	Standby
L	H	X	X	High-Z	High-Z	—	—	Operating
L	L	H	—	D_0 - D_{15}	D_{16} - D_{31}	A_0	A_{19}	Operating
L	L	L	L	D_0 - D_{15}	High-Z	A_{-1}	A_{19}	Operating
L	L	L	H	D_{16} - D_{31}	High-Z	A_{-1}	A_{19}	Operating

NOTES:
X = Don't care; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +4.6	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	3.0	—	3.6	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	2.0	V_{CC} + 0.3	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4	—	V	—
Output 'Low' voltage	V_{OL}	I_{OL} = 1.6 mA	—	0.4	V	—
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}	—	10	µA	—
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}	—	10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns	—	100	mA	2
Standby current	I_{SB1}	CE = V_{IH}	—	2	mA	—
	I_{SB2}	CE = V_{CC} - 0.2 V	—	150	µA	—
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:
1. CE = V_{IH}, OE = V_{IH}
2. V_{IN} = V_{IH}, V_{IL}, CE = V_{IL}, output is open

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Page address access time	t_{APA}	—	50	ns	—
Output enable delay time	t_{OE}	—	50	ns	—
Output hold time	t_{OH}	5	—	ns	—
Output floating time	t_{CHZ}	—	40	ns	1
	t_{OHZ}	—	40	ns	1

NOTE:
1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.4 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input/Output reference level	1.4 V
Output load condition	1TTL + 100 pF

NOTE:
It is recommended that a decoupling capactor be connected between V_{CC} and GND pin.

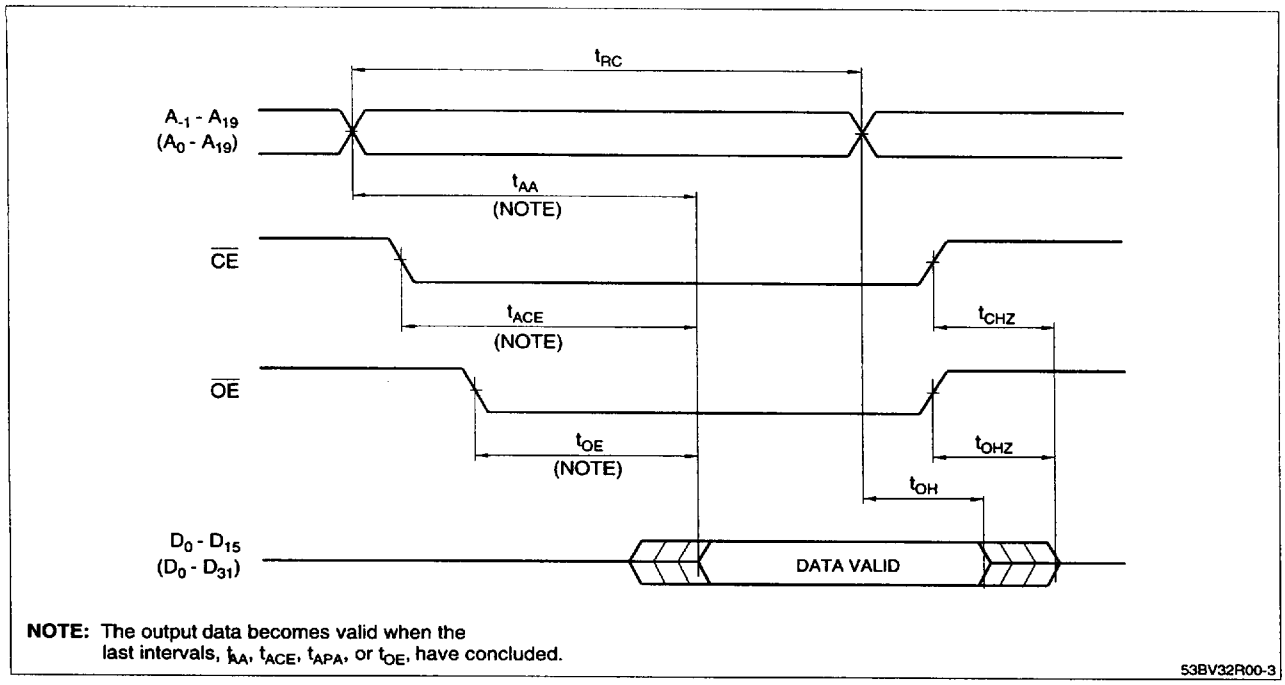


Figure 3. Read Cycle

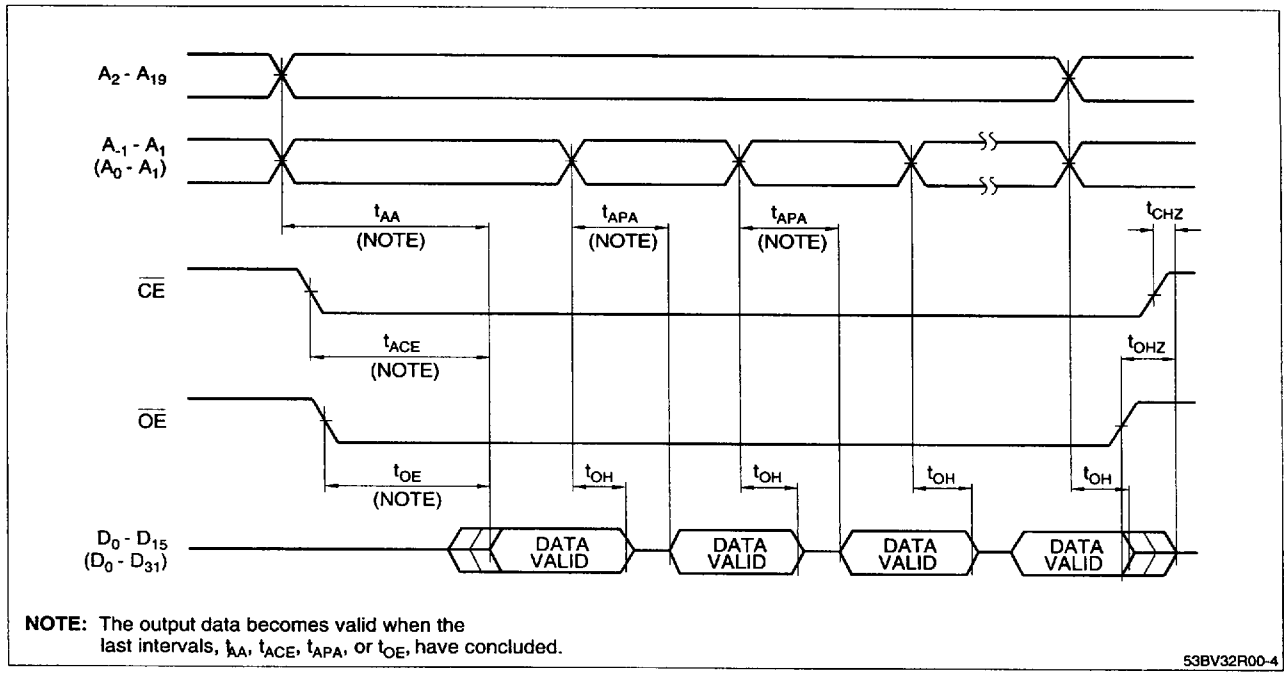
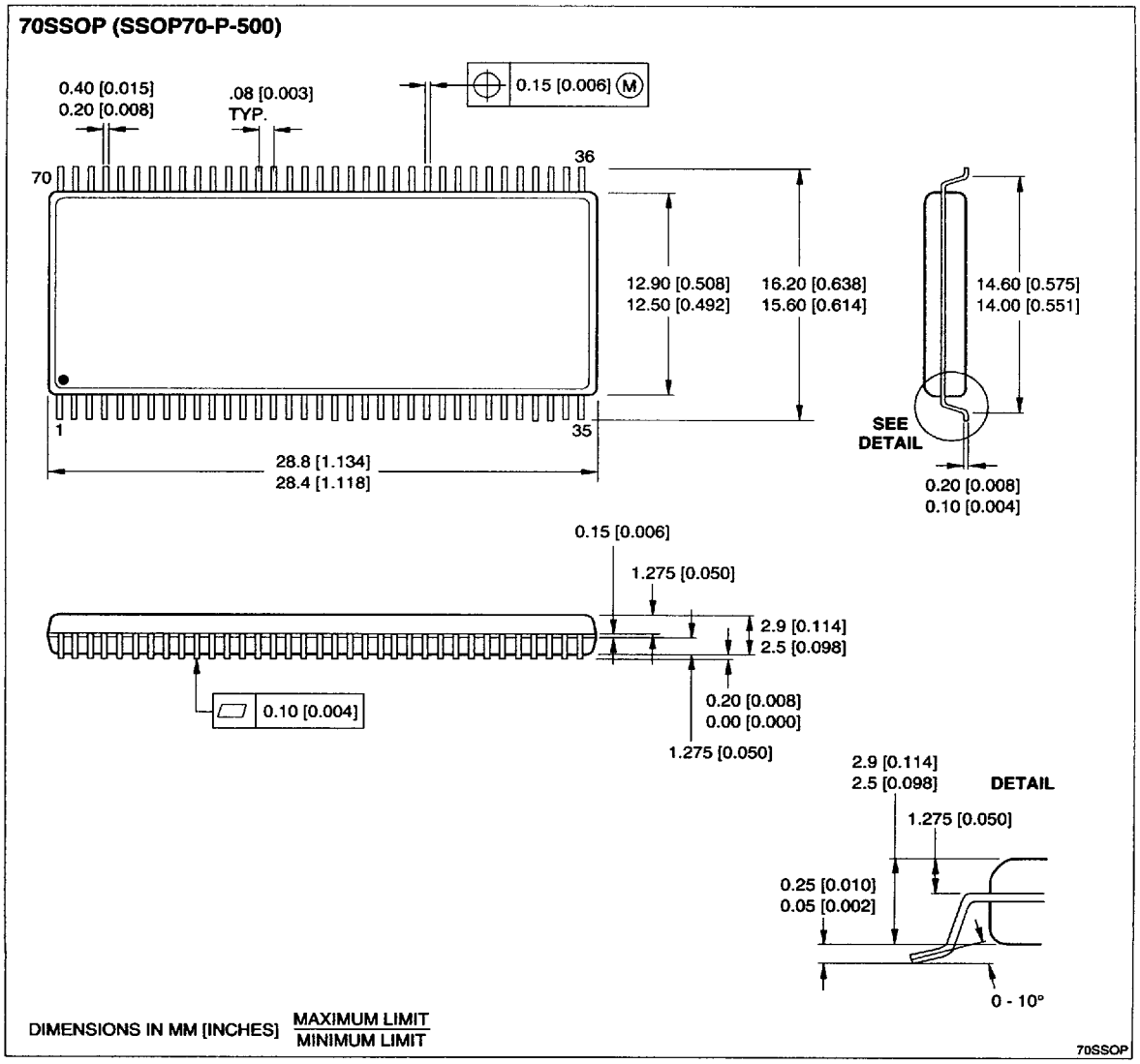


Figure 4. Page Mode Read Cycle

PACKAGE DIAGRAM



ORDERING INFORMATION