ANALOG DEVICES

12-Bit Serial Daisy-Chain CMOS D/A Converter

DAC-8143

FEATURES

- Fast, Flexible, Microprocessor Interfacing in Serially-Controlled Systems
- Buffered Digital Output-Pin for Daisy-Chaining Multiple DACs
- Minimizes Address-Decoding in Multiple DAC Systems – Three Wire Interface for Any Number of DACs
  - One Data Line
  - One CLK Line
  - One Load Line
- Improved Resistance to ESD
- –40°C to +85°C for the Extended Industrial Temperature Range
- Available in Die Form

APPLICATIONS

- Multiple-Channel Data Acquisition Systems
- Process Control and Industrial Automation
- Test Equipment
- Remote Microprocessor-Controlled Systems

ORDERING INFORMATION †

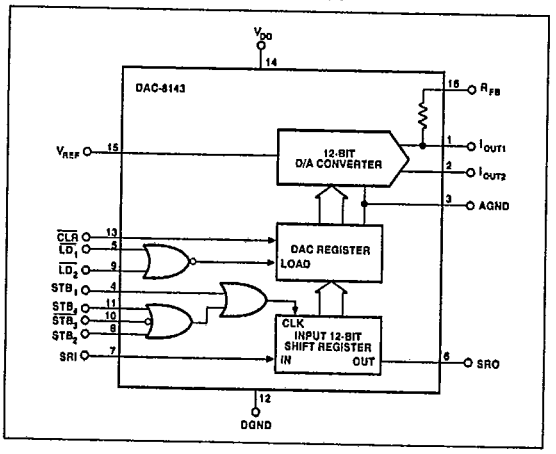
		PACKAGE: 16-PIN	
NON-LINEARITY	GAIN ERROR	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	±1 LSB	DAC8143AQ	DAC8143EQ
±1/2 LSB	±1 LSB	DAC8143AQ/883	–
±1 LSB	±2 LSB	–	DAC8143FP
±1 LSB	±2 LSB	–	DAC8143FS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL BLOCK DIAGRAM



GENERAL INFORMATION T-51-09-12

The DAC-8143 is a 12-bit serial-input daisy-chain CMOS D/A converter, which features serial data input and buffered serial data output. It was designed for multiple serial DAC systems, where serially daisy-chaining one DAC after another is greatly simplified.

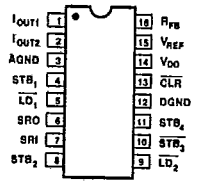
The DAC-8143 also minimizes address decoding lines enabling simpler logic interfacing. It allows 3-wire interface for any number of DACs: one data line, one CLK line, and one load line.

Serial data in the input register (MSB first) is sequentially clocked out to the SRO pin as the new data word (MSB first) is simultaneously clocked in from the SRI pin. The strobe inputs are used to clock in/out data on the rising or falling (user selected) strobe edges (STB_1, STB_2, $\overline{STB_3}$, STB_4).

When the shift register's data has been updated, the new data word is transferred to the DAC register with use of $\overline{LD_1}$ and $\overline{LD_2}$ inputs.

Continued

PIN CONNECTIONS

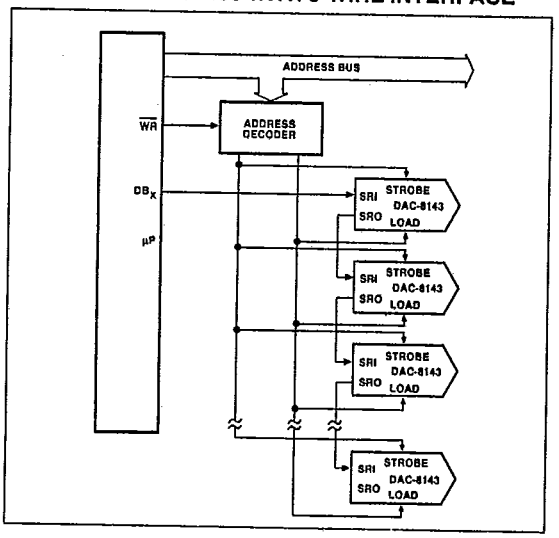


16-PIN EPOXY DIP (P-Suffix)

16-PIN CERDIP (Q-Suffix)

16-PIN SOL (S-Suffix)

MULTIPLE DAC-8143s WITH 3-WIRE INTERFACE



DAC-8143

T-51-09-12

GENERAL INFORMATION *Continued*

Separate LOAD control inputs allow simultaneous output updating of multiple DACs. An asynchronous CLEAR input resets the DAC register without altering data in the input register.

Improved linearity and gain error performance permits reduced circuit parts count through the elimination of trimming components. Also, fast interface timing reduces timing design consideration while minimizing microprocessor wait states.

The DAC-8143 is available in standard cerdip and plastic packages that are compatible with auto-insertion equipment.

Cerdip and plastic packages devices come in the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... +17V
V_{REF} to DGND ..... ±25V
V_{RFB} to DGND ..... ±25V
AGND to DGND ..... V_{DD}+0.3V
DGND to AGND ..... V_{DD}+0.3V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}
Operating Temperature Range
AQ Version ..... –55°C to +125°C
EQ/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
1. Do not apply voltage higher than V_{DD} or less than DGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8143 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	–	–	Bits
Nonlinearity (Note 1)	INL	DAC-8143A/E	–	–	±1/2	LSB
		DAC-8143F	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	DAC-8143A/E	–	–	±1/2	LSB
		DAC-8143F	–	–	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C DAC-8143A/E	–	–	±1	LSB
		DAC-8143F	–	–	±2	
		T_A = Full Temp. Range All Grades	–	–	±2	
Gain Tempco (ΔGain/Δ Temp) (Note 5)	TC_{GFS}		–	–	±5	ppm/°C
Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	±0.0006	±0.002	%/%
Output Leakage Current (Note 4)	I_{LKG}	T_A = +25°C	–	–	±5	nA
		T_A = Full Temp. Range DAC-8143A	–	–	±100	
		DAC-8143E/F	–	–	±25	
Zero Scale Error (Note 7, 12)	I_{ZSE}	T_A = +25°C	–	±0.002	±0.03	LSB
		T_A = Full Temp. Range DAC-8143A	–	±0.05	±0.61	
		DAC-8143E/F	–	±0.01	±0.15	
Input Resistance (Note 8)	R_{IN}	V_{REF} pin	7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8143 MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Output Current Settling Time (Notes 5, 6)	t_s		–	0.380	1	µs
AC Feedthrough Error (V_{REF} to I_{OUT1}) (Notes 5, 11)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz T_A = 25°C	–	–	2.0	mV_{p-p}
Digital to Analog Glitch Energy (Notes 5, 10)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF	–	–	20	nVs
Total Harmonic Distortion (Note 5)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	–	–	-92	dB
Output Noise Voltage Density (Notes 5, 13)	e_n	10Hz to 100kHz between R_{FB} and I_{OUT}	–	–	13	$nV/\sqrt{Hz}$
DIGITAL INPUTS/OUTPUT						
Digital Input HIGH	V_{IH}		2.4	–	–	V
Digital Input LOW	V_{IL}		–	–	0.8	V
Input Leakage Current (Note 9)	I_{IN}	V_{IN} = 0V to +5V	–	–	±1	µA
Input Capacitance (Note 5)	C_{IN}	V_{IN} = 0V	–	–	8	pF
Digital Output High	V_{OH}	I_{OH} = –200µA	4	–	–	V
Digital Output Low	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = all 1s Digital Inputs = all 0s	– –	– –	90 90	pF
Output Capacitance (Note 5)	C_{OUT1} C_{OUT2}	Digital Inputs = all 0s Digital Inputs = all 1s	– –	– –	60 60	pF
TIMING CHARACTERISTICS (Note 5)						
Serial Input to Strobe Setup Times (t_{STB} = 80ns)	t_{DS1}	STB_1 used as the strobe	50	–	–	ns
	t_{DS2}	STB_2 used as the strobe	20	–	–	
	t_{DS3}	STB_3 used as the strobe T_A = +25°C T_A = Full Temp. Range	10 20	– –	– –	
	t_{DS4}	STB_4 used as the strobe	20	–	–	
Serial Input to Strobe Hold Times (t_{STB} = 80ns)	t_{DH1}	STB_1 used as the strobe T_A = +25°C T_A = Full Temp. Range	40 50	– –	– –	ns
	t_{DH2}	STB_2 used as the strobe T_A = +25°C T_A = Full Temp. Range	50 60	– –	– –	
	t_{DH3}	STB_3 used as the strobe	80	–	–	
	t_{DH4}	STB_4 used as the strobe	80	–	–	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

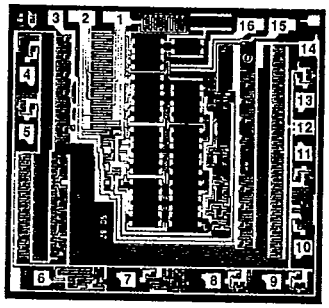
PARAMETER	SYMBOL	CONDITIONS	DAC-8143 MIN	TYP	MAX	UNITS
STB to SRO Propagation Delay (Note 15)	t_{PD}	T_A = 25°C T_A = Full Temp. Range	– –	– –	220 300	ns
SRI Data Pulse Width	t_{SRI}		100	–	–	ns
STB_1 Pulse Width ($\overline{STB_1}$ = 80ns) (Note 14)	t_{STB1}		80	–	–	ns
STB_2 Pulse Width ($\overline{STB_2}$ = 100ns) (Note 14)	t_{STB2}		80	–	–	ns
STB_3 Pulse Width ($\overline{STB_3}$ = 80ns) (Note 14)	t_{STB3}		80	–	–	ns
STB_4 Pulse Width ($\overline{STB_4}$ = 80ns) (Note 14)	t_{STB4}		80	–	–	ns
Load Pulse Width	t_{LD1}, t_{LD2}	T_A = +25°C T_A = Full Temp. Range	140 180	– –	– –	ns
LSB Strobe into Input Register to Load DAC Register Time	t_{ASB}		0	–	–	ns
CLR Pulse Width	t_{CLR}		80	–	–	ns
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All Digital Inputs = V_{IH} or V_{IL} All Digital Inputs = 0V or V_{DD}	– –	– –	2 0.1	mA
Power Dissipation	P_D	Digital Inputs = 0V or V_{DD} 5V x 0.1mA Digital Inputs = V_{IH} or V_{IL} 5V x 2mA	– –	– –	0.5 10	mW

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT1}; all digital inputs = V_{IL}, V_{REF} = +10V; Specification also applies for I_{OUT2} when all digital inputs = V_{IH}
5. Guaranteed by design and not tested.
6. I_{OUT1} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: ts = propagation delay (t_{PD}) +9τ, where τ equals measured time constant of the final RC decay.
7. V_{REF} = +10V, all digital inputs = 0V.
8. Absolute temperature coefficient is less than +300ppm/°C.
9. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
10. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
11. All digital inputs = 0V.
12. Calculated from worst case R_{REF}:
    I_{ZSE} (in LSBs) = (R_{REF} x I_{LKG} x 4096) / V_{REF}.
13. Calculations from $e_n = \sqrt{4K\,TRB}$ where:
    K = Boltzmann constant, J/°KR = resistance Ω
    T = resistor temperature, °K B = bandwidth, Hz
14. Minimum low time pulse width for STB_1, STB_2, and STB_4, and minimum high time pulse width for STB_3.
15. Measured from active strobe edge (STB) to new data output at SRO; C_L =50pF.

DICE CHARACTERISTICS

T-51-09-12



DIE SIZE 0.099 x 0.107 inch, 10,543 sq. mils
(2.51 x 2.72 mm, 6.83 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. $\overline{STB_1}$
5. $\overline{LD_1}$
6. SR0
7. SRI
8. $\overline{STB_2}$
9. $\overline{LD_2}$
10. $\overline{STB_3}$
11. $\overline{STB_4}$
12. DGND
13. $\overline{CLR}$
14. V_{DD} (Substrate)
15. V_{REF}
16. R_{FB}

Substrate (die backside) is internally connected to V_{DD}.

For additional DICE information, refer to 1990/91 Data Book, Section 2.

2

WAFER TEST LIMITS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	DAC-8143G LIMITS	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	±2	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I_{OUT1})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{IN}	V_{REF} pad	7/15	kΩ MIN/MAX
DIGITAL INPUTS/OUTPUT				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	µA MAX
Digital Output HIGH	V_{OH}	I_{OH} = –200µA	4	V MIN
Digital Output LOW	V_{OL}	I_{OL} = 1.6mA	0.4	V MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2.0 0.1	mA MAX

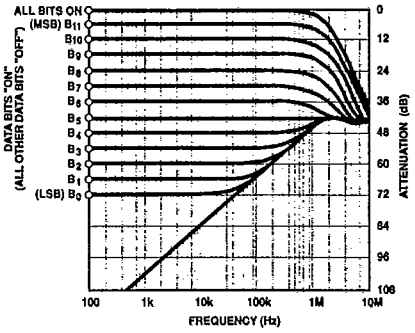
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

DAC-8143

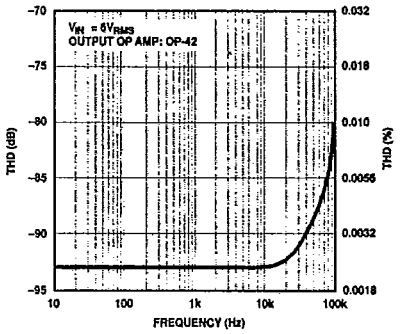
TYPICAL PERFORMANCE CHARACTERISTICS

T-51-09-12

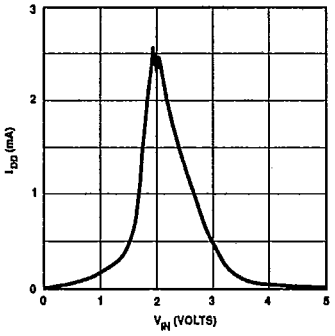
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



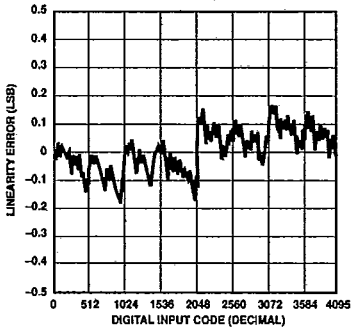
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



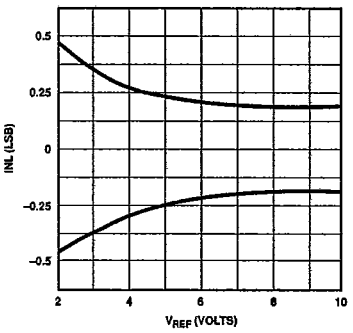
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



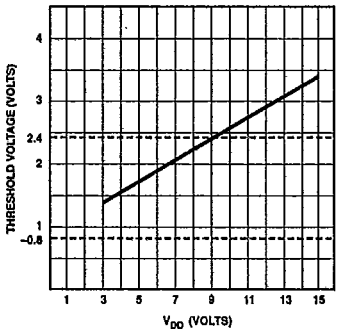
LINEARITY ERROR vs DIGITAL CODE



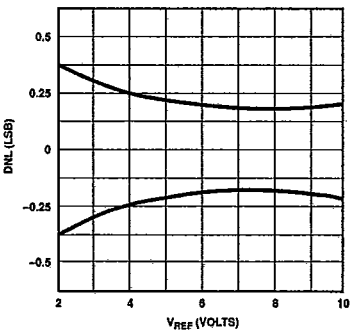
LINEARITY ERROR vs REFERENCE VOLTAGE



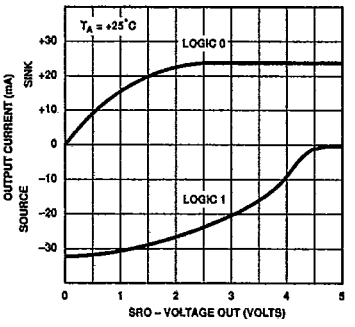
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



DIGITAL OUTPUT VOLTAGE vs OUTPUT CURRENT



SPECIFICATION DEFINITIONS

RESOLUTION
The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME
Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e., zero to full-scale.

GAIN
Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR
Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches off.

OUTPUT CAPACITANCE
Capacitance from I_{OUT1} to ground.

OUTPUT LEAKAGE CURRENT
Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

Refer to PMI 1988 Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT INFORMATION

The DAC-8143 is a 12-bit serial-input, buffered serial-output, multiplying CMOS D/A converter. It has an R-2R resistor ladder network, a 12-bit input shift register, 12-bit DAC register, control logic circuitry, and a buffered digital output stage.

The control logic forms an interface in which serial data is loaded, under microprocessor control, into the input shift register and then transferred, in parallel, to the DAC register. In addition, buffered serial output data is present at the SRO pin when input data is loaded into the input register. This buffered data follows the digital input data (SRI) by 12 clock cycles and is available for daisy-chaining additional DACs.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

A simplified circuit of the DAC-8143 is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistors, and twelve pairs of NMOS current-steering switches. These switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2}. Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It was essential to design these switches such that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10Ω, switch 2 for 20Ω, etc., a constant 5mV drop would then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches were included in series with the feedback resistor and the R-2R ladder's terminating resistor. The Simplified DAC Circuit, Figure 1, shows the location of these switches. These series switches are equivalently scaled to two times switch 1 (MSB) and top switch 12 (LSB) to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

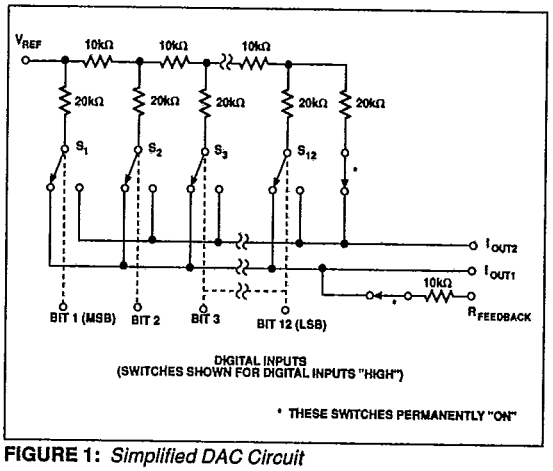


FIGURE 1: *Simplified DAC Circuit*

ESD PROTECTION

The DAC-8143 digital inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes were designed to clamp the inputs well below dangerous levels during static discharge conditions.

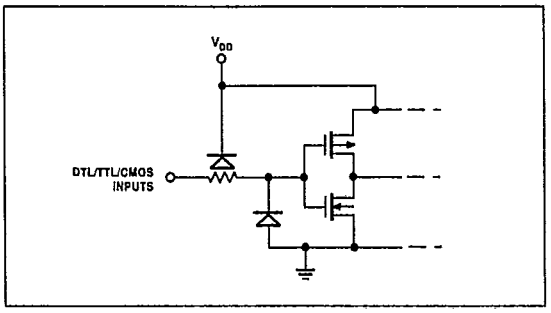


FIGURE 2: *Digital Input Protection*

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC-8143's internal DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW, and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the capacitance of a MOS transistor changes with applied gate voltage. This output capacitance varies between the low and high values.

DYNAMIC PERFORMANCE

ANALOG OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT1} terminal, varies between 11kΩ (the feedback resistor alone when all digital input are LOW) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations.

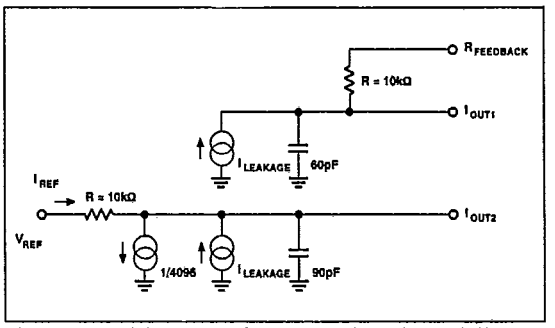


FIGURE 3: *DAC-8143 Equivalent Circuit (All Inputs LOW)*

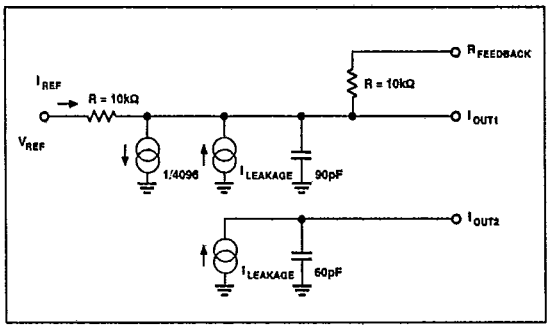


FIGURE 4: *DAC-8143 Equivalent Circuit (All Inputs HIGH)*

The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC-8143. The use of a small compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 7 and 8).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 5-30pF) should be used across the amplifiers to minimize overshoot and ringing. For low speed or static applications,

AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

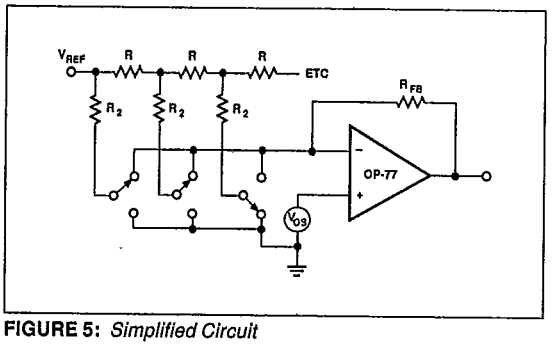


FIGURE 5: *Simplified Circuit*

Where RO is a function of the digital code, and :

R_O = 10kΩ for more than four bits of logic 1,
R_O = 30kΩ for any single bit of logic 1.

Therefore, the offset gain varies as follows:

at code 0011 1111 1111,

$$V_{ERROR_1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\,V_{OS}$$

at code 0100 0000 0000,

$$V_{ERROR_2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3\,V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for V_{REF} = +10V) of 2.4mV for the DAC-8143, it is clearly important that V_{OS} be minimized, using either the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-97, OP-07, OP-27, and OP-42.

INTERFACE LOGIC OPERATION

The microprocessor interface of the DAC-8143 has been designed with multiple STROBE and LOAD inputs to maximize interfacing options. Control signals decoding may be done on-chip or with the use of external decoding circuitry (see Figure 12).

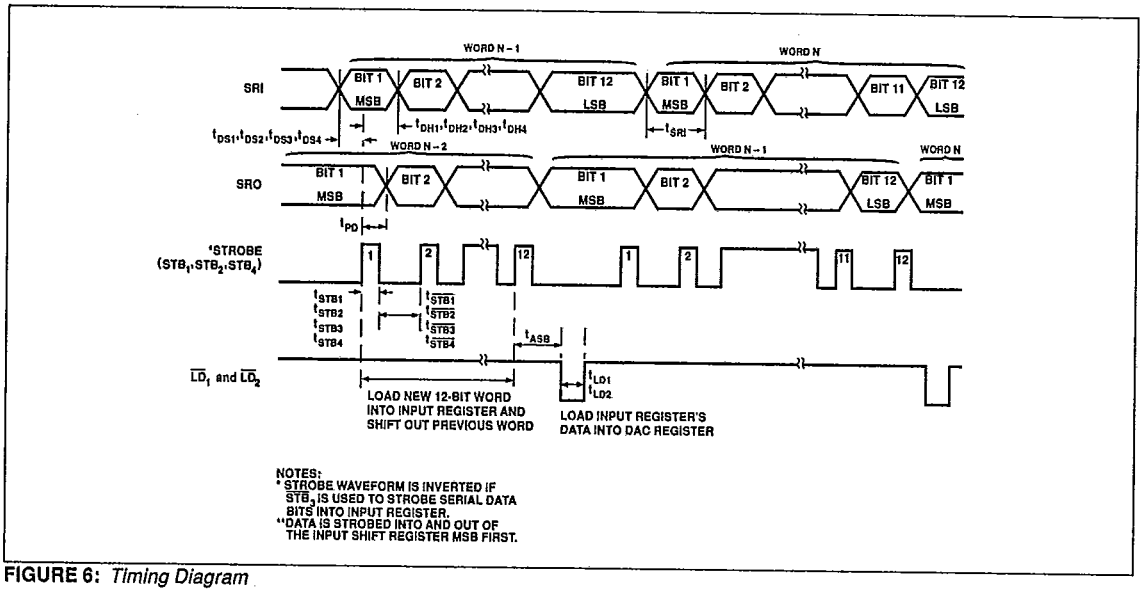


FIGURE 6: *Timing Diagram*

Serial data is clocked into the input register and buffered output stage with STB_1, STB_2, or STB_4. The strobe inputs are active on the rising edge. $\overline{STB_3}$ may be used with a falling edge clock data.

Serial data output (SRO) follows the serial data input (SRI) by 12 clocked bits.

Holding any STROBE input at its selected state (i.e., STB_1, STB_2 or STB_4 at logic HIGH or STB_3 at logic LOW) will act to prevent any further data input.

When a new data word has been entered into the input register, it is transferred to the DAC register by asserting both LOAD inputs.

The $\overline{CLR}$ input allows asynchronous resetting of the DAC register to 0000 0000 0000. This reset does not affect data held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{REF}$.

INTERFACE INPUT DESCRIPTION

STB_1 (Pin 4), STB_2 (Pin 8), STB_4 (Pin 11) – Input Register and Buffered Output Strobe. Inputs Active on Rising Edge. Selected to load serial data into input register and buffered output stage. See Table 1 for details.

$\overline{STB_3}$ (Pin 10) – Input Register and Buffered Output Strobe Input. Active on Falling Edge. Selected to load serial data into input register and buffered output stage. See Table 1 for details.

$\overline{LD_1}$ (Pin 5), $\overline{LD_2}$ (Pin9) – Load DAC Register Inputs. Active Low. Selected together to load contents of input register into DAC register.

$\overline{CLR}$ (Pin 13) – Clear Input. Active Low. Asynchronous. When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

TABLE 1: DAC-8143 Truth Table

DAC-8143 Logic Inputs							DAC-8143 Operation	Notes
Input Register/ Digital Output		Control Inputs		DAC Register	Control Inputs			
STB_4	$\overline{STB_3}$	STB_2	STB_1	$\overline{CLR}$	$\overline{LD_2}$	$\overline{LD_1}$		
0	1	0	↑	X	X	X	Serial Data Bit Loaded from SRI into Input Register and Digital Output (SRO pin) after 12 clocked bits.	2,3
0	1	↑	0	X	X	X		
0	↓	0	0	X	X	X		
↑	1	0	0	X	X	X		
1	X	X	X				No Operation (Input Register and SRO)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Reset DAC Register to Zero Code (Code: 0000 0000 0000) (Asynchronous Operation)	1,3
				1	1	X	No Operation (DAC Register and SRO)	3
				1	X	1		
				1	0	0	Load DAC Register with the Contents of Input Register	3

1. $\overline{CLR}$ = 0 asynchronously resets DAC Register to 0000 0000 0000, but has no effect on Input Register.
2. Serial data is loaded into Input Register MSB first, on edges shown. ↑ is positive edge, ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

APPLICATIONS INFORMATION

UNIPOLAR OPERATON (2-QUADRANT)

The circuit shown in Figures 7 and 8 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and +10(4095/4096)V depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The V_{REF} voltage range is the maximum input voltage range of the op amp or ±25V, whichever is lowest.

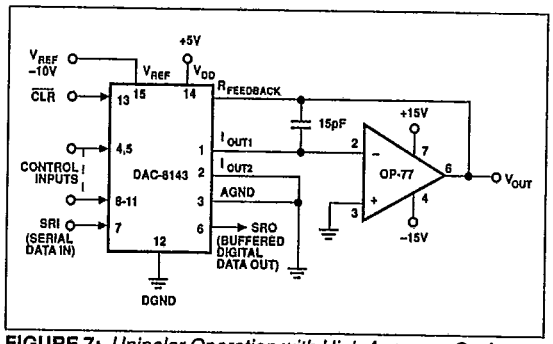


FIGURE 7: *Unipolar Operation with High Accuracy Op Amp (2-Quadrant)*

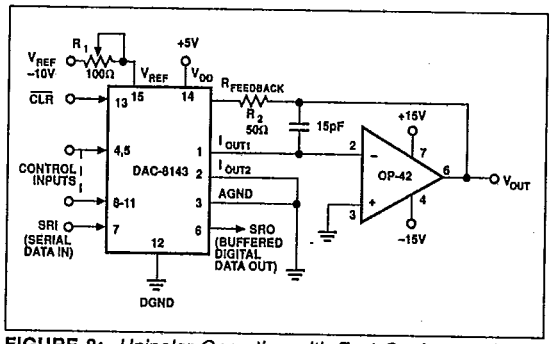


FIGURE 8: *Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)*

In many applications, the DAC-8143's zero scale error and low gain error, permit the elimination of external trimming components without adverse effects on circuit performance.

For applications requiring a tighter gain error than 0.024% at 25°C for the top grade part, or 0.048% for the lower grade part, the circuit in Figure 8 may be used. Gain error may be trimmed by adjusting R_1.

The DAC register must first be loaded with all 1s. R_1 is then adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

2

TABLE 2: Unipolar Code Table

DIGITAL INPUT MSB		LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 7 and 8)
1111	1111	1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000	0000	0001	$-V_{REF}\left(\frac{2049}{4096}\right)$
1000	0000	0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0111	1111	1111	$-V_{REF}\left(\frac{2047}{4096}\right)$
0000	0000	0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:

1. Nominal full scale for the circuits of Figures 7 and 8 is given by $FS = -V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 7 and 8 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$

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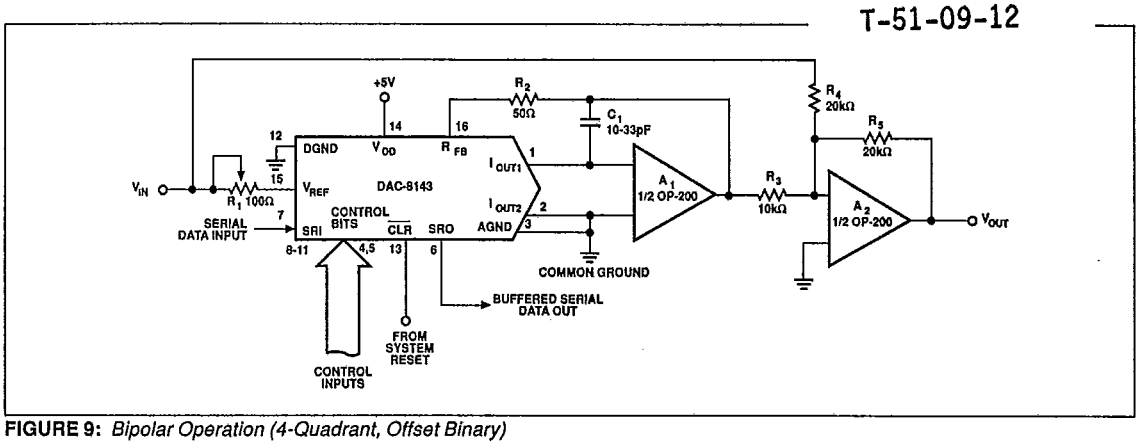

FIGURE 9: *Bipolar Operation (4-Quadrant, Offset Binary)*

BIPOLAR OPERATION (4-QUADRANT)

Figure 9 details a suggested circuit for bipolar, or offset binary operation. Table 3 shows the digital input-to-analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB intput.

Resistor R_3, R_4, and R_5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient match. Mismatching between R_3 and R_4 causes offset and full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until $V_{OUT} = 0V$. R_1 and R_2 may be omitted by adjusting the ratio of R_3 to R_4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and adjusting either the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

DAISY-CHAINING DAC-8143s

Many applications use multiple serial-input DACs that use numerous inter-connecting lines for address decoding and data

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB			LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 9)
1111	1111	1111		$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001		$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000		0
0111	1111	1111		$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0001		$-V_{REF}\left(\frac{2047}{2048}\right)$
0000	0000	0000		$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:

1. Nominal full scale for the circuits of Figure 9 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuits of Figure 9 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

lines. In addition, they use some type of buffering to reduce loading on the bus. The DAC-8143 is ideal for just such an application. It not only reduces the number of inter-connecting lines, but also reduces bus loading. The DAC-8143 can be daisy-chained with only three lines: one data line, one CLK line, and one Load line, see Figure 10.

ANALOG/DIGITAL DIVISION

The transfer function for the DAC-8143 connect in the multiplying mode as shown in Figures 7 and 8 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 11 and is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1}+\frac{A_2}{2^2}+\frac{A_3}{2^3}+\ldots\frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON" the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1}, I_{OUT2}, and AGND (pins 1, 2 and 3)being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 7 and 8). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than ±200µV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

It is recommended that the digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital input pass through the transition region (see the Supply Current vs. Logic Input Voltage graph under the Typical Performance Characteristics). The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e., rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

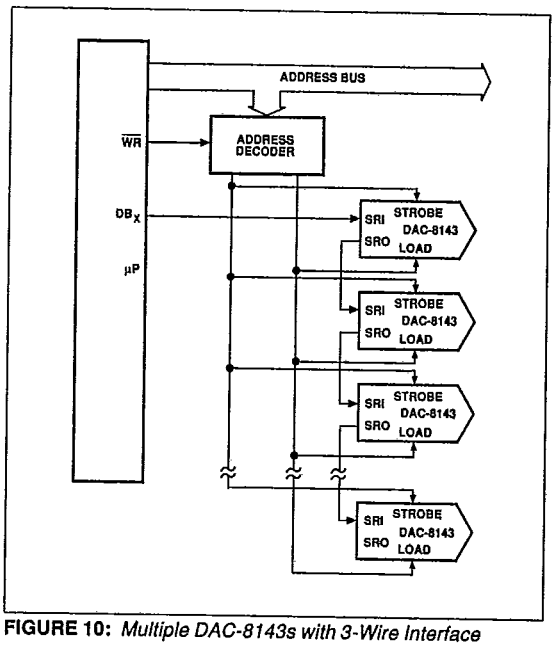

FIGURE 10: *Multiple DAC-8143s with 3-Wire Interface*

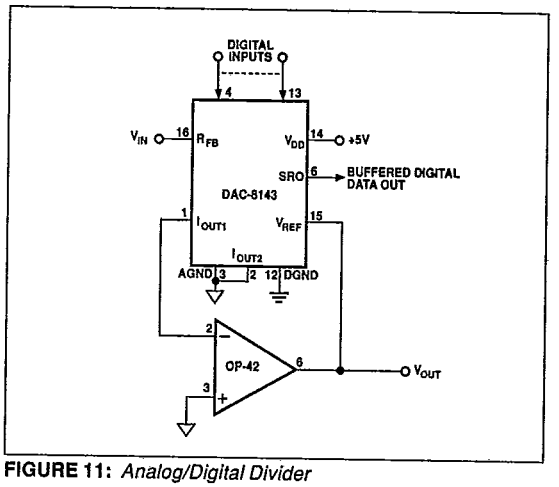

FIGURE 11: *Analog/Digital Divider*

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INTERFACING TO THE MC6800

As shown in Figure 12, the DAC-8143 may be interfaced to the 6800 by successively executing memory WRITE instruction while manipulating the data between WRITEs, so that each WRITE presents the next bit.

In this example, the most significant bits are found in memory locations 0000 and 0001. The four MSBs are found in the lower half of 0000, the eight LSBs in 0001. The data is taken from the DB_7 line.

The serial data loading is triggered by STB_4 which is asserted by a decoded memory WRITE to a memory location, R/$\overline{W}$, and Φ2. A WRITE to another address location transfers data from input register to DAC register.

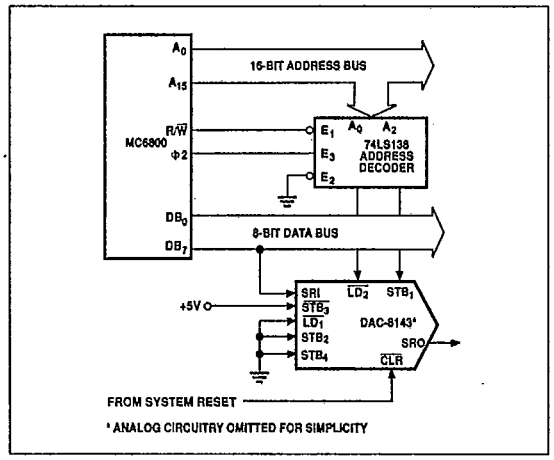

FIGURE 12: *DAC-8143 – MC6800 Interface*

DAC-8143 INTERFACE TO THE 8085

The DAC-8143's interface to the 8085 microprocessor is shown in Figure 13. Note that the microprocessor's SOD line is used to present data serially to the DAC.

Data is strobed into the DAC-8143 by executing memory write instructions. The strobe 2 input is generated by decoding an address location and $\overline{WR}$. Data is loaded into the DAC register with a memory write instruction to another address location.

Serial data supplied to the DAC-8143 must be present in the right-justified format in registers H and L of the microprocessor.

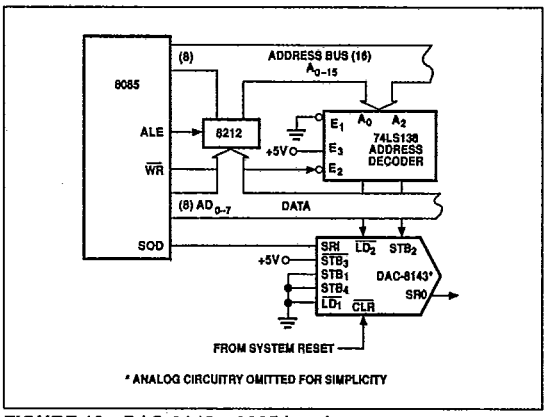

FIGURE 13: *DAC-8143 – 8085 Interface*

DAC-8143 INTERFACE TO THE 68000

Figure 14 shows the DAC-8143 configured to the 68000 microprocessor. Serial data input is similar to that of the 6800 in Figure 12.

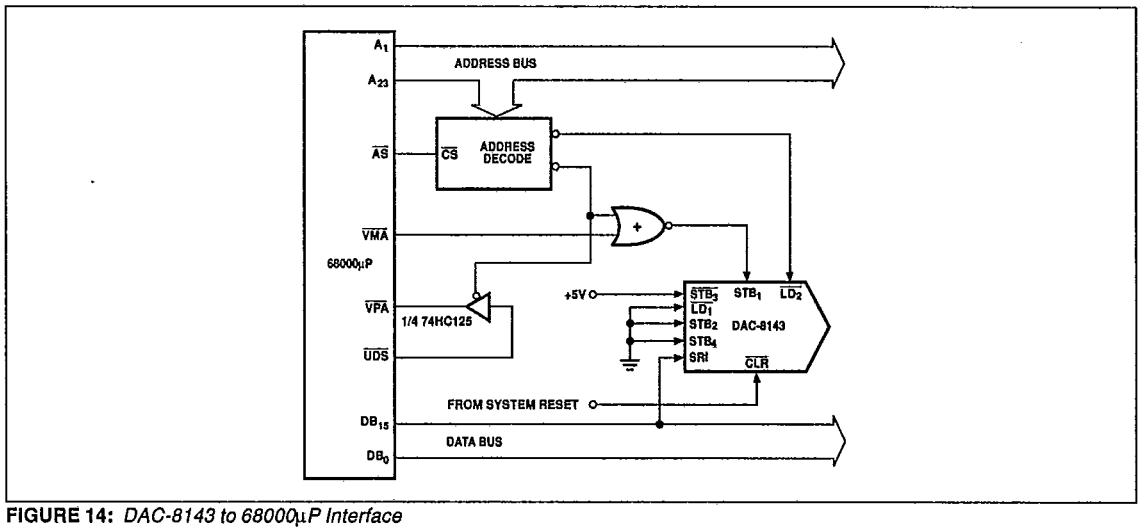

FIGURE 14: *DAC-8143 to 68000μP Interface*