1.1 Scope.

This specification covers the detail requirements for a quad, voltage output, 12-bit BiCMOS DAC with readback. It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number	Package
−1	DAC-8412AT/883	T
−2	DAC-8412BT/883	T
−2	DAC-8412BTC/883	TC
−3	DAC-8413AT/883	T
−4	DAC-8413BT/883	T
−4	DAC-8413BTC/883	TC

1.2.3 Case Outline.

Letter	Case Outline (Lead Finish Per MIL-M-38510)
T	28-Lead Ceramic Dual-in-Line Package (Cerdip)
TC	28-Contact Hermetic Leadless Chip Carrier (LCC)

1.3 Absolute Maximum Ratings.* (T_A = +25°C unless otherwise noted)

V_{SS} to V_{DD} ..... −0.3 V, +33.0 V
V_{SS} to V_{LOGIC} ..... −0.3 V, +23.5 V
V_{DD} to DGND ..... +16.5 V
V_{SS} to DGND ..... −16.5 V
V_{LOGIC} to DGND ..... −0.3 V, +7 V
V_{SS} to V_{REFL} ..... −0.3 V, +V_{DD} − 2.0 V
V_{REFH} to V_{DD} ..... +2.0 V, +33.0 V
V_{REFH} to V_{REFL} ..... +2.0 V, V_{DD} − V_{SS}
Current into Any Pin ..... ±15 mA
Digital Input Voltage to DGND ..... −0.3 V, V_{LOGIC} + 0.3 V
Digital Output Voltage to DGND ..... −0.3 V, +7.0 V
Operating Temperature Range (AT, BT, BTC) ..... −55°C to +125°C
Junction Temperature (T_J) ..... +150°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation ..... 1000 mW
Lead Temperature (Soldering 60 sec) ..... +300°C

*CAUTION: a. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability. b. Analog and digital inputs and outputs are protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures. c. Remove power before inserting or removing units from their sockets.

DAC-8412/DAC-8413—SPECIFICATIONS

Table 1.

Test	Symbol	Device Types	Limits Min	Limits Max	Group A Subgroups	Conditions[1]	Units
Integral Linearity	INL	−1, 3		±3/4	1	T_A = +25°C	LSB
					2, 3	T_A = −55°C, +125°C	
		−2, 4		±1.5	1	T_A = +25°C	LSB
					2, 3	T_A = −55°C, +125°C	
Differential Linearity	DNL	All		±1	1	T_A = +25°C	LSB
					2, 3	T_A = −55°C, +125°C	
Min-Scale Error	V_{ZSE}	All		±2	1	$R_L \geq 2$ kΩ; T_A = +25°C	LSB
					2, 3	$R_L \geq 2$ kΩ; T_A = −55°C, +125°C	
Full-Scale Error	V_{FSE}	All		±2	1	$R_L \geq 2$ kΩ; T_A = +25°C	LSB
					2, 3	$R_L \geq 2$ kΩ; T_A = −55°C, +125°C	
Linearity Matching		All		±1	1	T_A = +25°C	LSB
Min-Scale Offset Matching		All		±1	1	T_A = +25°C	LSB
Full-Scale Offset Matching		All		±2	1	T_A = +25°C	LSB
Reference Input Current	I_{REFH}	All	−2.75	+2.75	1, 2, 3	Code 555_H & 000_H; T_A = +25°C, −55°C, +125°C	mA
	I_{REFL}		0	+2.75	1, 2, 3	Code 555_H & 000_H; T_A = +25°C, −55°C, +125°C	
Output Voltage Swing	$V_{OUT\ (MIN)}$	All	−10.0098	−9.9902	1, 2, 3	T_A = +25°C, −55°C, +125°C; R_L = 2 kΩ	V
	$V_{OUT\ (MAX)}$		+9.9853	+10.0048	1, 2, 3	T_A = +25°C, −55°C, +125°C; R_L = 2 kΩ	
Settling Time[2]	t_S	All		15	9	10 V Step to 0.01%; T_A = +25°C	μs
Logic Input High Voltage	V_{INH}	All	2.4		1	T_A = +25°C	V
					2, 3	T_A = −55°C, +125°C	
Logic Input Low Voltage	V_{INL}	All		0.8	1	T_A = +25°C	V
					2, 3	T_A = −55°C, +125°C	
Logic Output High Voltage	V_{OH}	All	2.4		1	I_{OH} = +0.4 mA; T_A = +25°C	V
					2, 3	I_{OH} = +0.4 mA; T_A = −55°C, +125°C	
Logic Input Low Voltage	V_{OL}	All		0.4	1	I_{OL} = −1.6 mA; T_A = +25°C	V
					2, 3	I_{OL} = −1.6 mA; T_A = −55°C, +125°C	
Logic Input Current	I_{IN}	All		10	1	T_A = +25°C	μA
					2, 3	T_A = −55°C, +125°C	
Slew Rate[2]	SR	All	2		7	T_A = +25°C	V/μs
LOGIC TIMING CHARACTERISTICS[3] WRITE							
Chip Select Write Pulse Width[2]	t_{WCS}	All	90		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Write Setup[2]	t_{WS}	All	0		9	t_{WCS} = 90 ns; T_A = +25°C	ns
					10, 11	t_{WCS} = 90 ns, T_A = −55°C, +125°C	
Write Hold[2]	t_{WH}	All	0		9	t_{WCS} = 90 ns; T_A = +25°C	ns
					10, 11	t_{WCS} = 90 ns; T_A = −55°C, +125°C	
Address Setup[2]	t_{AS}	All	0		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Address Hold[2]	t_{AH}	All	0		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Load Setup[2]	t_{LS}	All	70		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	

Test	Symbol	Device Types	Limits Min	Limits Max	Group A Subgroups	Conditions[1]	Units
WRITE (Continued) Load Hold[2]	t_{LH}	All	30		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Write Data Setup[2]	t_{WDS}	All	20		9	t_{WCS} = 90 ns; T_A = +25°C	ns
					10, 11	t_{WCS} = 90 ns; T_A = −55°C, +125°C	
Write Data Hold[2]	t_{WDH}	All	0		9	t_{WCS} = 90 ns; T_A = +25°C	ns
					10, 11	t_{WCS} = 90 ns; T_A = −55°C, +125°C	
Load Pulse Width[2]	t_{LWD}	All	170		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Reset Pulse Width[2]	t_{RESET}	All	200		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
READ Chip Select Read Pulse Width[2]	t_{RCS}	All	130		9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Read Data Hold[2]	t_{RDH}	All	0		9	t_{RCS} = 130 ns; T_A = +25°C	ns
					10, 11	t_{RCS} = 130 ns; T_A = −55°C, +125°C	
Read Data Setup[2]	t_{RDS}	All	10		9	t_{RCS} = 130 ns; T_A = +25°C	ns
					10, 11	t_{RCS} = 130 ns; T_A = −55°C, +125°C	
Data to Hi Z[2]	t_{DZ}	All		200	9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
Chip Select to Data[2]	t_{CSD}	All		200	9	T_A = +25°C	ns
					10, 11	T_A = −55°C, +125°C	
SUPPLY CHARACTERISTICS Power Supply Sensitivity	PSS	All		150	1	14.25 V≤V_{DD}≤15.75 V; T_A = +25°C	ppm/V
					2, 3	14.25 V≤V_{DD}≤15.75 V; T_A = −55°C, +125	
Power Supply Current	I_{DD}	All		13	1	V_{REFH} = +10 V; T_A = +25°C	mA
					2, 3	V_{REFH} = +10 V; T_A = −55°C, +125	
Negative Supply Current	I_{SS}	All	−10		1	T_A = +25°C	mA
					2, 3	T_A = −55°C, +125	
Logic Supply Current	I_{LOGIC}	All		100	1	T_A = +25°C	µA
Power Dissipation[4]	P_{DISS}	All		345	1	T_A = +25°C	mW
					2, 3	T_A = −55°C, +125	

NOTES
[1]All supplies can be varied ±5% and operation is guaranteed. V_{DD} = +15 V, V_{SS} = −15 V, V_{LOGIC} = +5 V, V_{REFH} = +10 V, V_{REFL} = −10 V.
[2]Guaranteed but not 100% tested.
[3]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[4]Power dissipation (P_{DISS}) guaranteed by supply current testing.

1.4 Recommended Operating Conditions.

Supply Voltage Range . . . . . ±15 V
Logic Supply Voltage . . . . . +5 V
Positive Reference Voltage (V_{REFH}) . . . . . +2.5 V to +10 V
Negative Reference Voltage (V_{REFL}) . . . . . −10 V to 0 V
Ground Potential (GND) . . . . . 0 V
Ambient Operating Temperature Range (T_A) . . . . . −55°C to +125°C

1.5 Thermal Characteristics.[1]

Thermal Resistance, Cerdip (T) Package:
Junction-to-Case (θ_{JC}) = 7°C/W max
Junction-to-Ambient (θ_{JA}) = 50°C/W max

Thermal Resistance, LCC (TC) Package:
Junction-to-Case (θ_{JC}) = 28°C/W max
Junction-to-Ambient (θ_{JA}) = 70°C/W max

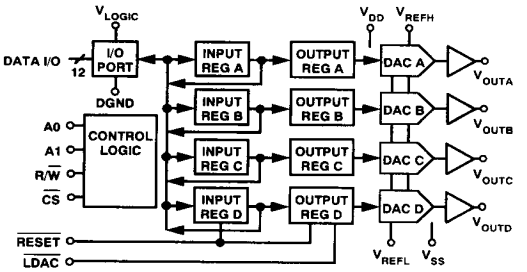
NOTE
[1]θ_{JA} is specified for device in socket for cerdip and mounted to PC board for LCC.

Table 2. Electrical Test Requirements

MIL-STD-883 Test Requirements	Group A Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1,* 2, 3
Group A Test	1, 2, 3, 7, 9, 10, 11

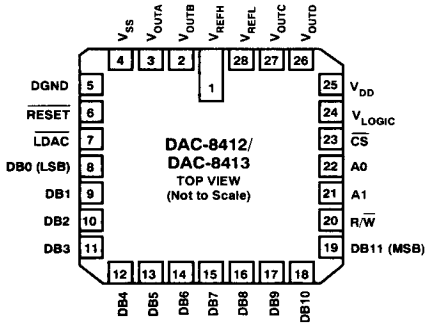
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

3.2.1 Functional Block Diagram and Terminal Assignments.



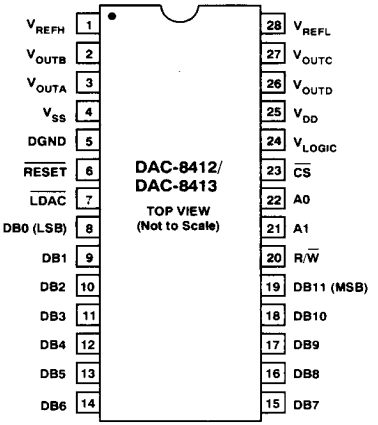
28-Position LCC

(TC Suffix)



28-Pin Ceramic DIP

(T Suffix)

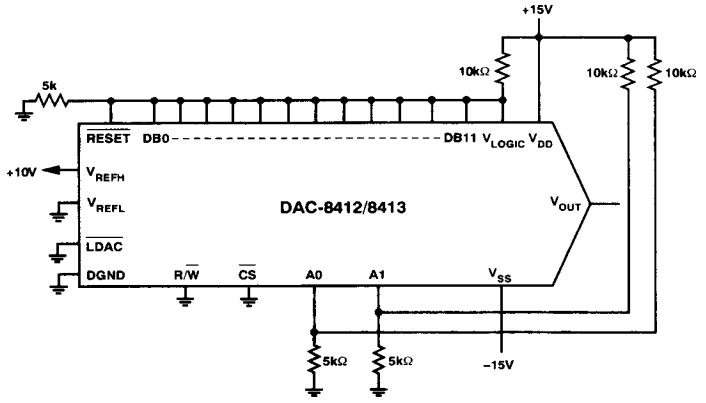


3.2.4 Microcircuit Technology Group.

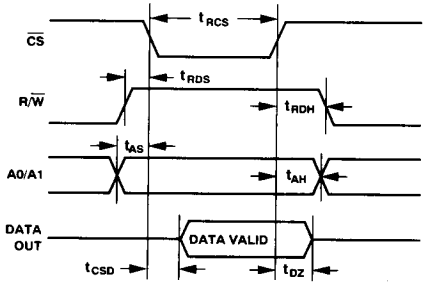
This microcircuit is covered by technology group (92).

4.2.1 Life Test/Burn-In Circuit.

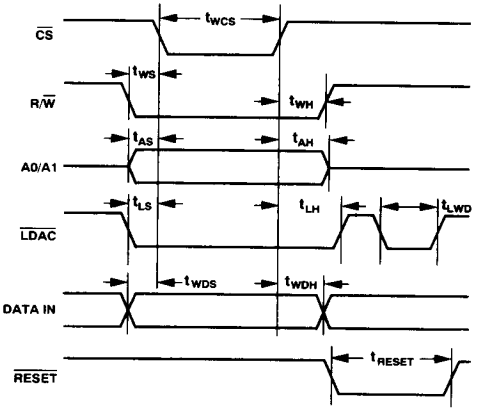
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (C).



4.3 AC Timing Diagram



Data Output (Read Timing)



Data Write (Input and Output Registers) Timing

Table 3. Logic Table

A1	A0	R/$\overline{W}$	$\overline{CS}$	$\overline{RS}$	$\overline{LDAC}$	INPUT REG	INPUT REG	MODE	DAC
L	L	L	L	H	L	WRITE	WRITE	WRITE	A
L	H	L	L	H	L	WRITE	WRITE	WRITE	B
H	L	L	L	H	L	WRITE	WRITE	WRITE	C
H	H	L	L	H	L	WRITE	WRITE	WRITE	D
L	L	L	L	H	H	WRITE	HOLD	WRITE INPUT	A
L	H	L	L	H	H	WRITE	HOLD	WRITE INPUT	B
H	L	L	L	H	H	WRITE	HOLD	WRITE INPUT	C
H	H	L	L	H	H	WRITE	HOLD	WRITE INPUT	D
L	L	H	L	H	H	READ	HOLD	READ INPUT	A
L	H	H	L	H	H	READ	HOLD	READ INPUT	B
H	L	H	L	H	H	READ	HOLD	READ INPUT	C
H	H	H	L	H	H	READ	HOLD	READ INPUT	D
X	X	X	H	H	L	HOLD	Update All Output Registers		All
X	X	X	H	H	H	HOLD	HOLD	HOLD	All
X	X	X	X	L	X	*All Registers Reset to Mid/Zero Scale			All
X	X	X	H	↓	X	*All Registers Latched to Mid/Zero Scale			All

*DAC-8412 resets to mid-scale, and DAC-8413 resets to zero scale.
L is a logic Low; H is a logic High; X is don't care.