DAC-UP8B
8-Bit Monolithic D/A Converter with Input Register

DATEL

FEATURES

- **Input register**
- **Internal reference**
- **Voltage output**
- **Low cost**
- **8-Bit resolution**

GENERAL DESCRIPTION

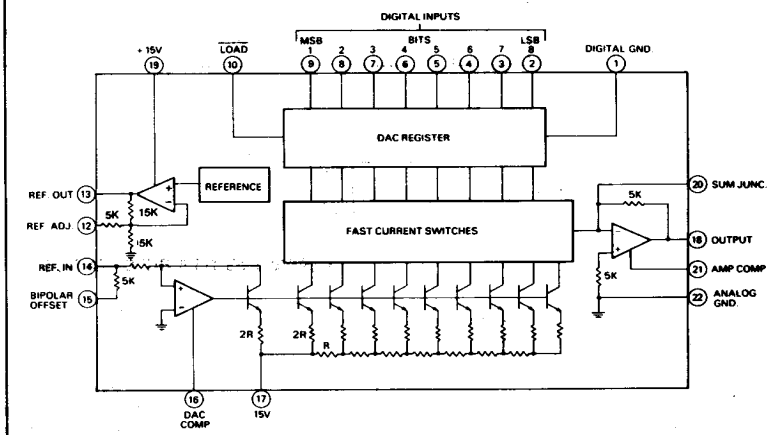
The DAC-UP8BC and DAC-UP8BM are 8-bit monolithic DAC's with internal registers. Contained in the 22-pin DIP is an 8-bit DAC, stable reference, a high-speed output amplifier and an 8-bit input latch. These microprocessor-compatible converters are ideal for low-cost applications.

The output voltage range is 0 to +10V for unipolar mode and ±5V for bipolar. Typical settling time is 2 microseconds for a full-scale change. Either the internal reference or an external reference can be used to bias the current switching network. The converter can function as a multiplying DAC by varying the reference input voltage. The reference and output amplifier are short circuit protected.

The input register is controlled by an enable line (LOAD). When low, the registers are transparent and any change on the digital input pins will be reflected on the analog output. A high state level will latch this digital information, and the data is retained until this enable line goes low. The data and latch enable input lines have low input load currents.

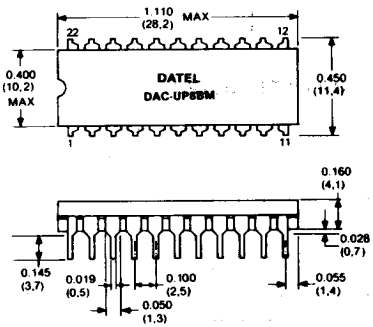
The DAC design consists of 8 fast-switching current sources, a diffused R-2R resistor ladder network and a control amplifier. The diffused resistor network gives excellent temperature tracking resulting in a gain temperature coefficient of 30 ppm/°C. This bipolar monolithic fabrication results in excellent linearity and temperature coefficient.

With an accuracy of 0.19% the device is monotonic (no missing codes) over the entire operating temperature range. Power supply requirements are ±12V to ±18V. The operating temperature range of the DAC-UP8BC is 0 to +70°C while the DAC-UP8BM operates from −55°C to +125°C.

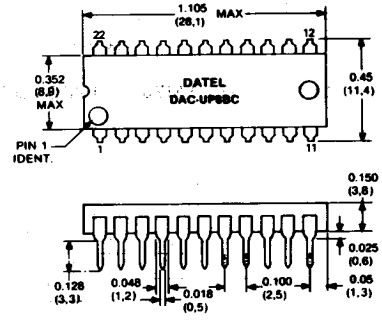


MECHANICAL DIMENSIONS
INCHES (MM)

CERAMIC PACKAGE
DAC-UP8BM



PLASTIC PACKAGE
DAC-UP8BC



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL GND	12	REF ADJ
2	BIT 8 IN (LSB)	13	REF OUT
3	BIT 7 IN	14	REF IN
4	BIT 6 IN	15	BIPOLAR OFFSET
5	BIT 5 IN	16	DAC COMP
6	BIT 4 IN	17	−15V
7	BIT 3 IN	18	OUTPUT
8	BIT 2 IN	19	+15V
9	BIT 1 IN (MSB)	20	SUM JUNCTION
10	LOAD	21	AMP COMP
11	NC	22	ANALOG GND

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ABSOLUTE MAXIMUM RATINGS	
Positive Supply, pin 19	+18V
Negative Supply, pin 17	−18V
Digital Input Voltage, pins 2-10	+18V
Reference Input, pin 14	+12V
Summing Junction, pin 20	+12V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V Supply, Ref. In = +5V unless otherwise noted.

INPUTS	
Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+2.0V to +5.5V at 10 μA
Input Logic Level, bit OFF ("0")	0V to +0.8V at −10 μA
Load Input	High ("1") = Hold Data Low ("0") = Transfer Data
Load Pulse Width[1]	150 nsec. minimum
Reference Input Voltage	+5V ±10%
Reference Input Resistance	5K
Reference Input Slew Rate	25V/μsec.
OUTPUT	
Output Voltage Range, unipolar	0 to +10V
Output Voltage Range, bipolar	±5V
Output Current	5 mA
Output Resistance	5 ohms
Reference Output Voltage	+5V ±10%
Reference Output Current	5 mA
PERFORMANCE	
Linearity Error	±½ LSB maximum
Differential Linearity Error	±½ LSB
Monotonicity	8 Bits over operating temperature range
Gain Error	Adjustable to zero
Zero Error	Adjustable to zero
Gain Tempco	20 ppm/°C
Zero Tempco, Unipolar	5 ppm/°C of FS.
Offset Tempco, Bipolar	10 ppm/°C of FS.
Reference Tempco	60 ppm/°C
Settling Time to ½ LSB[2]	2 μsec.
Power Supply Rejection	±1 mV/V
POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V dc
Power Supply Voltage Range	±12 to ±18V dc
Supply Current, quiescent	+7 mA, −10 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BC) 55°C to +125°C (BM)
Storage Temperature Range	−65°C to +150°C
Package Type	22 pin plastic (BC) 22 pin ceramic (BM)

FOOTNOTES:

1. See Timing Diagram
2. For 10V change

OUTPUT RANGE SELECTION

MODE	RANGE	CONNECTION
Unipolar	0 to +10V	Pin 15 to 20
Bipolar	±5V	Pin 15 open

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with 0.1 μf ceramic capacitors. This precaution will assure noise-free operation of the converter.
2. Both the Output (pin 18) and Reference Output (pin 13) are short circuit protected. Output short circuit current is typically 40 mA for the Output and 15 mA for the Reference Output.
3. The "LOAD" control pin is a level triggered input which causes the register to hold data with a logic "1" input state and transfer data to the DAC with a logic "0" input.
4. A Setup Time of 200 nanoseconds minimum must be allowed for the input data before the LOAD input goes from low to high. In addition, a 50 nanoseconds minimum Hold Time must be allowed for the input data after the LOAD input goes from low to high. The minimum pulse width for the LOAD input is 200 nanoseconds. The maximum update rate is determined by the output settling time. See the Timing Diagram.
5. The output settling time may be decreased somewhat by decreasing the value of the 50 pF feedback capacitor from the amplifier Output (pin 18) to the Summing Junction (pin 20). The minimum capacitance value is 10 pF.
6. The gain temperature coefficient of the DAC-UP8B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm typical results for the converter. If greater temperature stability is required, a more stable external reference should be used.
7. The data inputs (Bits 1 through 8) are high impedance inputs which give minimal logic loading. For an input low, the current that must be sinked is only 50 μA maximum, or about 1/32 of a standard TTL load. This minimizes the loading of the DAC-UP8B on a data bus.

CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION table.
2. Apply a logic "0" to $\overline{\text{LOAD}}$ (pin 10).
3. **Zero and Offset Adjustments**

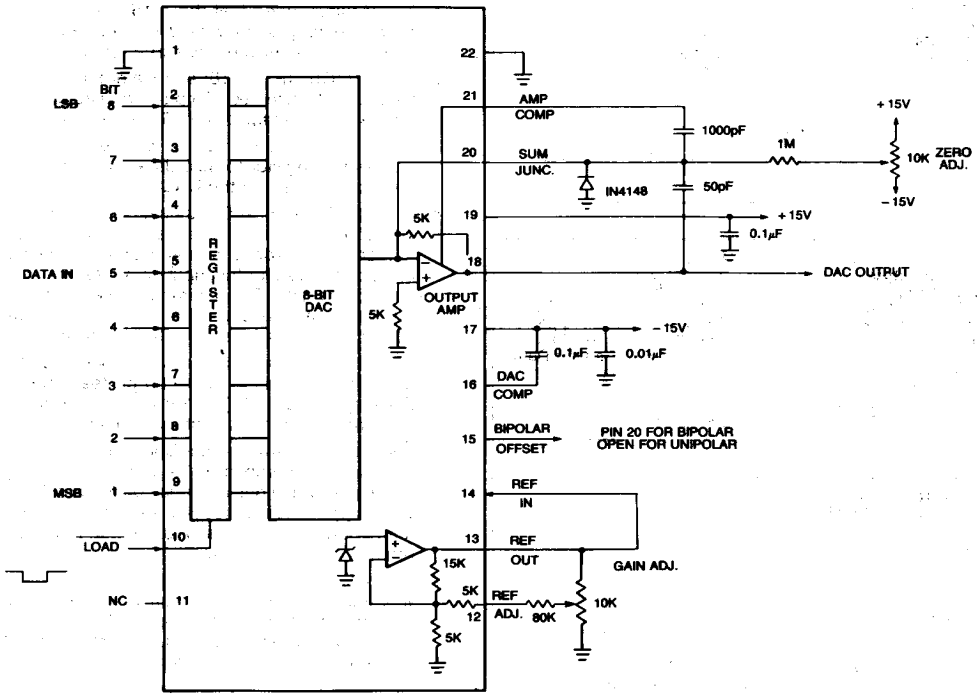
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for negative full scale voltage of −5.000V.
4. **Gain Adjustment**

   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust FULL SCALE ADJ for the positive full scale voltage of +9.961V (unipolar) or +4.961V (bipolar).

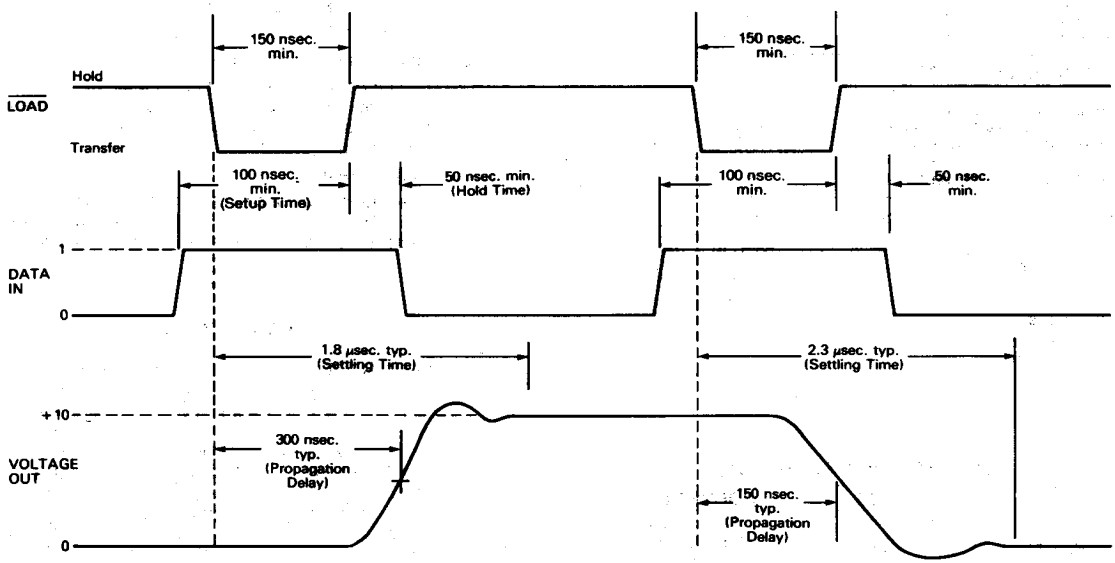
CODING TABLE

INPUT CODE MSB	LSB	OUTPUT RANGES 0 to +10V	±5V
1111	1111	+9.961V	+4.961V
1110	0000	+8.750	+3.750
1100	0000	+7.500	+2.500
1000	0000	+5.000	0.000
0100	0000	+2.500	−2.500
0000	0001	+0.039	−4.961
0000	0000	0.000	−5.000

CONNECTION AND CALIBRATION

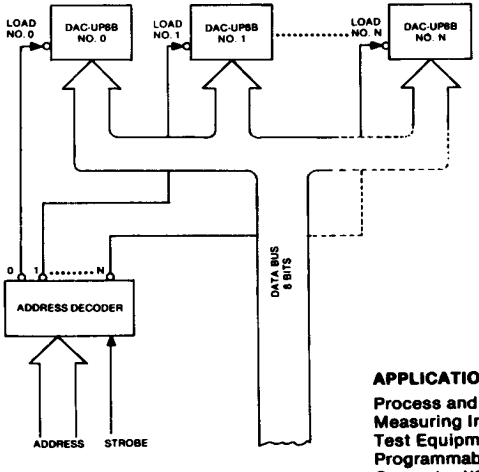


TIMING DIAGRAM



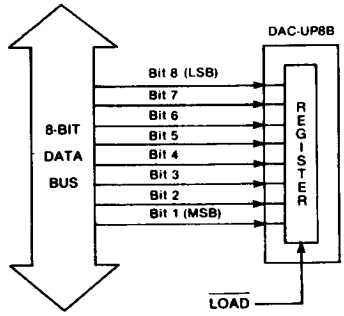
APPLICATIONS

INTERFACING TO 8 BIT DATA BUS



APPLICATIONS

Process and Control
Measuring Instruments
Test Equipment
Programmable Power Supplies
Computer I/O Equipment



This illustrates the connection for loading parallel data into the input register. The register circuit is a static latch and is controlled by the $\overline{\text{LOAD}}$, active low. When the data is stable on the data inputs (bits 1-8), it can be transferred on the positive edge of the $\overline{\text{LOAD}}$ pulse. The voltage levels on the data bus should be stable for at least 200 nsec before $\overline{\text{LOAD}}$ goes HI. The minimum pulse width of the $\overline{\text{LOAD}}$ command is 200 nsec.

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ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	CASE
DAC-UP8BC	0 to 70°C	Plastic
DAC-UP8BM	−55 to 125°C	Ceramic

ACCESSORIES

Part Number	Description
TP10K	Trimming Potentiometers