Contents

1. General

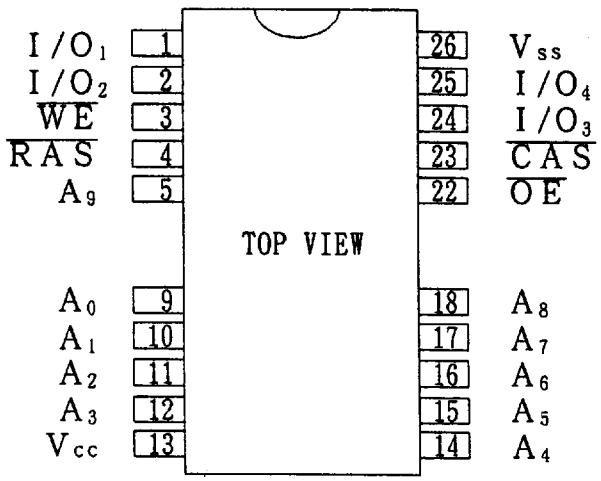
SHARP LH6B4400BK-6 is 1,048,576word x 4bit Dynamic Random access memory. With its input multiplexed and packaged in the standard 26/20pin SOJ, it is easy to realize memory systems with low power dissipation and large memory capacity. The LH6B4400BK-6 operates on single +5.0V power supply and the built-in biasing voltage generator circuit.

The LH6B4400BK-6 allows fast page mode access.

2. Features

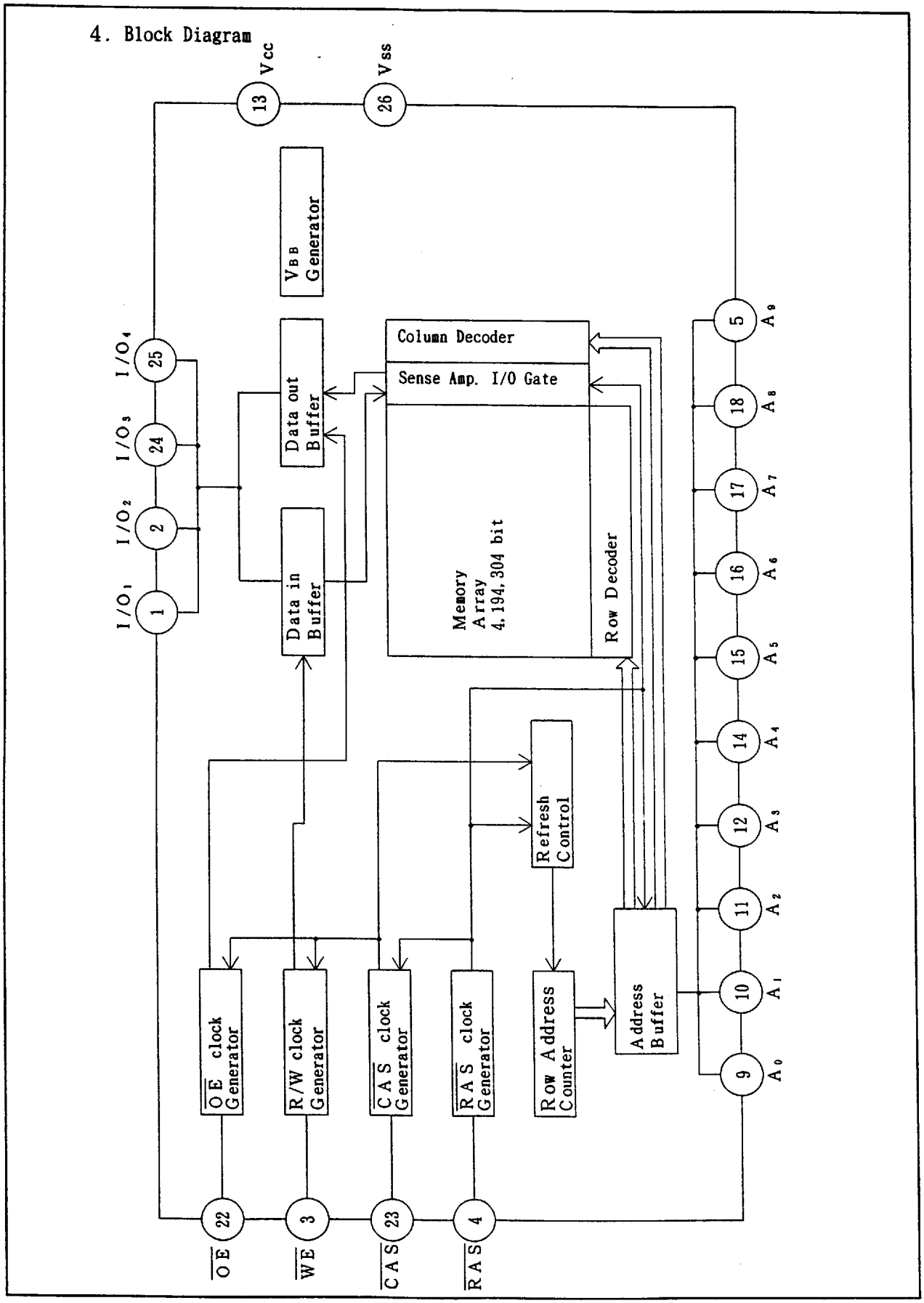
- 1,048,576word × 4bit
- Standard 300mil 26/20pin SOJ (SOJ26-P-300) plastic package
- Access time 60ns(Max.)
- Cycle time 110ns(Min.)
- Fast page mode cycle time 40ns(Min.)
- Power supply +5.0V±10%
- Power consumption(Max.) 605mW (Operating t_{RC}=min.)
  11mW (Standby : TTL input level)
  5.5mW (Standby : CMOS input level)
- Built-in latch circuit for Row-address, Column-address and Input-data
- $\overline{OE}$=Don't care in early write operation
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- On-chip refresh counter
- 1024 refresh cycle / 16ms
- Not designed or rated as radiation hardened
- Substrate material : P-type silicon
- CMOS process
- Operating temperature range : 0 to +70℃

3. Pin configuration



Symbol	Pin Name
A_0 to A_9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1 to I/O_4	Data Input/Output
V_{cc}	Power Supply(+5.0V)
V_{ss}	Power Supply(0V)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Rating	Unit	Note
Applied voltage on all pins	−1.0 to +7.0	V	1
Operating temperature	0 to +70	℃	
Storage temperature	−55 to +125	℃	
Power dissipation	1.0	W	

Note 1. With respect to Vss.

6. Recommended D C Operating Conditions

(Ta=0to+70℃)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage		V_{CC}	4.5	5.0	5.5	V	
		V_{SS}	0	0	0	V	
Input voltage		V_{IH}	2.4		6.5	V	
	I/O pin	V_{IL}	-1.0		0.8	V	
	Others	V_{IL}	-2.0		0.8	V	

7. Pin Capacitance

(Ta=25℃, V_{CC}=5.0V±10%)

Parameter		Symbol	MIN.	MAX.	Unit
Input capacitance	A_0 to A_9	C_{IN1}	−	5	pF
	$\overline{RAS}$, $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	−	7	pF
Input/Output capacitance	I/O_1 to I/O_4	C_{OUT}	−	10	pF

8. DC Electrical Characteristics

(Ta=0 to +70℃, V_{CC}=5.0V±10%)

Parameter			Symbol	MIN.	MAX.	Unit	Note
Average supply current in normal operation			I_{CC1}	–	110	mA	2, 3
Supply current in the stand-by mode	CMOS	$\overline{RAS}$=$\overline{CAS}$≥Vcc-0.2V	I_{CC2}	–	1	mA	2
	TTL	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		–	2	mA	2
Average supply current in the fast page mode			I_{CC4}	–	110	mA	2, 3
Average supply current in $\overline{CAS}$ before $\overline{RAS}$ refresh cycle			I_{CC6}	–	110	mA	2, 3
Average supply current in $\overline{RAS}$ only refresh cycle			I_{CC3}	–	110	mA	2, 3
Input leakage current	0V≦V_{IN}≦7V		I_{LI}	-10	10	μA	
Output leakage current	0V≦V_{OUT}≦7V Output=Disable		I_{LO}	-10	10	μA	4
Output "High" voltage	I_{OUT}=−5mA		V_{OH}	2.4	Vcc	V	
Output "Low" voltage	I_{OUT}=4.2mA		V_{OL}	0	0.4	V	

Note 2. The output pins are in high impedance state.

3. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on the cycle time.

4. The output pins are disabled by $\overline{RAS}$=$\overline{CAS}$=V_{IH} or $\overline{CAS}$=V_{IH}.

9. AC Electrical Characteristics(Note 5, 6, 7, 20)(Ta=0 to +70℃, Vcc=5.0V±10%)

Test Conditions

Input rise and fall times : 5ns Output load : 2 TTL qate + C_L(100pF)

Input, Output timing reference levels:0.8v, 2.4v (Including scope and jig)

Common Parameters

Parameter	Symbol	MIN.	MAX.	Unit	Note
Random read or write cycle time	t_{RC}	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	ns	
Row address set-up time	t_{ASR}	0	–	ns	
Row address hold time	t_{RAH}	10	–	ns	
Column address set-up time	t_{ASC}	0	–	ns	
Column address hold time ($\overline{RAS}$)	t_{CAH}	15	–	ns	
$\overline{CAS}$ delay time ($\overline{RAS}$)	t_{RCD}	20	45	ns	8
Column address delay time ($\overline{RAS}$)	t_{RAD}	15	30	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	–	ns	
$\overline{CAS}$ precharge time ($\overline{RAS}\downarrow$)	t_{CRP}	10	–	ns	
$\overline{OE}$ delay time	t_{OED}	15	–	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	–	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	–	ns	
Transition time (rise and fall)	t_T	3	50	ns	10
Column address lead time ($\overline{RAS}$)	t_{RAL}	30	–	ns	
$\overline{OE}$ pulse width	t_{OEP}	15	–	ns	

Read Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	–	60	ns	11, 12
Access time from $\overline{CAS}$	t_{CAC}	–	15	ns	12, 13
Access time from column address	t_{AA}	–	30	ns	12, 14
Access time from $\overline{OE}$	t_{OEA}	–	15	ns	12
Read command set-up time ($\overline{CAS}$)	t_{RCS}	0	–	ns	
Read command hold time ($\overline{CAS}$)	t_{RCH}	0	–	ns	
Read command hold time ($\overline{RAS}\uparrow$)	t_{RRH}	0	–	ns	
Output data disable time ($\overline{CAS}$)	t_{OFF}	0	15	ns	15
Output data disable time ($\overline{OE}$)	t_{OEZ}	0	15	ns	15
$\overline{CAS}$ to Din delay time	t_{CDD}	15	–	ns	

Write Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
Write command set-up time ($\overline{CAS}$)	t_{WCS}	0	–	ns	9
Write command hold time ($\overline{CAS}$)	t_{WCH}	15	–	ns	
Write pulse width ($\overline{WE}$)	t_{WP}	10	–	ns	
Write command lead time ($\overline{RAS}$)	t_{RWL}	15	–	ns	
Write command lead time ($\overline{CAS}$)	t_{CWL}	15	–	ns	
Data input set-up time	t_{DS}	0	–	ns	17
Data input hold time	t_{DH}	15	–	ns	17

Read Modify Write Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
Read-write cycle time	t_{RWC}	150	–	ns	
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	80	–	ns	16
$\overline{WE}$ delay time ($\overline{CAS}$)	t_{CWD}	35	–	ns	16
Column address delay time ($\overline{WE}$)	t_{AWD}	50	–	ns	16
$\overline{OE}$ hold time ($\overline{WE}$)	t_{OEH}	15	–	ns	

Refresh Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
$\overline{CAS}$ set-up time ($\overline{RAS}$)	t_{CSR}	10	–	ns	
$\overline{CAS}$ hold time ($\overline{RAS}$)	t_{CHR}	10	–	ns	
$\overline{RAS}$ · $\overline{CAS}$ precharge time ($\overline{RAS}$ ↑)	t_{RPC}	10	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	ns	
Refresh time interval	t_{REF}	–	16	ms	

Fast Page Mode Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
Fast page mode cycle time	t_{PC}	40	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	–	100,000	ns	18
$\overline{CAS}$ precharge access time	t_{CPA}	–	35	ns	19
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	–	ns	

Fast Page Mode Read Modify Write Cycle

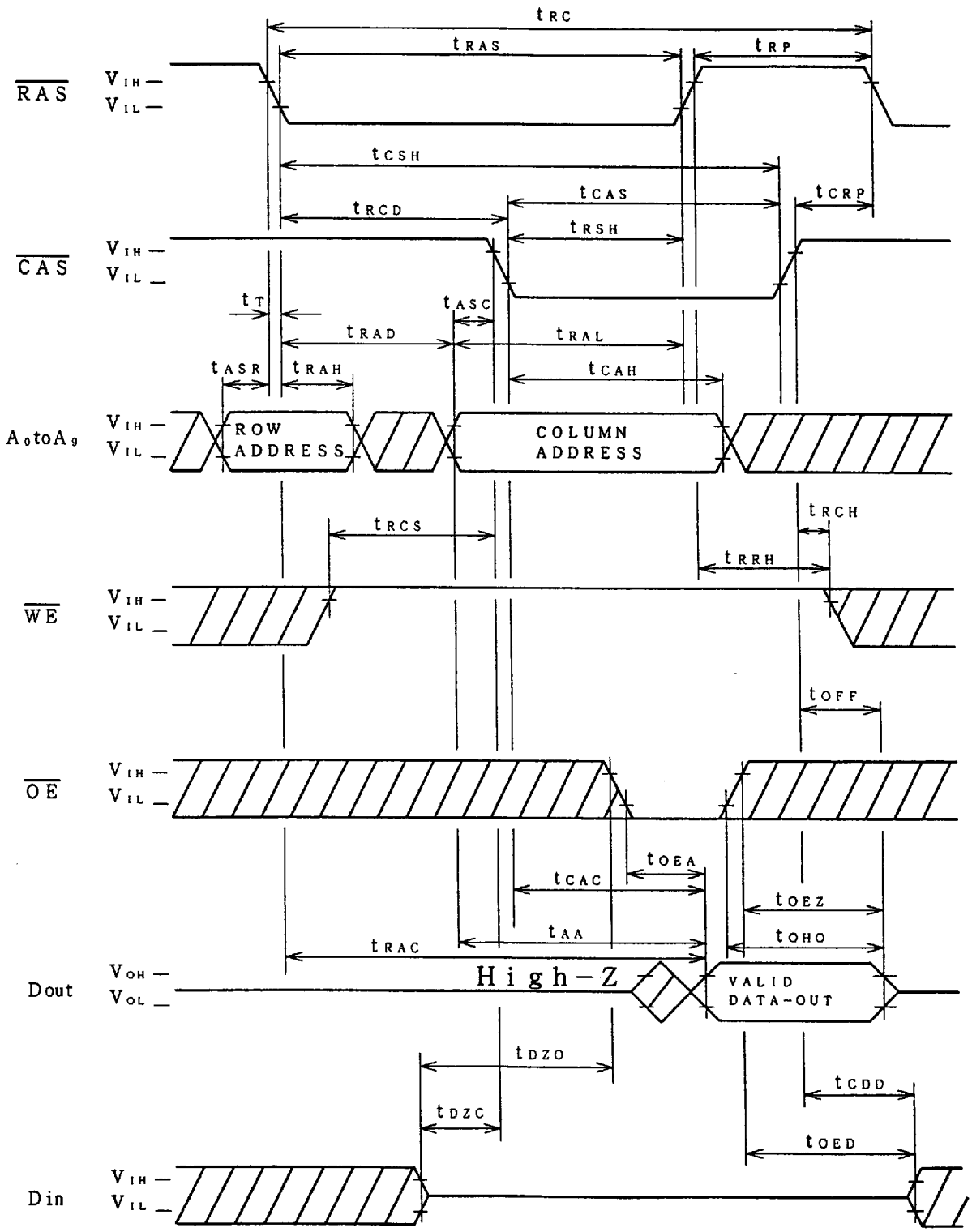
Parameter	Symbol	MIN.	MAX.	Unit	Note
Read-write cycle time (page mode)	t_{PRWC}	80	–	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	55	–	ns	

Note:

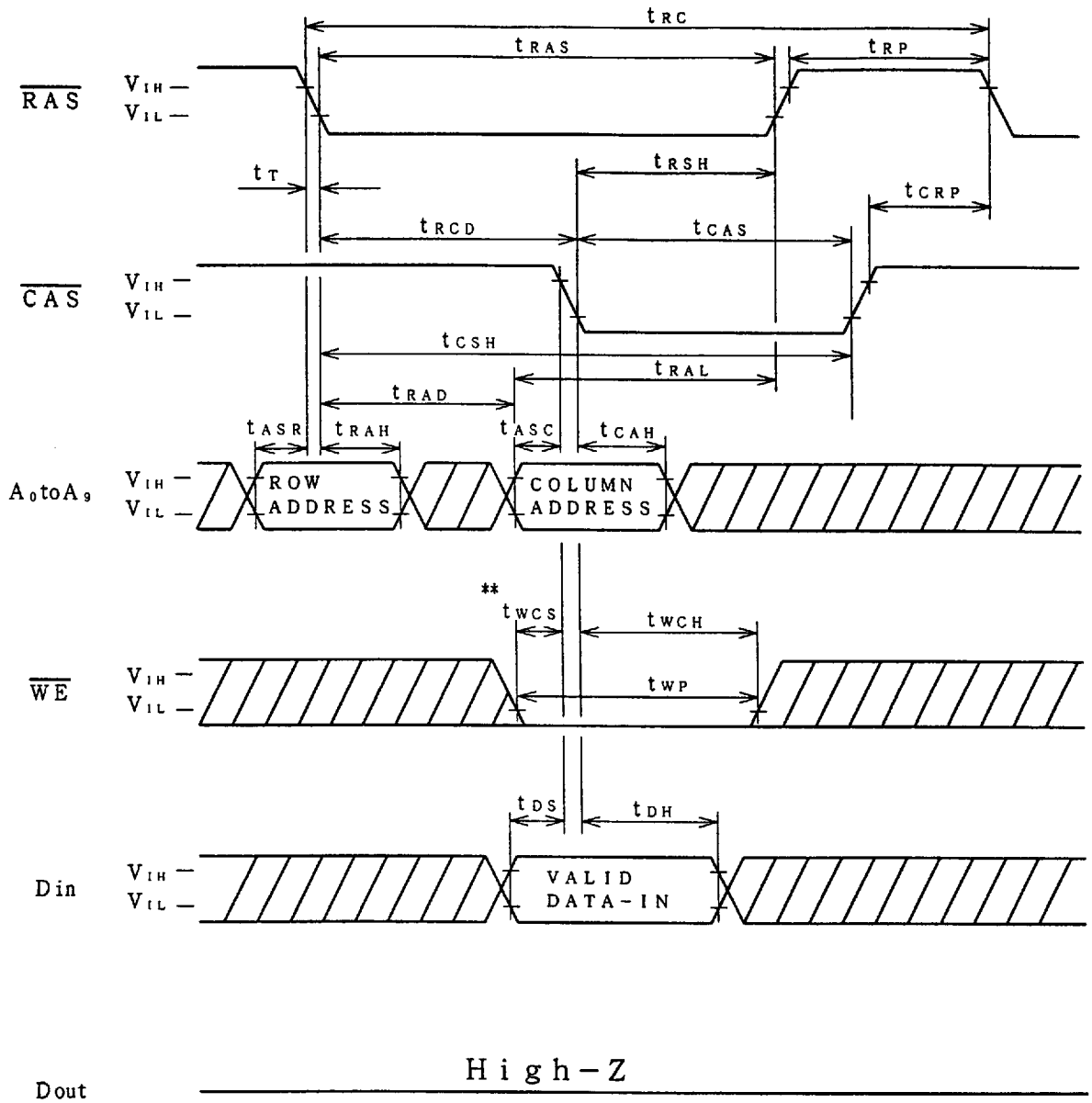
5. AC characteristics assume t_T=5ns.
6. For properly functioning the memory, at least 100μs of pause time after power-on and followed by several 8 dummy cycles. When $\overline{RAS}$=V_{IH} continued for more than 8ms, the same dummy cycles should be given.
   Usually 8 ordinary refresh cycles should be given.
7. Row address are indispensable on address A0 to A9, column address are A0 to A9.
8. t_{RCD}(MAX.) is the maximum point for t_{RCD} where t_{RAC}(MAX.) is ensured, and dose not represent a limit of operation.
   If $t_{RCD} \geqq t_{RCD}$(MAX.), the access time comes under the control of t_{CAC}.
9. t_{RAD}(MAX.) is the maximum point for t_{RAD} where t_{RAC}(MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RAD} \geqq t_{RAD}$(MAX.), the access time comes under the control of t_{AA}.
10. V_{IH}(MIN.) and V_{IL}(MAX.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(MIN.) and V_{IL}(MAX.).
11. Assumes that $t_{RCD} \leqq t_{RCD}$(MAX.) and $t_{RAD} \leqq t_{RAD}$(MAX.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
12. Measured with a load equivalent to 2 TTL (-1mA, +4mA) + C load (100pF).
    (Including the scope and the jig)
13. Assumes that $t_{RCD} \geqq t_{RCD}$(MAX.) and $t_{RAD} \leqq t_{RAD}$(MAX.).
14. Assumes that $t_{RCD} \leqq t_{RCD}$(MAX.) and $t_{RAD} \geqq t_{RAD}$(MAX.).
15. t_{OFF}(MAX.) and t_{OEZ}(MAX.) define the time at which the outputs achieve the high-Z condition and are not referenced to output voltage levels.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not the restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$(MIN.), the cycle is an early write cycle and the data out pin will remain open circuit(high-Z) throughout the entire cycle; if
    $t_{RWD} \geqq t_{RWD}$(MIN.), $t_{CWD} \geqq t_{CWD}$(MIN.) and $t_{AWD} \geqq t_{AWD}$(MIN.), or
    $t_{CWD} \geqq t_{CWD}$(MIN.), $t_{AWD} \geqq t_{AWD}$(MIN.) and $t_{CPW} \geqq t_{CPW}$(MIN.) the cycle is a read modify write and the date output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
17. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read modify write cycle.
18. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
19. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
20. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.

10. Timing Chart

Read Cycle



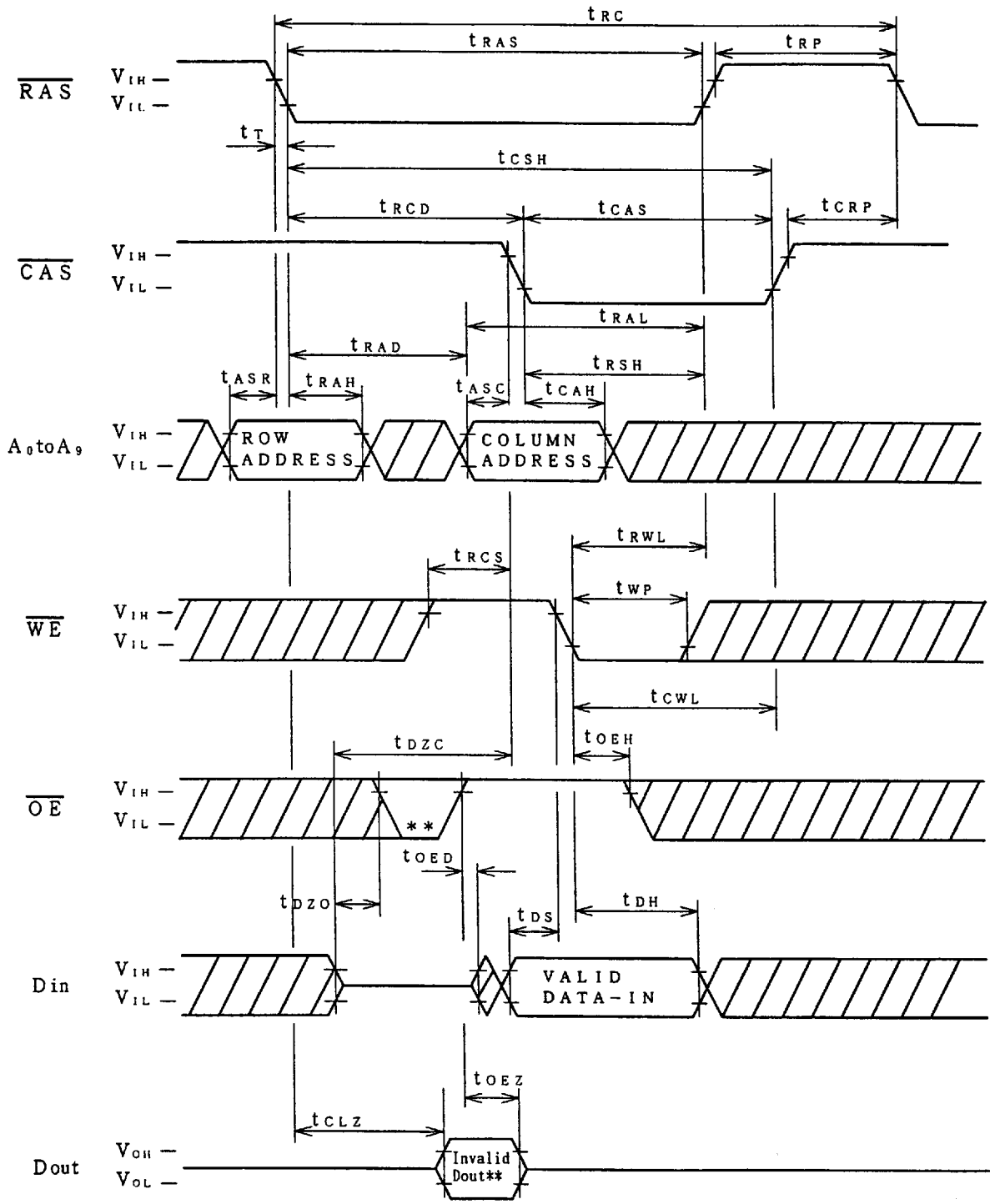
Early Write Cycle



$\overline{OE}$ = Don't Care

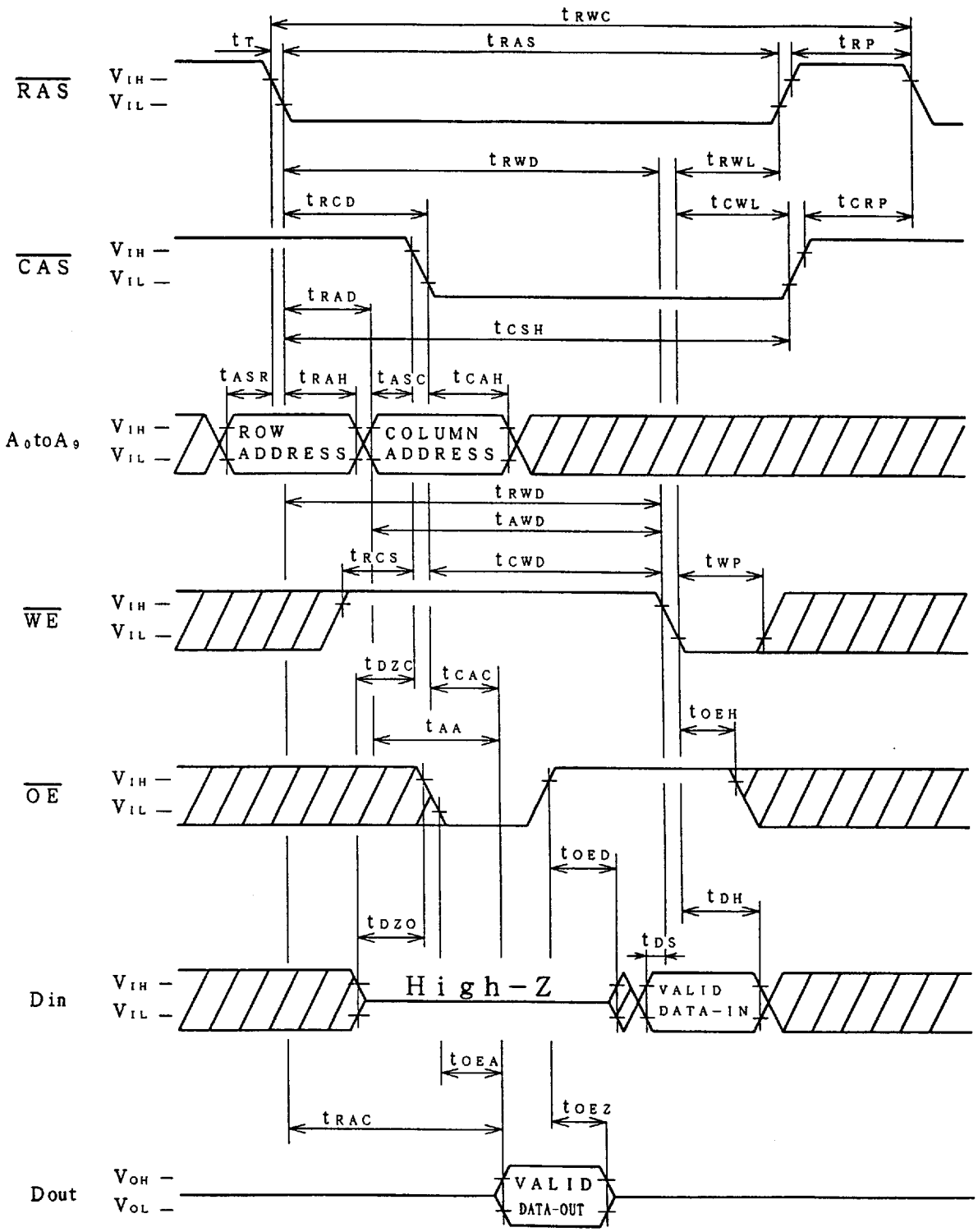
** twcs≥twcs(MIN.)

Delayed Write Cycle

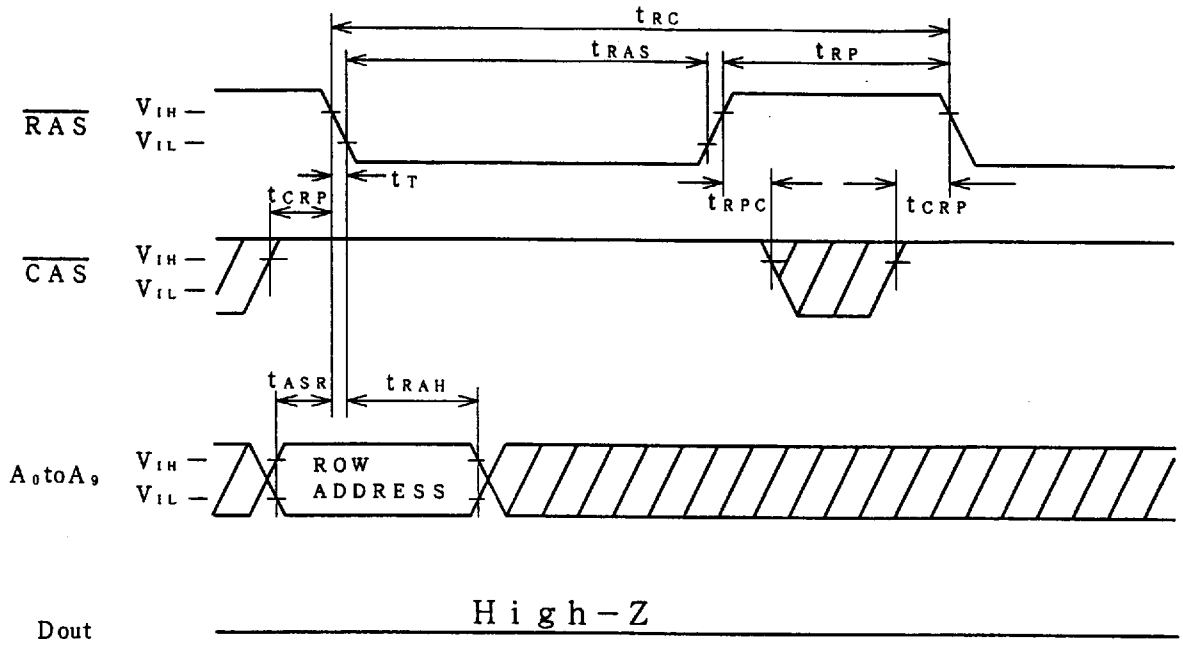


** : Invalid Dout comes out, when $\overline{OE}$ is low level.

Read Modify Write Cycle



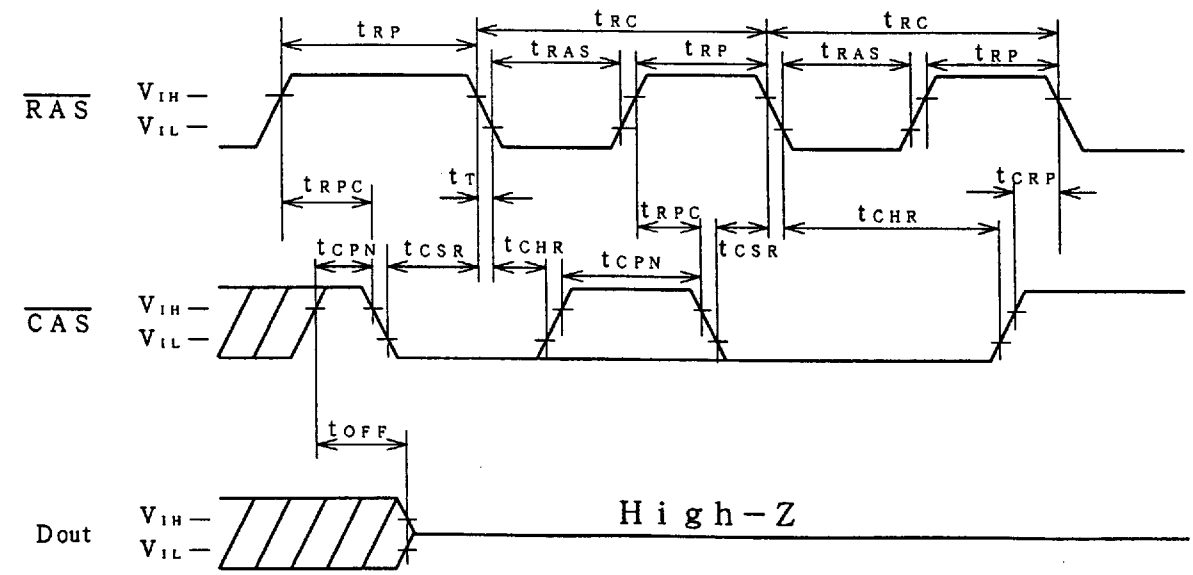
$\overline{RAS}$ Only Refresh Cycle



$\overline{WE}$, $\overline{OE}$ = Don't Care

Refresh address : A0 to A9 (AX0 to AX9)

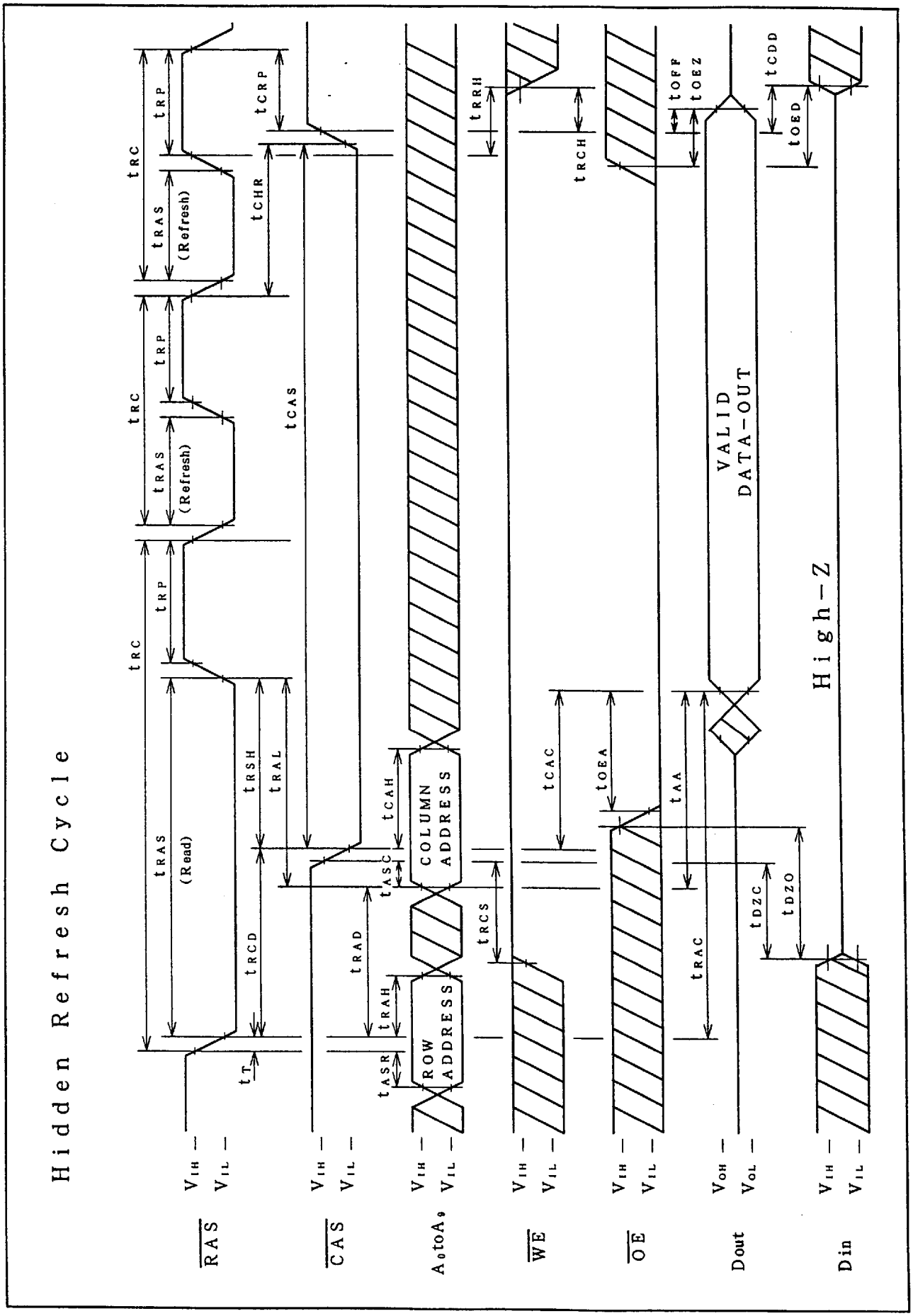
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



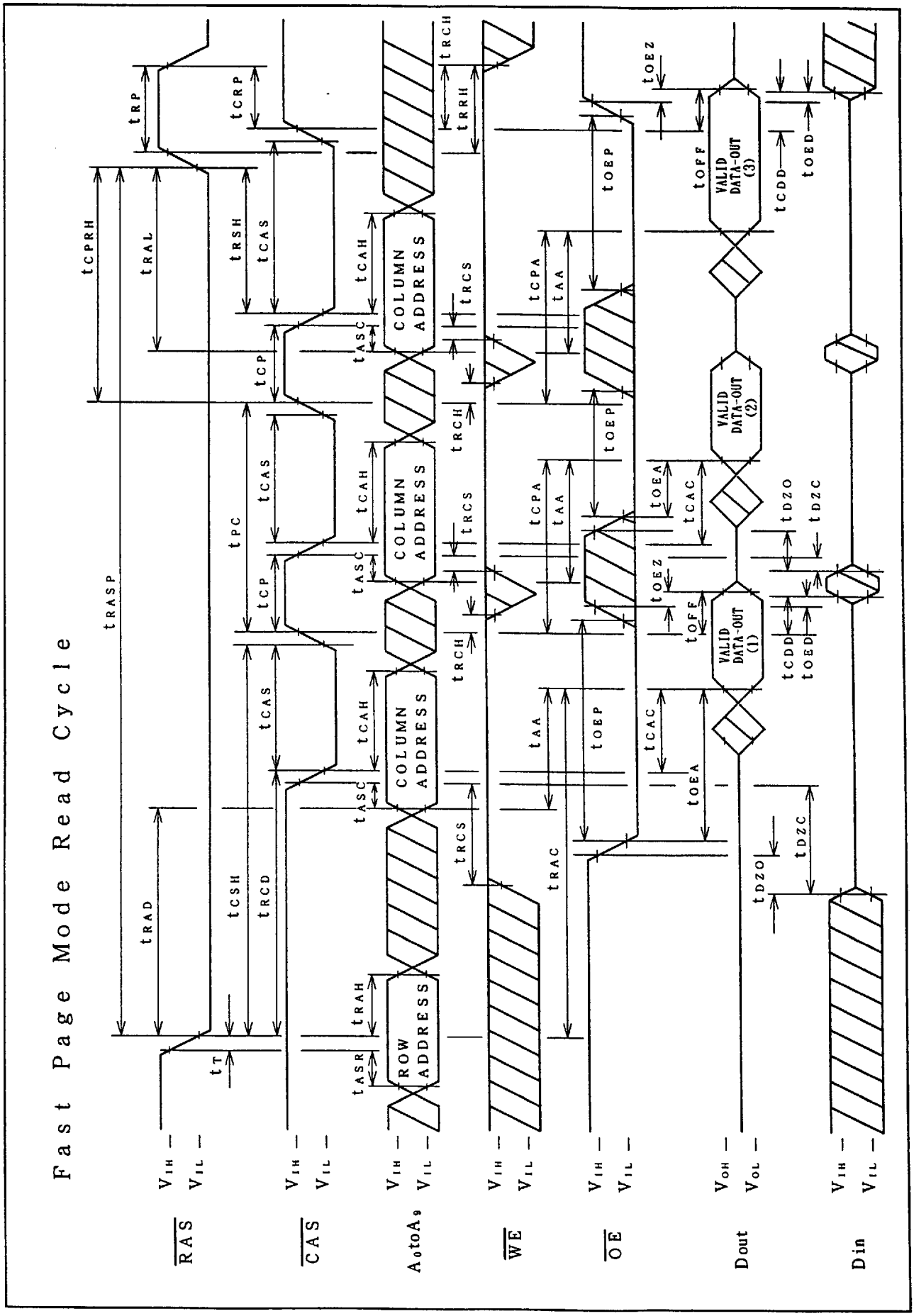
$\overline{OE}$, A0 to A9 = Don't Care

$\overline{WE}$ = VIH

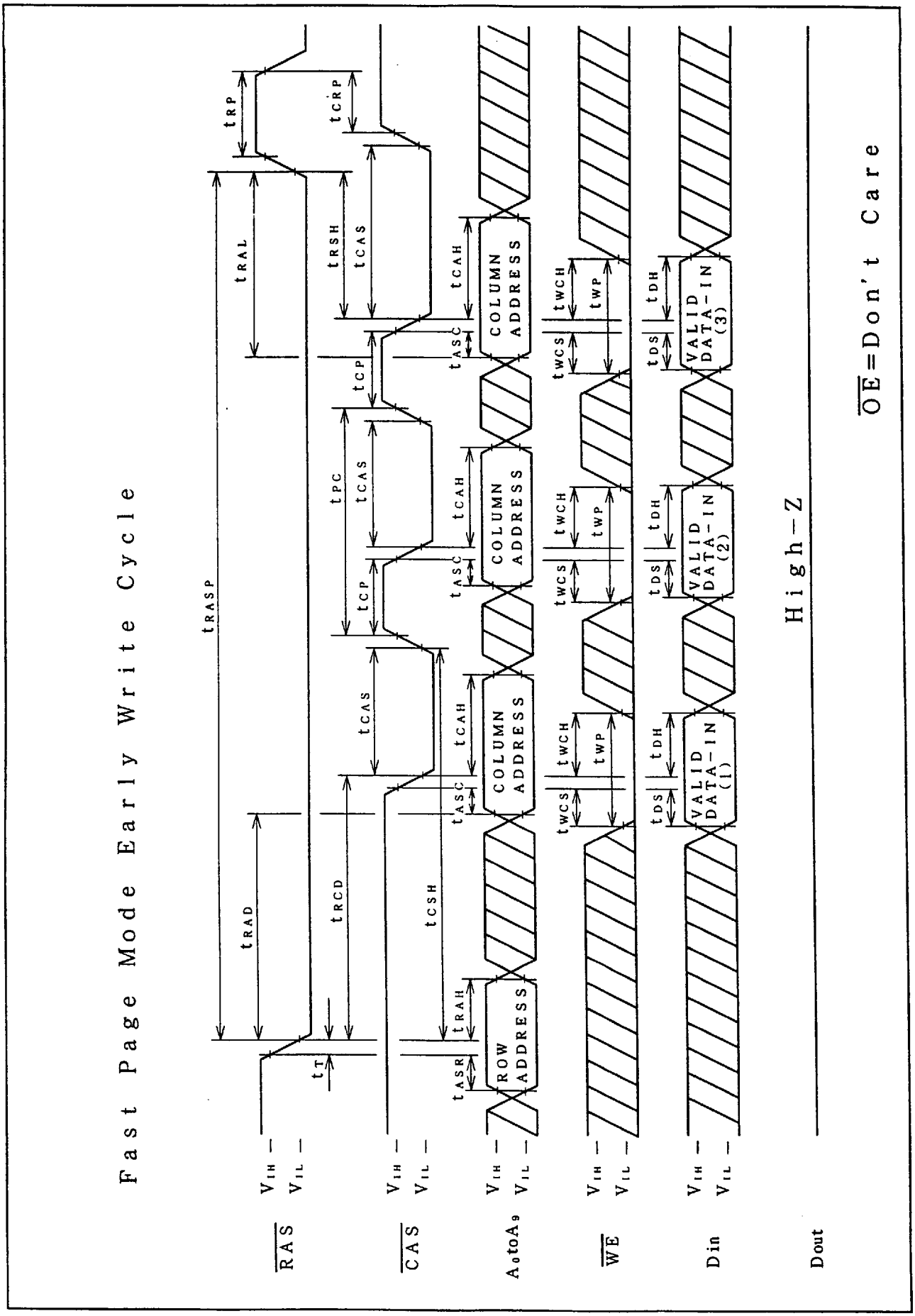
Hidden Refresh Cycle



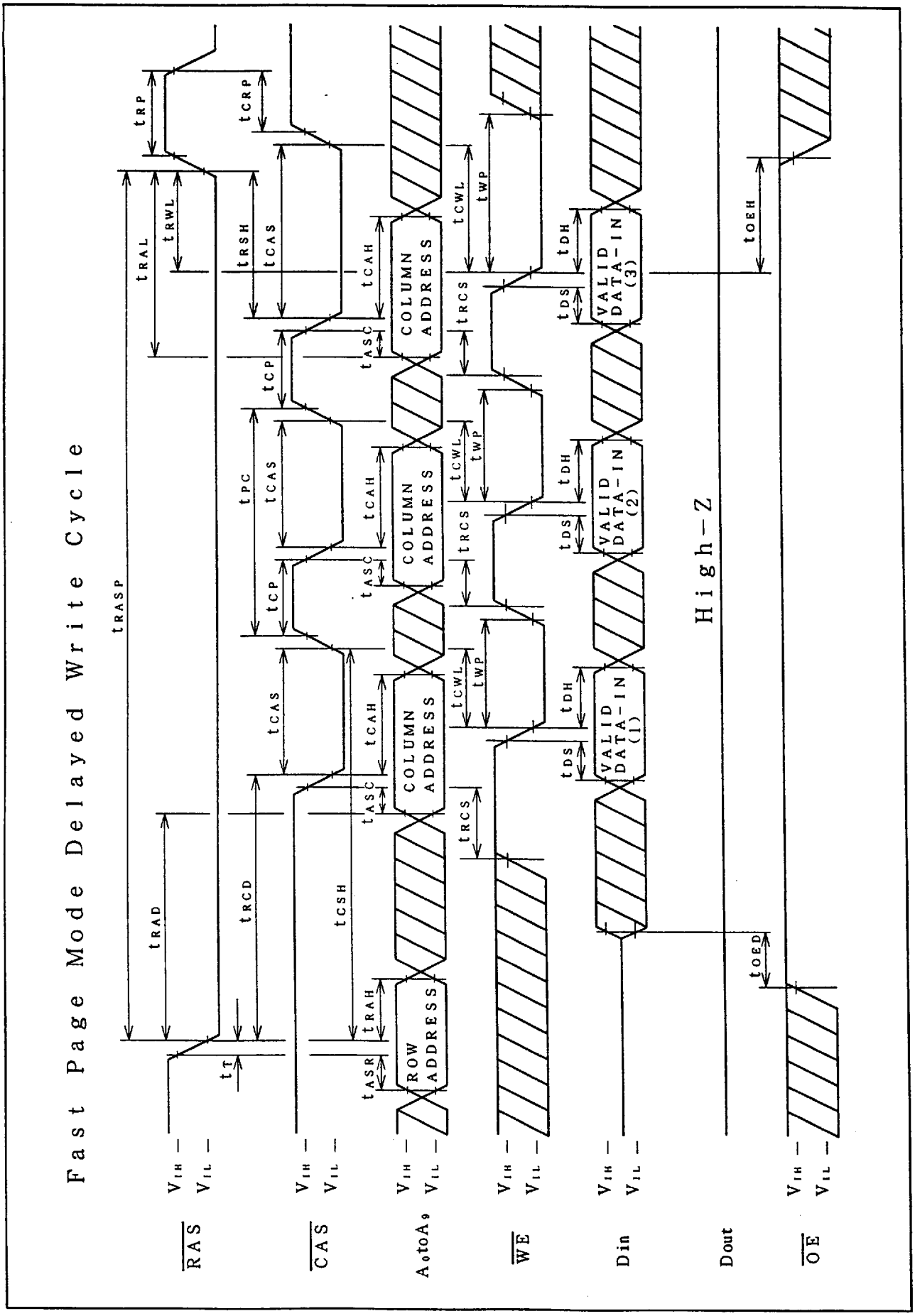
Fast Page Mode Read Cycle



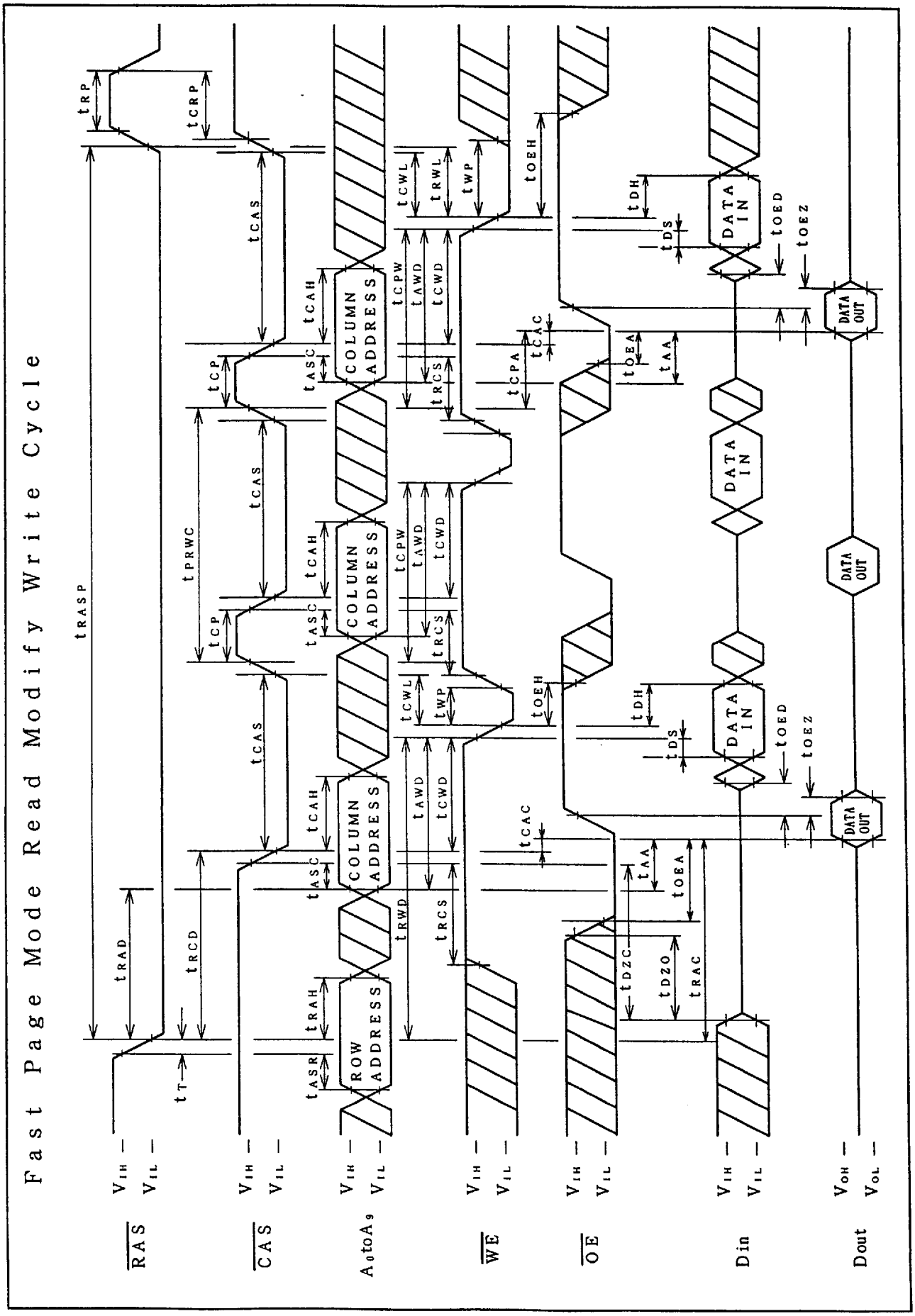
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle



Fast Page Mode Read Modify Write Cycle



11 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1146

2. Markings

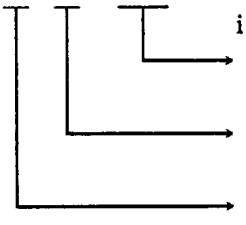
2-1. Marking contents

(1) Product name : LH6B4400BK-6

(2) Company name : SHARP

(3) Date code

(Example) T Y WW



(4) The marking of "KOREA" indicates the country of origin.

2-2. Marking layout

Refer to drawing No.AA1146

(This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3-1. Packing Materials

Material Name	Material Specificaiton	Purpose
Magazine	Anti-static treated plastic (25devices/magazine)	Packing of device
Stopper	Plastic or rubber	Fixing of device
Cap	Plastic (2caps/bag)	Fixing of Magazine
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
Inner case	Card board (1500devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of Magazine

(Devices shall be inserted into a magazine (sleeve) in the same direction.)

3－2. Outline dimension of magazine (sleeve)
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 90% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The magazine has been treated to be conductive or anti-static. If the device is transferred to another magazine, use a equivalent magazine.
(3) A stopper is included with the magazine. Before storage, make sure the stopper is inserted.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5 ~ 30℃ and a relative humidity of 60% or less and mount ICs within 168 hours after opening dry packing.

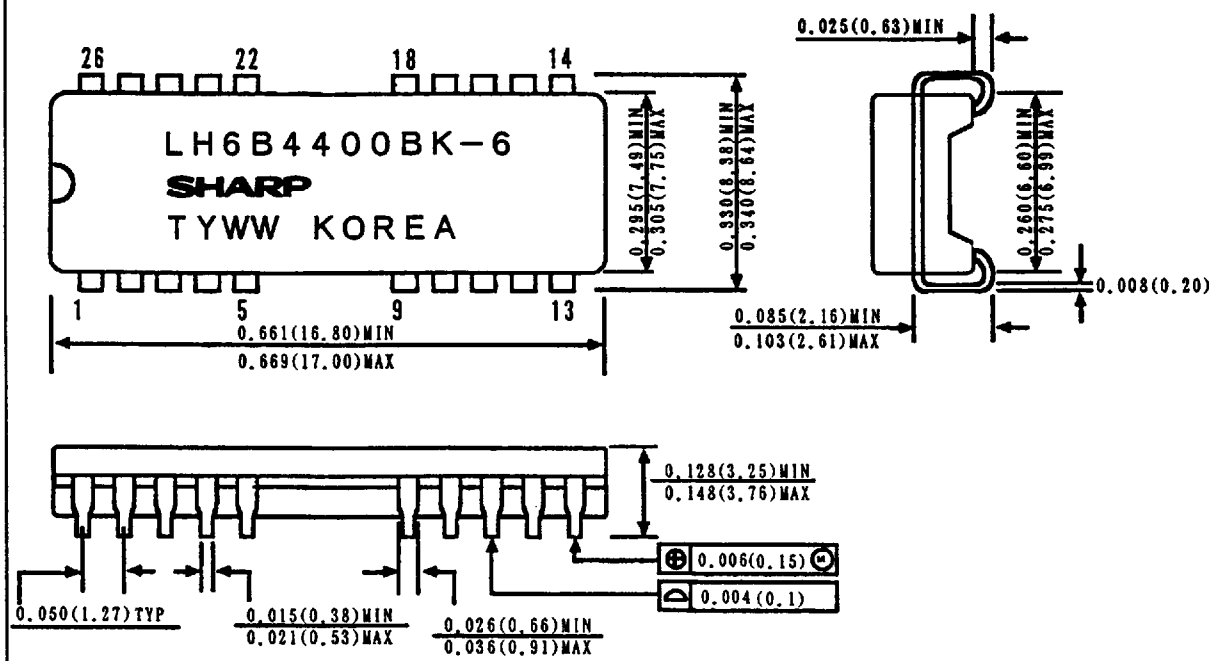
4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 24 hours at 125℃.
Note that the standard magazine can not be baked. Use the heat resistant magazine.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.

5. Surface Mount Conditions

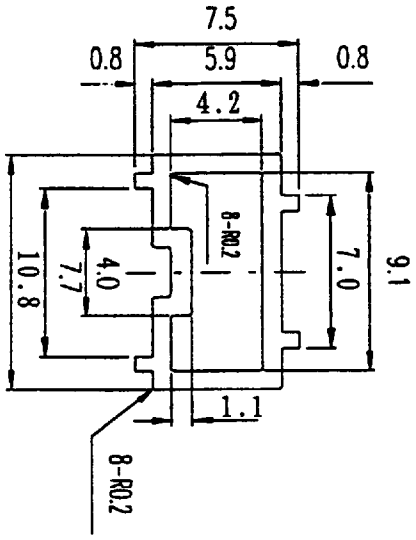
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

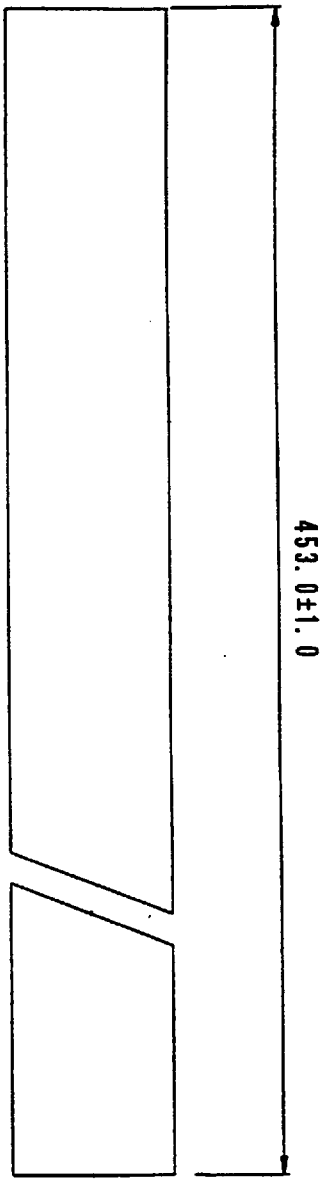
5－1. Soldering conditions (The conditions below are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 235℃ or less, duration of less than 10 seconds. Preheating of 150±10℃ ,duration of about 60 seconds. Temperature increase rate of 1～4℃/second.	IC package surface



名称 NAME	SOJ26/20-P-300	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE
DRAWING NO.	AA1146	単位 UNIT	INCHES (mm)	





注記 ：マガジン(スリーブ)両側のストッパーは、ゴムストッパーとする。
指示無き寸法公差は全て±０．２mmとする。

NOTES : Stopper which is set at the both ends of magazine (sleeve) is made of rubber.
All tolerances are ±0.2mm unless otherwise specified.

名称 NAME	SOJ26/20 MAGAZINE	備考 NOTE
単位 UNIT	mm	