Rockwell

Lightning Series™ - LI300, LI1000
Ultrahigh-Speed GaAs Gate Arrays

Features

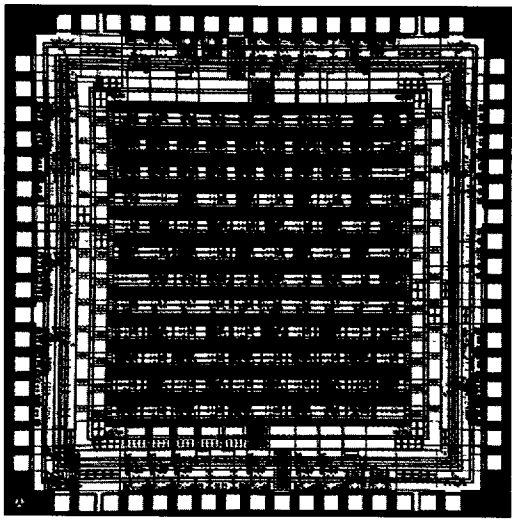
- Advanced HBT GaAs process for high performance
- Two array sizes: 300 or 1000 equivalent gates
- Clock rates up to 5 GHz
- Triple-layer metal routing and power distribution
- Three-level series gating for increased cell functionality
- Channeled architecture with up to 98 percent cell utilization
- Macrocell performance:
  - Implements 3-input exclusive OR, latch or other complex macros in one core cell
  - 20 ps typical delay @ 10.4 mW
- Fully differential logic minimizes skew and eliminates current spikes
- Choice of I/O: single or differential ECL, high speed differential CML, or CMOS-compatible PECL
- Choice of packages:
  - High performance 68-pin or 132-pin leaded ceramic chip carriers (LDCCs)
  - Low cost 52-pin plastic quad flatpack (PQFP)
- Power supplies: V_{CC} = ØV, V_{EE} = -5.2V, V_{CCP} = +5.0V (PECL-mode: V_{CC} = +5.0V, V_{EE} = ØV, V_{CCP} = +10V)
- Typical power: 2 W (LI300); 4-5 W (LI1000)
- Cadence, Mentor*, and Viewlogic* CAD support for schematic capture and simulation
- Verilog-XL for behavioral modeling and simulation
- PC-based GT-Estimater™ (gate timer) available for delay and power estimation*
- Testing up to 660 MHz (1.3 GHz in mux mode)

* contact factory for availability

Lightning Series Gate Arrays

Array	Equivalent Gates	Core Cells	D-Type Flip Flops	I/O Cells
LI300	300	120	60	40
LI1000	1,000	504	252	84

Figure 1
Photomicrograph of the Lightning LI300 array



Introduction

The Lightning Series™ of gate arrays are the first in a series of GaAs ASICs from Rockwell targeted at ultrahigh-speed applications. A unique three-level cell architecture, coupled with Rockwell's advanced AlGaAs/GaAs heterojunction bipolar transistor (HBT) technology, yields power-efficient devices with clock rates up to 5 GHz. The array is designed to interface with standard ECL, high-speed CML, or CMOS (PECL) systems to provide a cost-effective, high-performance solution.

Given their superior speed performance and fully-differential heterojunction circuit topology, Lightning devices provide robust noise margins and power conservation that is relatively independent of operation temperature and power supply variation. The Lightning architecture utilizes three levels of series gating for efficient device functionality to meet the challenges of today's most demanding high-performance applications.

Rockwell's world class manufacturing capability offers quick turnaround time, low cost assembly and packaging combined with statistical process control (SPC) to ensure that products are built right the first time. High speed testing is available using a HP83000 VLSI tester capable of 660 MHz (1.3 GHz in multiplexed mode).

Advanced HBT Technology

Fabrication of Lightning arrays is accomplished using a proprietary AlGaAs/GaAs HBT (heterojunction bipolar transistor) process developed at Rockwell over a five year period. A variety of circuits, including prescalers, gain blocks, digital-to-analog converters, and multiplexers have been successfully fabricated with high yields. The performance of some of these devices have exceeded frequencies of 10 GHz. A photomicrograph of a Lightning LI300 die is shown in figure 1; the layout of core cells and input/output cells for both arrays are depicted in figures 2 and 3.

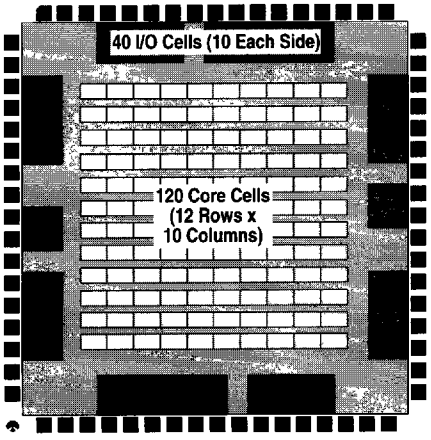


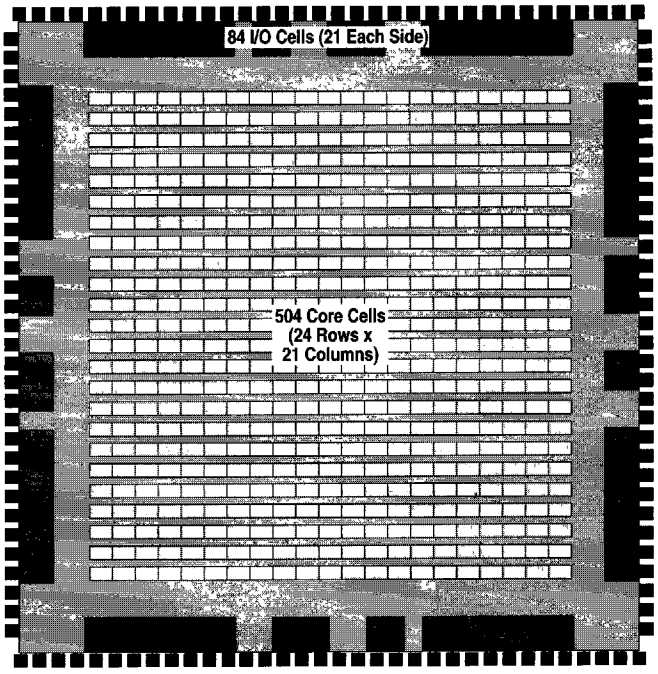
Figure 2
Core and I/O cell placement in the Lightning LI300 array

The process features high noise margins, low input capacitance, ultrahigh speed, relatively low power, and high output drive current. Three layers of metal are used for signal routing and power distribution. The typical loaded propagation delay for a high performance three-input exclusive-OR gate is 60 ps driving a single fan-out and one millimeter of wire.

The HBT technology employed by Rockwell in the Lightning Series features emitter-up/single-heterojunction bipolar transistors, monolithically-integrated Shottky diodes, NiCr thin-film resistors, MIM capacitors, and three levels of Au metal interconnect isolated by an advanced polyimide dielectric. A cross section showing an integrated HBT and Shottky diode are shown in figure 4.

Device isolation is accomplished with a combination of mesa etching and ion implantation. Thin film resistors, three-level logic gating, and three layers of metal combine to reduce the chip size and lower overall cost.

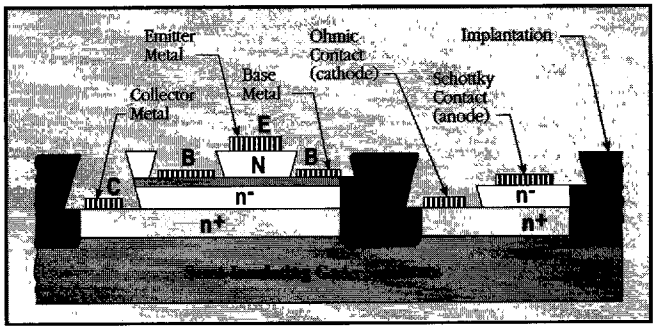
Figure 3
Core and I/O cell placement in the LI1000 array



Metal Routing for Personalizations

Three layers of metal are used for compact layouts. Signals are routed on two layers and power is distributed on the third. For maximized performance, Rockwell has developed an advanced polyimide dielectric for reduced capacitance in signal lines. The use of this state-of-the-art dielectric significantly increases each macro's drive capability, thereby reducing the delay on critical paths.

Figure 4
HBT process cross section



Placement and routing of metal interconnect is automated and optimized through the use of Cadence's Gate Ensemble™ (TANGATE). Gate Ensemble includes timing

driven placement (net and path constrained), soft grouping of macros, incremental layout changes, and highly accurate distributed RC calculations.

Applications

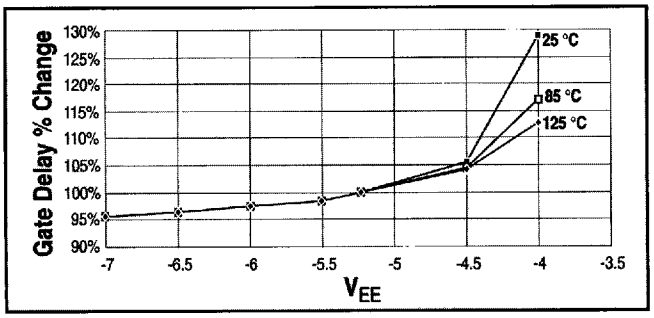
The Lightning Series of gate arrays are targeted at speed-critical system functions and bottlenecks requiring signal rates between 1 and 5 GHz. In addition to standard ECL and CML, the input/output cells are designed to interface with PECL logic levels so that lower speed portions of the system can be implemented in CMOS ASICs to help reduce overall system costs. Extended temperature capabilities make the Lightning arrays perfect for harsh environments such as communications, aerospace, or military applications. The following are ideal uses for the Lightning gate arrays:

- **Communications**—SONET Multiplexing and Demultiplexing, High Speed Switching, ATM Network Backplanes, Cellular-to-Telecom Switching;
- **Computers**—Backplanes, Data Switching, High-Speed LANs;
- **Testers**—Pin Electronics, Data Manipulation and Switching;
- **Digital Signal Processing**—Data Aquisition, Signal Analysis, Direct Digital Synthesis.

The fully differential logic used in Lightning core cells provides a high noise margin which is relatively independent of operation temperature and power supply variation. Figure 5 shows the minimal variation in propagation delay with respect to power supply and temperature variation typically observed in Lightning macrocells.

Figure 5

Change in gate delay (APT/ANT—>YPT/YNT) vs. V_{EE} at 25, 85, and 125 °C for a 3-input exclusive-OR gate

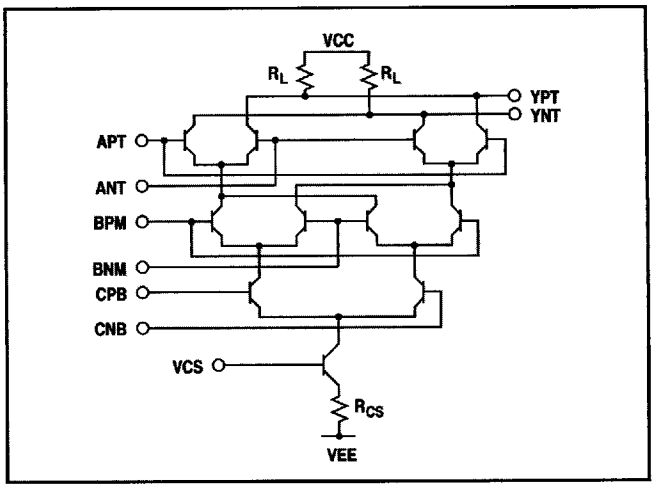


Architecture

The Lightning arrays utilize a tri-level current-mode logic (CML) approach to cell design (see figure 6). The use of three logic levels allows complex functions to fit into a compact area, yielding power economy coupled with short propagation delays. All internal signals are fully differential to minimize current switching transients and yield robust noise margins.

Figure 6

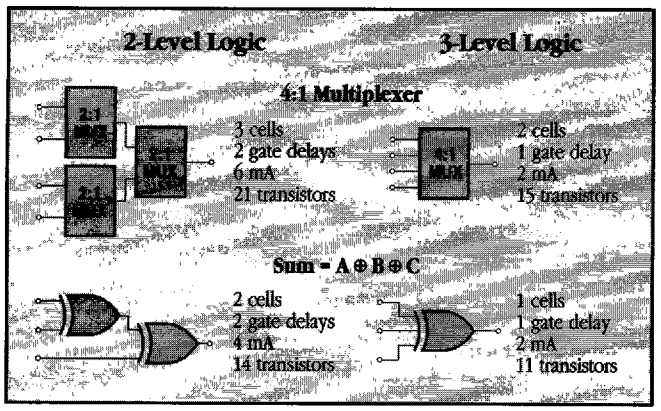
Schematic of a 3-input exclusive-OR gate showing the three-level logic tree characteristic of macrocells in the Lightning macro library



The use of three-level logic significantly improves chip performance. For example, the sum output from a full adder can be generated in only one equivalent gate delay and requires only 11 transistors. The same function in two-level logic requires two gate delays and 14 transistors. This difference lowers both power consumption and area as seen in figure 7.

Cell functions in the Lightning macro library are available in different speed/power versions to allow the designer to fine tune the overall chip performance. Most macrocells can be equipped with a level shift circuit, shown in figure 8, to drive the lower two logic levels (BPM/BNM and CPB/CNB inputs in figure 6) of driven macrocells. In a typical application though, only some of the circuitry will require level shifting, thereby saving power and freeing up these transistors for other functions.

Figure 7
Comparison of 2-level versus 3-level logic



Core and input/output cells are controlled by an on-chip reference voltage generator to compensate for temperature and power supply variations. The layout of pads, core cells, I/O cells, and routing channels are shown in figures 2 and 3.

Input/Output (I/O) Cells

The Lightning arrays contain I/O cells that can be configured to interface directly with ECL, CML and PECL logic levels. ECL and CML I/O types may be mixed in the same design for a flexible interface to external logic devices. The LI300 array contains 40 I/O cells—the LI1000 has 84. Each cell can be configured as either an output or input, providing flexibility over the arrangement and mixture of I/O signals.

Lightning ECL I/O are designed to be compatible with silicon ECL devices. Standard ECL 10K/100K outputs from other devices can interface directly with a Lightning array's ECL inputs. The ECL output is an emitter follower and is designed to be terminated with 50Ω to -2.0V. The ECL output requires a +5.0V supply.

PECL I/O requires a V_{CC} supply of +5.0V, V_{EE} = ØV, and V_{CCP} = +10V. PECL outputs are designed to be terminated with 50Ω to +3.0V.

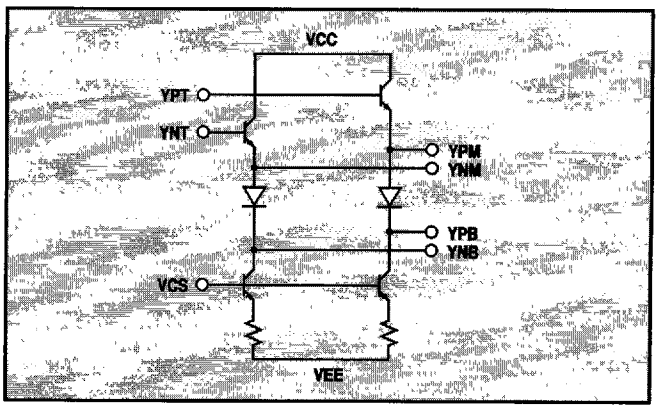
The Lightning CML I/O configuration is intended for the highest speed applications. The CML output is open collector and is designed to be terminated with 50Ω to GND. The CML input cell provides an on-chip 50Ω terminating resistor for optimized signal integrity.

Core Cells

The LI300 array contains 120 core cells, while the LI1000 contains 504. A single core cell can implement any three-level function such as a 3-input logic gate, 2-to-1 mux, or latch; only two cells are required for more complex functions such as data flip flops, adders, or 4-to-1 mux's. The LI300 array can contain up to 60 flip flops (252 in the LI1000) or 120 logic trees (504 in the LI1000). Each logic tree can implement a three-level logic gate.

Core cells are arranged in rows with routing channels placed between. Each core cell contains 11 transistors and two diodes that can be connected to form a three-level logic tree with a level shift. The logic tree output can drive the top logic input of the next cell without any level shifting or buffering. As seen in figure 8, an emitter follower level shift is used between gates to produce two lower logic levels used to drive BPM/BNM and CPB/CNB inputs of driven cells.

Figure 8
Schematic of Lightning level shift function

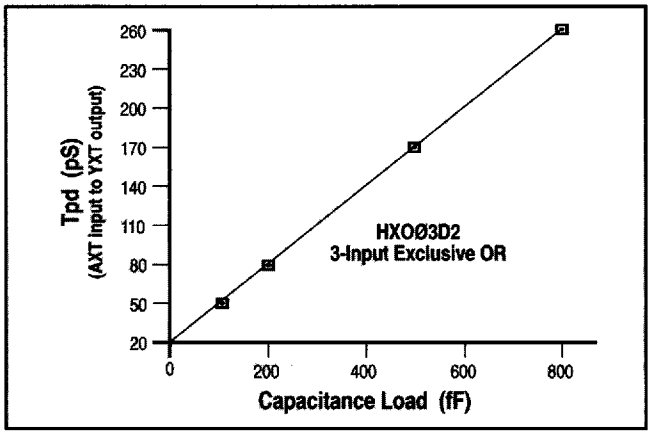


The middle logic level output is generated directly from the emitter follower, while the bottom level is generated from the diode. The cell library includes both level shifted and non-level shifted versions. Diodes are only needed for the level shift function.

All internal cells—and most I/O—are provided with three speed/power configurations. This allows the designer to select the precise performance required for every path in the circuit while minimizing power dissipation

To maximize performance, Rockwell has developed a state-of-the-art polyimide dielectric for reduced capacitance on signal routing. The use of this dielectric significantly decreases loading capacitance and delay on critical paths. Figure 9 shows the predictable nature of a typical macro's performance versus loading.

Figure 9
Performance versus loading for a 3-input exclusive-OR gate



Power Supplies

The Lightning arrays use standard supplies for ECL-only, CML-only, and mixed ECL/CML designs; -5.2V, GND, and +5.0V are the only supplies required. Lightning arrays can also operate in PECL-only mode using +5.0V, GND, and +10V supplies. All power must be controlled to within ±5%.

Macrocell Library

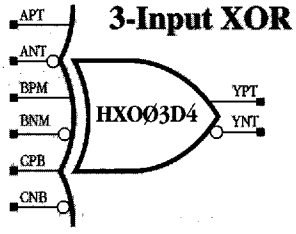
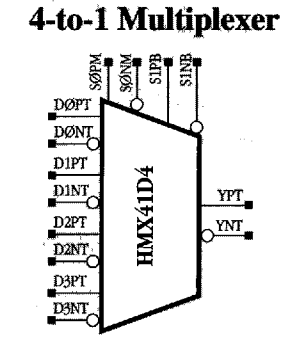
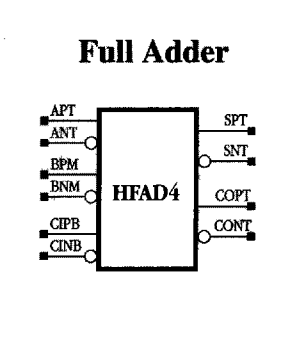
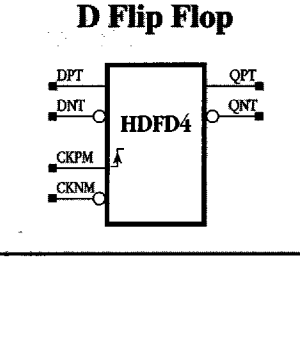
Internal macros range from simple logic gates to larger functions such as full adders, mux's, and flip flops. Most cells include low power, standard, and high performance versions and include a level shift circuit for output signals compatible with the lower level inputs of driven macros.

The list at right represents the cells currently available in the Lightning macro library. New cells are continually being developed and the user is advised to consult with the factory for desired functions not on this list. The performance of selected macros are given on the next page. For detailed specifications for other macros, see the Lightning Series design manual.

Macro Name	Function	Cells Required
Input/Output Cells		
HCDID12	CML Differential Input, High Speed	2 I/O Cells
HCDODX[1]	CML Differential Output	2 I/O Cells
HEDIDX[2]	ECL Differential Input	2 I/O Cells
HEDODX[1]	ECL Differential Output	2 I/O Cells
HESIDX[2]	ECL Single-ended Input	1 I/O Cell
HESODX[1]	ECL Single-ended Output	1 I/O Cell
Simple Gates		
HANØ2DX[2,3]	2-Input AND Gate	1
HANØ3DX[2,3]	3-Input AND Gate	1
HAOØ3DX[2,3]	2/1 AND-OR Gate	1
HLSØ1DX[2]	Level Shift	1
HNIØ1DX[2,3]	Non-inverting Buffer	1
HOAØ3DX[2,3]	2/1 OR-AND Gate	1
HORØ2DX[2,3]	2-Input OR Gate	1
HORØ3DX[2,3]	3-Input OR Gate	1
HXOØ2DX[2,3]	2-Input Exclusive-OR Gate	1
HXOØ3DX[2]	3-Input Exclusive-OR Gate	1
Multiplexers		
HMX21DX[2,3]	2-to-1 Multiplexer	1
HMX41DX[2,3]	4-to-1 Multiplexer	2
Adders		
HFADX[2]	1-Bit Binary Full Adder	2
HHADX[2,3]	1-Bit Binary Half Adder	2
Latches		
HDLDX[2,3]	Latch	1
HDLMDX[2]	Latch with Multiplexed Inputs	1
HDLRDX[2]	Latch with RESET	1
HDLSDX[2]	Latch with SET	1
Flip Flops		
HDFDX[2,3]	D Flip Flop	2
HDFMDX[2,3]	D Flip Flop with Multiplexed Inputs	2
HDFRDX[2,3]	D Flip Flop with RESET	2
HDFSDX[2,3]	D Flip Flop with SET	2
HTFRDX[2,3]	Toggle Flip Flop with RESET	2

NOTES
[1] Macro is available in low and standard power versions.
[2] Macro is available in low, standard, and high power versions
[3] Macro is available with level shift in all power versions.

Macrocell Examples (V_{CC} = ØV, V_{EE} = -5.2V, T_C = 25 °C, intrinsic propagation delay)

Parameter	Min	Typ	Max	Units	Function/Symbol
Propagation Delay					
AXT to **YXT**	—	17	—	ps	
BXM to **YXT**	—	30	—	ps	
CXB to **YXT**	—	45	—	ps	
Load Dependent Delay					
Delay/Fan-out	—	6	—	ps	
Delay/mm wire	—	37	—	ps	
Power Dissipation	—	10.4	—	mW	
Propagation Delay					
DØXT to **YXT**	—	17	—	ps	
D1XT to **YXT**	—	17	—	ps	
D2XT to **YXT**	—	17	—	ps	
D3XT to **YXT**	—	17	—	ps	
SØXM to **YXT**	—	30	—	ps	
S1XB to **YXT**	—	45	—	ps	
Load Dependent Delay					
Delay/Fan-out	—	6	—	ps	
Delay/mm wire	—	37	—	ps	
Power Dissipation	—	10.4	—	mW	
Propagation Delay					
AXT to **SXT**	—	17	—	ps	
BXM to **SXT**	—	30	—	ps	
CIXB to **SXT**	—	45	—	ps	
AXT to **COXT**	—	17	—	ps	
BXM to **COXT**	—	30	—	ps	
CIXB to **COXT**	—	45	—	ps	
Load Dependent Delay					
Delay/Fan-out	—	6	—	ps	
Delay/mm wire	—	37	—	ps	
Power Dissipation	—	20.8	—	mW	
Propagation Delay					
CKXM to **QXT**	—	30	—	ps	
T_{SET-UP}	—	45	—	ps	
T_{HOLD}	—	25	—	ps	
Load Dependent Delay					
Delay/Fan-out	—	6	—	ps	
Delay/mm wire	—	37	—	ps	
Power Dissipation	—	20.8	—	mW	

Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Units	Notes
T_{STOR}	Storage Temperature	-65 to +150	°C	
T_J	Junction Temperature	-55 to +150	°C	
T_C	Case Temperature Under Bias	-55 to +125	°C	
V_{CC}	ECL/CML, V_{CC} Supply Voltage	GND	V	
V_{EE}	ECL/CML, V_{EE} Supply Voltage	V_{CC} (GND) to -6.0	V	
V_{CCP}	ECL, V_{CCP} Supply Voltage	V_{CC} (GND) to +6.0	V	
V_{CC}-PECL	PECL, V_{CC} Supply Voltage	V_{EE} (GND) to +6.0	V	[5]
V_{EE}-PECL	PECL, V_{EE} Supply Voltage	GND	V	[5]
V_{CCP}-PECL	PECL, V_{CCP} Supply Voltage	+5.0 to +11.0	V	[5]
V_{CMLIN}	Voltage Applied to Any CML Input; Continuous	-1.0 to +0.5	V	[2]
V_{ECLIN}	Voltage Applied to Any ECL Input; Continuous	-2.5 to +0.5	V	[2]
V_{PECLIN}	Voltage Applied to Any PECL Input; Continuous	+2.5 to +5.5	V	[2,5]
I_{CMLIN}	Current Into Any CML Input	-20 to +20	mA	[3]
I_{ECLIN}	Current Into Any ECL/PECL Input	-0.1 to +0.1	mA	[3]
V_{CMLOUT}	Voltage Applied to Any CML Output	-2.0 to +0.5	V	[2,4]
V_{ECLOUT}	Voltage Applied to Any ECL Output	-3.0 to +0.5	V	[2,4]
$V_{PECLOUT}$	Voltage Applied to Any PECL Output	+2.0 to +5.5	V	[2,4,5]
I_{CMLOUT}	Current From Any CML Output; Continuous	-24	mA	
I_{ECLOUT}	Current From Any ECL/PECL Output; Continuous	+24	mA	

NOTES
[1] Sustained application may result in damage to the device Each parameter may be applied to the device one at a time
[2] Device under test is powered up with nominal supply voltages
[3] Subject to input voltage requirements
[4] Subject to output current requirements
[5] V_{CC} = +5.0V, V_{EE} = ØV

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Notes
V_{CC}	ECL/CML, V_{CC} Supply Voltage	—	Ø V	—	[1]
V_{EE}	ECL/CML, V_{EE} Supply Voltage	-4.9 V	-5.2 V	-5.5 V	[2]
V_{CCP}	ECL/CML, V_{CCP} Supply Voltage	+4.5 V	+5.0 V	+5.5 V	[3]
V_{CC}-PECL	PECL, V_{CC} Supply Voltage	+4.75 V	+5.0 V	+5.25 V	[2]
V_{EE}-PECL	PECL, V_{EE} Supply Voltage	—	Ø V	—	[1]
V_{CCP}-PECL	PECL, V_{CCP} Supply Voltage	+9.5 V	+10 V	+10.5 V	[3]
R_{LD}-CML	CML Output Termination Load	—	50 Ohms	—	[4]
R_{LD}-ECL	ECL/PECL Output Termination Load	—	50 Ohms	—	[5]
T_{CC}	Commercial Case Temperature	0 °C	—	+70 °C	[6]
T_{CI}	Industrial Case Temperature	-40 °C	—	+85 °C	[6]
T_{CM}	Military Case Temperature	-55 °C	—	+125 °C	[6]

NOTES:
[1] V_{CC} is typically connected to the ground plane (in PECL mode, V_{EE}-PECL is connected to the ground plane)
[2] Power supply variation should be within ±5%
[3] V_{CCP} power supply is used only to provide true ECL output high voltage
[4] CML outputs terminated with 50 Ohms to ground Both the true and complement outputs must be terminated.
[5] ECL outputs terminated with 50 Ohms to -2 0V, PECL outputs terminated with 50 Ohms to +3.0V
Both true and complement outputs must be terminated
[6] Case temperature is measured at the heat sink side of the package

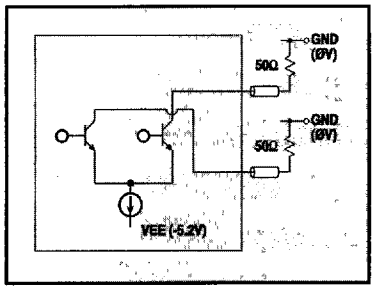
DC Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions	Notes
CML I/O							
V_{OH}	Output Voltage High	—	-20	—	mV	Load: 50 Ohms to ØV (GND)	[1]
V_{OL}	Output Voltage Low	—	-400	—	mV	Load: 50 Ohms to ØV (GND)	[1]
V_{IH}	Input Voltage High	—	-100	—	mV		[1]
V_{IL}	Input Voltage Low	—	-300	—	mV		[1]
I_{IH}	Input High Current	—	-2	—	mA		
I_{IL}	Input Low Current	—	-8	—	mA		
ECL I/O							
V_{OH}	Output Voltage High	—	-1.0	—	V	Load: 50 Ohms to -2.0V	[2]
V_{OL}	Output Voltage Low	—	-1.6	—	V	Load: 50 Ohms to -2.0V	[2]
V_{IH}	Input Voltage High	—	-1.2	—	V		
V_{IL}	Input Voltage Low	—	-1.4	—	V		
I_{IH}	Input High Current	—	50	—	µA		
I_{IL}	Input Low Current	—	50	—	µA		
PECL I/O							
V_{OH}	Output Voltage High	—	4.0	—	V	Load: 50 Ohms to +3.0V	[3]
V_{OL}	Output Voltage Low	—	3.4	—	V	Load: 50 Ohms to +3.0V	[3]
V_{IH}	Input Voltage High	—	3.8	—	V		
V_{IL}	Input Voltage Low	—	3.6	—	V		
I_{IH}	Input High Current	—	50	—	µA		
I_{IL}	Input Low Current	—	50	—	µA		

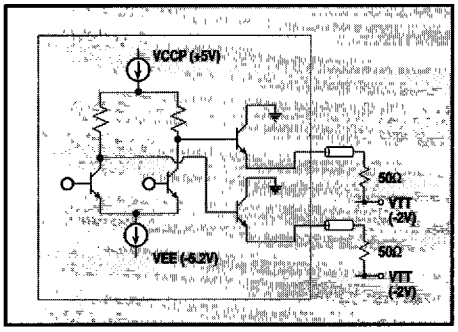
NOTES
[1] Assumes all I/O signals are differential
[2] Assumes V_{CCP} = +5.0V.
[3] Assumes V_{CC} = +5.0V, V_{EE} = ØV, V_{CCP} = +5 5V

AC Test Load for Output Buffers

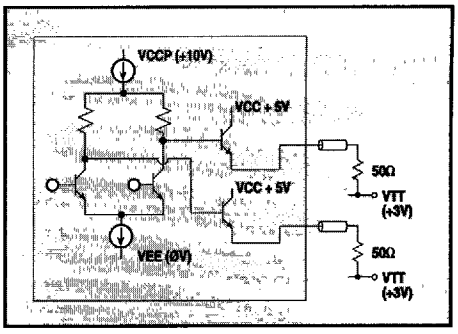
CML Output Load



ECL Output Load



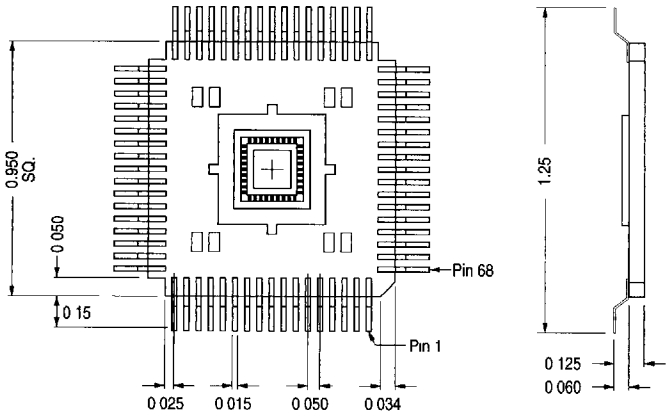
PECL Output Load



Packaging

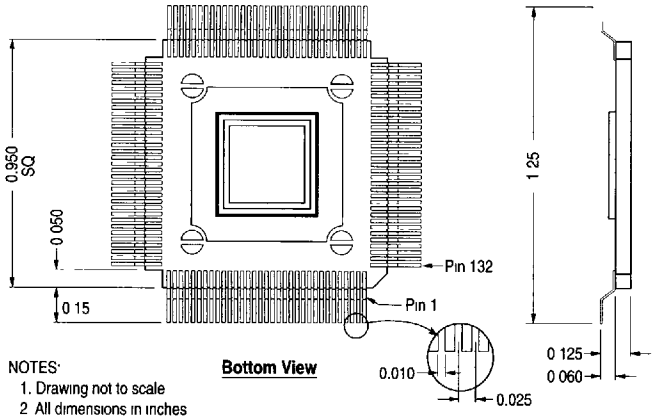
Figures 10, 11, and 12 below show outlines of the packages currently available for Lightning designs. The 68- and 132-pin LCC packages—intended for the LI300 and LI1000, respectively— feature a high performance, cavity-down, multi-layer ceramic design. These packages provide controlled impedance signal lines, isolated power and ground planes, good cross talk control, and low thermal resistance. The 52-pin PQFP—intended for LI300 designs only—features an integral heat spreader and excellent electrical characteristics in a low cost molded plastic package design. Contact factory for the latest information regarding additional packages that may be available for Lightning gate arrays.

Figure 10
68 lead high speed ceramic package for LI300 designs



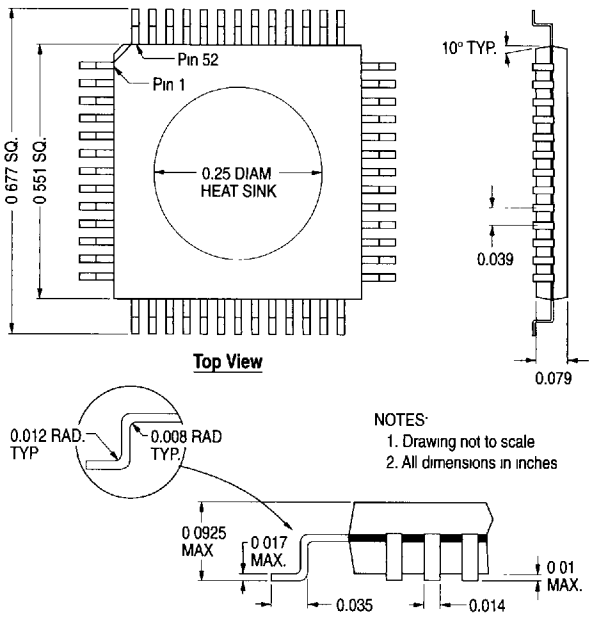
NOTES
1 Drawing not to scale
2 All dimensions in inches
3 Package body: cofired alumina ceramic, metalization/plating: gold

Figure 11
132 lead high speed ceramic package for LI1000 designs



NOTES·
1. Drawing not to scale
2 All dimensions in inches
3. Package body· cofired alumina ceramic, metalization/plating. gold

Figure 12
52 lead high performance plastic package for LI300 designs



NOTES·
1. Drawing not to scale
2. All dimensions in inches

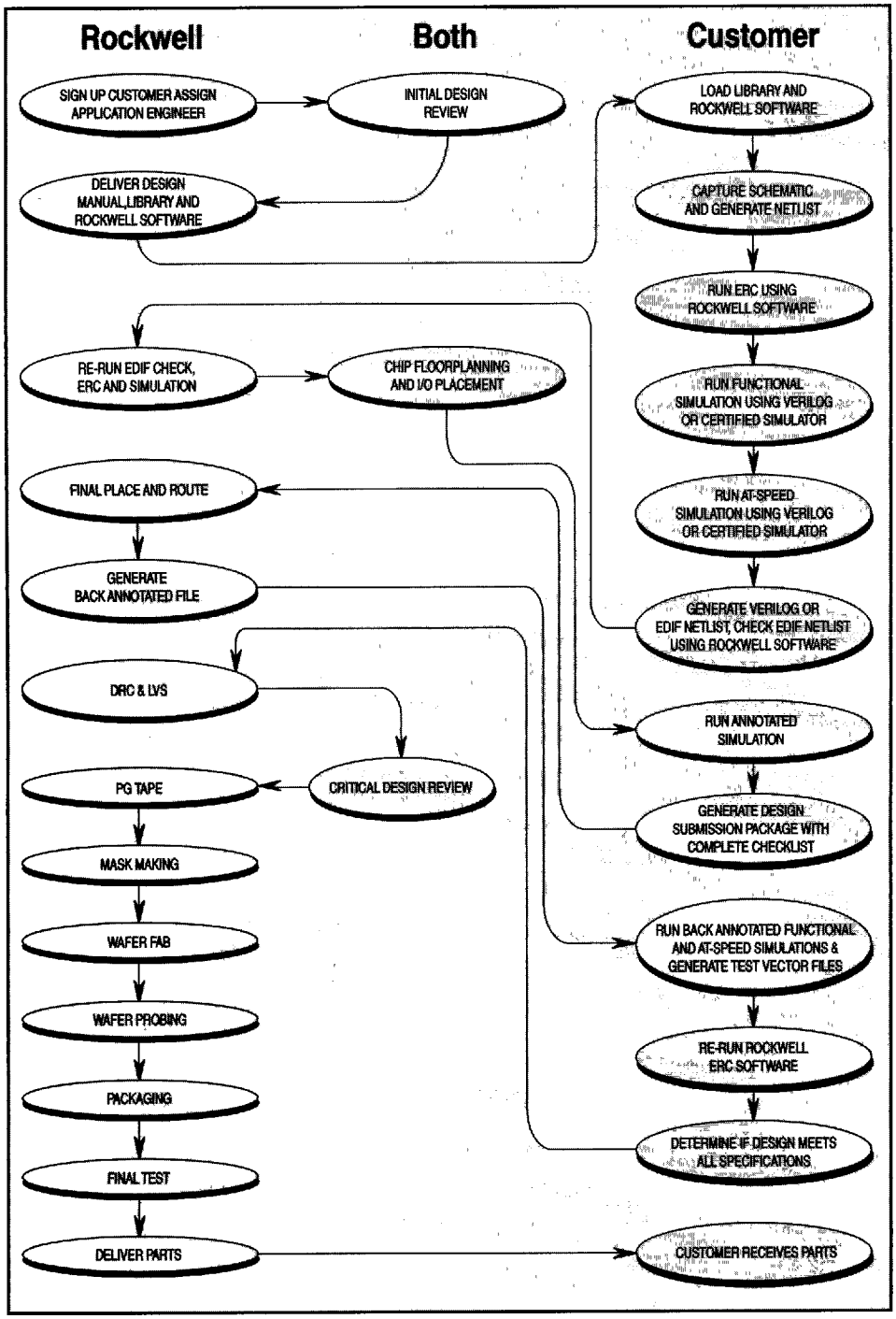
Implementation

Rockwell's design methodology is designed to be efficient, flexible, and reliable. Customers can choose to do the design, or have Rockwell engineers perform a turn-key implementation based on a detailed set of specifications. A Rockwell engineer is assigned to every customer to track progress and answer questions. In every design, the following steps are normally performed by Rockwell's application engineers.

- Final placement of macrocells
- Routing of metal interconnection
- Extraction of back-annotated net-lengths
- Final design rule checks
- Layout versus schematic verification

Figure 13 shows the flow and delegation of responsibilities when the customer chooses to do the implementation.

Figure 13
The customer implementation option

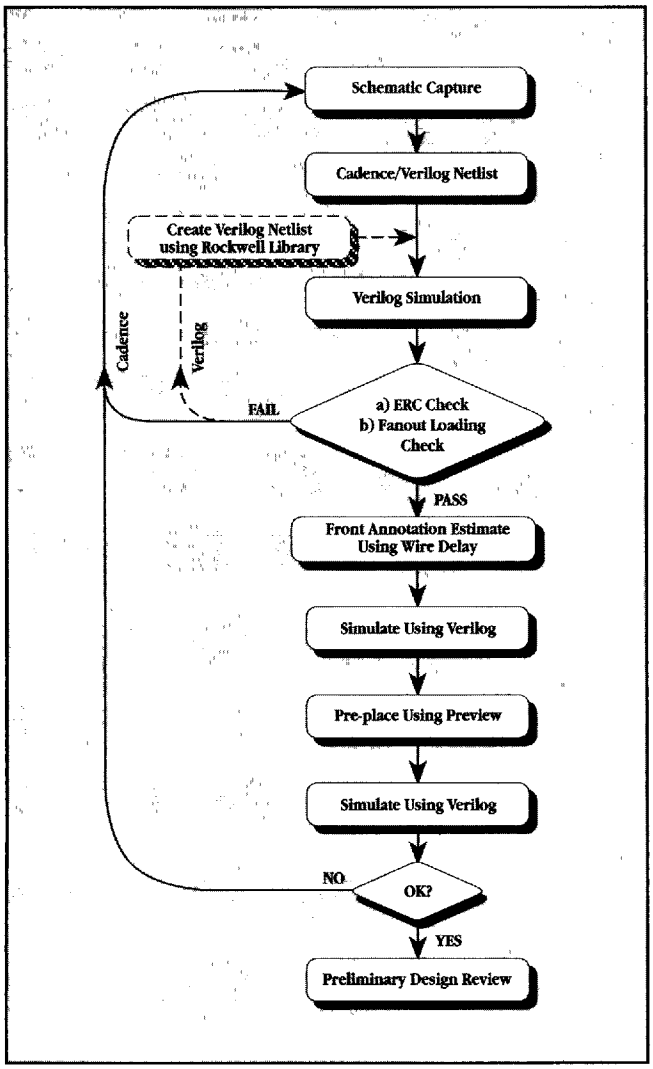


Design Support

Lightning Series designs are currently supported through the use of the Cadence/Verilog platform. Figure 14 illustrates the design methodology employed with the Cadence/Verilog tools. Front-end design support is also currently under development for Mentor and Viewlogic, and logic synthesis through Synopsys.

Front-end critical path evaluation is supported by Rockwell's GT-Estimater™ path delay calculator, which is designed to operate on virtually any DOS PC. The program allows a designer to build and evaluate complex combinatorial paths from macro elements found in the Lightning macrocell library.

Figure 14
Design flow using Cadence/Verilog



Test

Rockwell's testing procedure includes several steps to ensure full functionality of finished devices. A state-of-the-art HP83000 tester (see figure 15) is employed. The HP83000 features a tester-per-pin architecture that currently supports up to 112 I/O (expandable to 1024). The HP83000 tests at a maximum rate of 660 MHz, though 1.3 GHz is achievable by multiplexing pins. The tester provides 10 ps resolution and 50 ps accuracy.

Test Vector Requirements

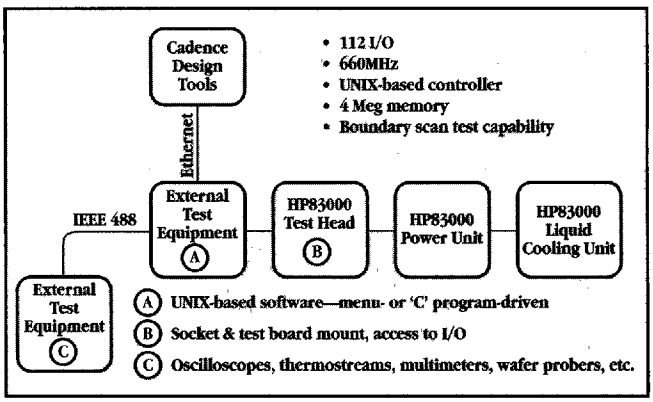
For all Lightning designs, Rockwell requires that the customer supply functional test vectors in combination with either a set of critical path vectors or a set of at-speed vectors. The use of at-speed or critical path delay vectors depends on the specific requirements of each customer, and a brief description of each follows:

Functional Vectors—These vectors are used to test functionality and can be performed on devices in die form or in a package. Functional vectors specify combinations of input stimuli and the resulting outputs for all paths. These vectors can be generated from simulations at 10 MHz and must be timing-independent.

Critical Path Delay Vectors—These vectors are used to verify the timing of critical paths. The timing relationships between all input stimuli and their associated effect on outputs of critical paths must be defined.

At-Speed Vectors—These vectors verify timing requirements and full speed functionality. For designs operating at speeds up to 660 MHz, testing is carried out on the HP83000 tester. If the design requires testing at greater than 660 MHz, critical path vectors must be provided.

Figure 15
Hewlett Packard HP83000 tester



Ordering Information

Rockwell Lightning arrays are available with different operating temperature ranges, I/O types, and package options. The order number is formed by using a combination of the device type (LI300, or LI1000), I/O type, package type, and temperature of operation.

LI300-F-M

DEVICE TYPE:
LI300 = 300 equivalent gates
LI1000 = 1000 equivalent gates

OPERATING TEMPERATURE RANGE:
C = Commercial (0 to 70 °C)
I = Industrial (-40 to +85 °C)
M = Military (-55 to +125 °C)

PACKAGE TYPE:
P = 52-pin Plastic Quad Flatpack (LI300 only)
F = Leaded Ceramic Chip Carrier
(68-pin, LI300 only; 132-pin, LI1000 only)

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