LSI LOGIC CORPORATION

LL5000 Series
Silicon-Gate HCMOS Logic Arrays

S-121 Prc Only

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General

The LL5000 series of silicon-gate HCMOS logic arrays from LSI LOGIC CORPORATION exhibits bipolar speeds, while at the same time, offers low power consumption, high noise margins, and ease of design of HCMOS. The LL5000 series is implemented in silicon-gate 3-micron drawn gate length, dual-layer metal interconnection technology. A ranges of complexities from 504 to 5902 blocks is offered; each block is equivalent to a 2-input NAND or NOR gate. Maximum pin counts range up to 180.

The speeds and densities of the LL5000 series make it suitable for LSI implementation of complete, high-performance functions such as special processors, dedicated peripheral controllers and intelligent support chips. It is also ideal for replacement of LS/S TTL logic in medium-and high-speed systems. IC count can be reduced by factors of tens to hundreds depending on the density of the array used. Power requirements can be reduced by several orders of magnitude, reliability significantly enhanced and the total size and cost of the system similarly reduced.

Features

- Silicon-gate 3 micron (drawn) HCMOS technology
- Speeds comparable to 74S TTL — 2.5ns through 2-input NAND gate and interconnection, $T_A = 25°C$, fanout = 2, $V_{DD} = 5V$
- Optimal block structure of 2N and 2P transistors
- Complexities ranging from 504 to 5902 blocks
- Pin counts ranging up to 180
- Fully supported by LDS™ (LSI Design System), Daisy LOGICIAN*, Mentor Graphics IDEA 1000*, Valid Logic SCALDsystem* and FutureNet Dash-1 Schematic Designer* Systems
- Extensive macrocell and macrofunction libraries
- Most non-power pads configurable as inputs, outputs or bidirectional I/O
- TTL/CMOS I/O compatibility
- Configurable output drive up to 12mA under worst-case commercial conditions
- All inputs and outputs protected from over-voltage and latch-up
- LL5220Q evaluation device available
- Full military capability
- Ceramic and plastic packages
- Alternately-sourced by Toshiba, RCA, GE/Intersil and SGS

Product Outline

Device Number	Gate Complexity	Max[3] I/O	V_{DD} Pads	V_{SS} Pads	Max Pads	Gate Speed (ns)[1]	
						Typ	Max[2]
LL5050	504	44	2	6	52	2.5	4.5
LL5080	880	66	2	6	74	2.5	4.5
LL5140	1417	84	2	6	92	2.5	4.5
LL5170	1708	88	2	6	96	2.5	4.5
LL5220	2224	106	2	6	114	2.5	4.5
LL5320	3192	126	4	8	138	2.5	4.5
LL5420	4202	144	4	8	156	2.5	4.5
LL5600	5902	168	4	8	180	2.5	4.5

Notes:

1. 2-input NAND gate, fanout = 2, and typical interconnection
2. $T_A = 0$ to $70°C$, $V_{DD} = 5V \pm 5\%$
3. It may be necessary to configure additional I/O pads for V_{DD} and V_{SS}, depending on the number and drive of the output buffers. See section on "V_{DD} Requirements".

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Product Description

The LL5000 series of arrays is manufactured using an advanced 3-micron, oxide-isolated silicon-gate HCMOS fabrication process. The use of short channel lengths, thin gate oxides and two levels of metal interconnection provides bipolar speeds. The small device structures and low power consumption also allow high block counts due to the smaller chip size and the minimal heat dissipation.

Macrocells

The arrays consist of columns of blocks in the core region, I/O buffers around the periphery, and wiring channels in-between. Each block consists of 2N and 2P transistors. These blocks can be configured into a variety of logic elements such as exclusive-OR gates or flip-flops using unique metal interconnections. These elements are called macrocells, and are the basic building blocks available to the user. The LL5000 series contains approximately 145 macrocells. Macrocells needed to support scan testing are available.

Macrofunctions

To specify his logic, the user often defines elements of greater complexity. These more complex elements are called macrofunctions. They are composed of macrocells. Simple macrofunctions are in turn used to hierarchically build higher-level macrofunctions until the logic is completely specified.

For user convenience, a selection of macrofunctions composed of macrocells is also available in the LL5000 library. These macrofunctions implement generic functions such as counters, decoders, shift registers, etc., and are optimized for gate usage and for performance characteristics. Under some circumstances, such as for upgrading existing products using 7400/4000/2900 series MSI/SSI functions, or because of previous familiarity, designers may prefer to use 7400/4000/2900 series functions as building blocks. A large selection of these elements is also provided in the LL5000 series macrofunction library.

Table 1 lists some representative macrofunctions. Detailed information on available macrocells and macrofunctions is provided in other LSI LOGIC publications. The "AC Characteristics" section lists some of the commonly used macrofunctions, their propagation delays and their complexity.

Macrocells for Level-Sensitive Scan Design

The LL5000 series macrocell libraries also contain macrocells needed to support scan testing. Scan testing simply involves the capability to serially shift the contents of all internal flip flops off-chip in a test mode. (See LSI LOGIC Application Note A32 on "Testing Logic Arrays" for more details.)

I/O Buffers

Each I/O buffer around the perimeter of the array consists of an input protection circuit and large N- and P-channel transistors for driving off-chip loads. Eight to

ADDERS Up to 16 bits **COMPARATORS** Magnitude Equality 4 and 8 bits **PARITY GENERATORS** 8-bit odd parity detector **REGISTERS** 8-bit data latch 8-bit data register, clear direct 4-bit shift register, sync parallel load and clear 4-bit shift register, async parallel load **COUNTERS** Binary, BCD, Gray and Johnson counters in a variety of configurations Large modulo counters **CLOCK GENERATORS** Two-phase clock generator, buffered	**DECODERS** 2-4 decoders 3-8 decoders 4-10 decoders **ALUs** 8 and 16-bit 74181 type 8 and 16-bit 100181 type **2900 FAMILY** 2901 2909 2910 2911 **FIFO** 16 x 4 **MULTIPLIERS** 8 x 8 12 x 12 16 x 16 **BARREL SHIFTERS** 8 bit 16 bit

Table 1. Representative Macrofunctions Available in the LL5000 Series

12 dedicated power and ground pads are provided. All the remaining peripheral cells can be used as input, output or bidirectional 3-state. If necessary, they can even be used to buffer heavily loaded internal signals. Further flexibility is available in the use of pullup/pulldown resistors and choice of input levels and current drive:

- All I/O pads have pullup and pulldown resistors available (typically 880kΩ).
- Output drive may be tailored to 1.0mA, 2.0mA or 4.0mA. Additional drive capability may be obtained by paralleling two (8.0mA) or three (12.0mA) drivers.
- Three input voltage level options are available on any input/output pin. CMOS input buffers provide standard 1.5V and 3.5V input levels. TTL input buffers provide standard 0.8V and 2.0V (2.25V on industrial and military devices) input levels. Schmitt trigger inputs provide 1.5V of hysteresis. See the "DC Characteristics" section for more details.
- All I/Os are protected against latch-up and static discharge.

Propagation Delays

Propagation delays of the LL5000 series logic elements are a function of several factors

- fanout,
- interconnection routing,
- junction temperature,
- supply voltage,
- processing tolerance,
- input transition time, and,
- input signal polarity.

The LDS Design Verifier™ generates the propagation delays for all networks automatically once the network has been entered into the development system or workstation. Prior to layout, these values are based on the estimated interconnections. After layout, the program is re-run and final delay values based on actual interconnections are obtained.

Prior to availability of the network in computer format, approximate delay calculations may be used. This may be done as follows:

Propagation delays for some popular macrocells are shown in the "AC Characteristics" section for nomimal processing, 5V operation, 25°C temperature and for various fanouts, with statistically estimated wirelengths.

The effect of temperature may be estimated from Figure 1. The maximum junction temperature will determine a temperature multiplier (K_T). The LSI LOGIC. macrocell manual should be consulted for package thermal resistances. In CMOS technology, the junction temperature is usually close to the ambient temperature. Similarly, Figure 2 shows the effect of supply voltage (K_V). LSI LOGIC assumes a 40% variability resulting from all other factors including processing, a factor of 1.4 for the worst-case processing multiplier (K_O).

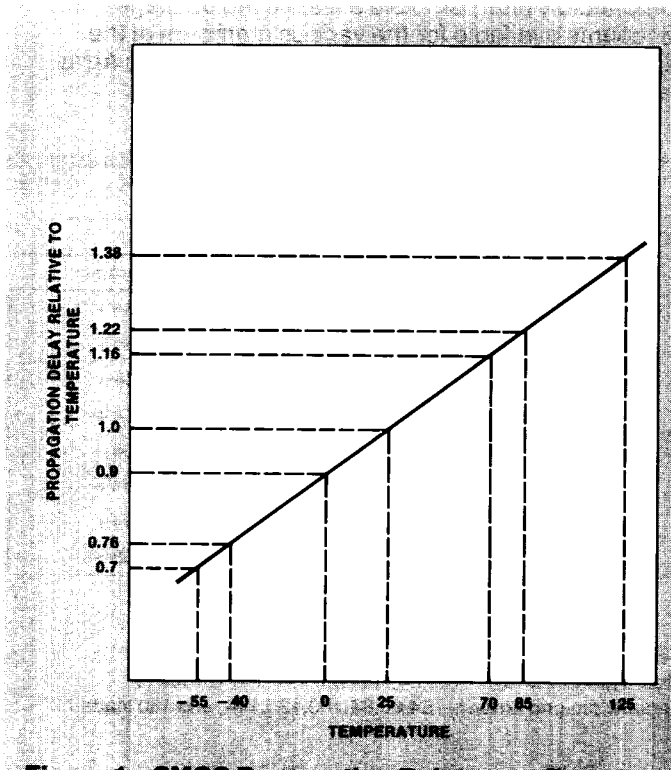


Figure 1. CMOS Propagation Delays as a Function of Temperature

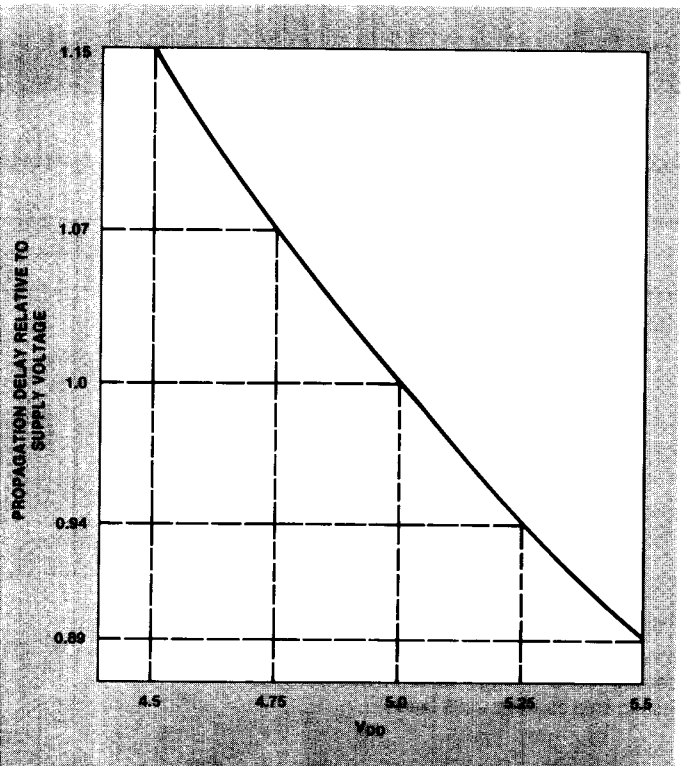


Figure 2. CMOS Propagation Delays as a Function of Supply Voltage

The maximum propagation delay is

$$T_{MAX} = K_O \bullet K_T \bullet K_V \bullet T_{TYP}$$

A simple example will illustrate the technique.

The circuit of Figure 3 must operate over 0°C to 70°C, and 4.75V to 5.25V power supply voltage. Using Figures 1 and 2 and the K_O multiplier, we determine the worst-case maximum delay to be $1.4 \times 1.16 \times 1.07 = 1.74$ times the typical delay.

The FD1 flip-flop, clocked by the signal CLK, feeds an A02 AND-NOR gate combination and three other loads. The A02 drives a BTS1 3-state buffer directly. The BTS1 drives off-chip, through a PC board, and on to another array using a TLCHT input level shifter. The total capacitance at the output, interconnect, and input is 50pF. The TLCHT drives the D input of an FD1 D flip-flop (whose equivalent input loading is 2) and two other loads for an equivalent F.O. = 4. The delay characteristics of all the macrocells are tabulated in Table 2. The total clock-to clock delay is 20.8ns typical, $20.8 \times 1.74 = 36.2$ns worst-case. LDS programs are used to obtain accurate delays after the logic has been entered into the system.

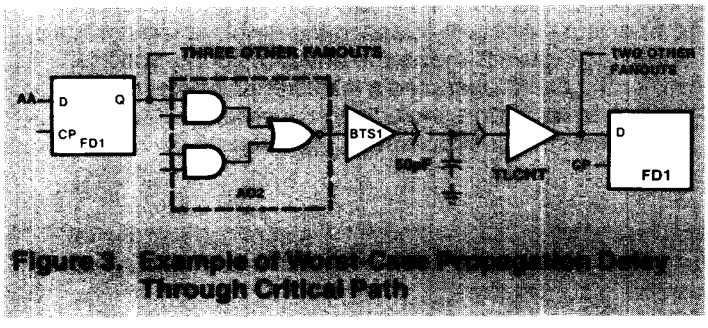


Figure 3. Example of Worst-Case Propagation Delay Through Critical Path

Input Signal AA	FD1 FO = 4	A02 FO = 5	3-State Output BTS1 C_L = 50pF	TLCHT FO = 4	FD1 Set-up Delay	Typical Path Delay	WC Path Delay
Goes high	tpdLh 7.9	tpdhL 3.4	tpdhL 8.8	tpdhL 3.6	2.5	26.2	45.6
Goes low	tpdhL 5.7	tpdLh 11.1	tpdLh 8.8	tpdLh 2.5	2.5	30.6	53.2

Table 2. Propagation Delay Calculation

Product Options Available

The LL5000 series is offered in a variety of operating temperature ranges and production processing flows. The following standard operating temperature ranges are offered.

- Military (−55°C to +125°C)
- Industrial (−40°C to +85°C)
- Commercial (0°C to +70°C)

Other special temperature ranges are also available.

Production flow options other than LSI LOGIC's standard commercial flow are available. Various military flows including MIL-STD-883 Level C are supported. Full MIL 38510 qualification is available when required.

Packaging

The LL5000 series can be packaged in a variety of plastic and ceramic dual-in-line packages, leadless and leaded chip carriers, and pin grid arrays. The compatibility chart of Table 3 shows the packages and pin counts available for the various members of the LL5000 series. See Application Note A33, Logic Array Packaging, for more details.

Device	Dual-In-Line Packages		Chip Carriers		Pin Grid Arrays	
	Plastic	Ceramic	Plastic	Ceramic	Plastic	Ceramic
LL5050	24 +	24 +	68	28 +	N/A	64 +
LL5080	24 +	24 +	68	28 +	68 +	64 +
LL5140	24 +	24 +	68	44 +	68 +	64 +
LL5170	24 +	24 +	68	44 +	68 +	64 +
LL5220	40 +	24 +	68	44 +	68 +	64 +
LL5320	40 +	40 +	68	68 +	68 +	64 +
LL5420	N/A	64 +	68	68 +	68 +	64 +
LL5600	N/A	64 +	68	68 +	68 +	68 +

Package families include:

Plastic DIPs — 24,28,40,48 and 64 (0.070" pitch) leads
Ceramic DIPs — 24,28,40,42,48 and 64 leads
Plastic chip carriers — 68 leads
Ceramic chip carriers — 28,44,52,68,84, and 100 leads
Plastic pin grid arrays — 68,84,100,120,144 and 180 leads
Ceramic pin-grid arrays — 64,68,84,100,120,144, and 180 leads

Table 3. Package Selector Guide for the LL5000 Series

LL5220Q Evaluation Device

A potential user of the LL5000 series can, prior to design commencement, measure its performance under his unique system and environmental conditions. The LL5220Q contains a variety of logic functions such as 2-, 3-, or 4-input NAND gates, 2- or 4-input NOR gates, output buffers with different drive capability, a variety of different flip-flops, inverters, TTL-to-CMOS level-shifters, etc. In addition, complex circuits such as ALUs and up-down counters are included. These functions are implemented in several different test circuits. Technology parameters such as propagation delays, power consumption, input/output characteristics, etc., can be measured under different conditions of loading, supply voltage, ambient temperature, etc. See the LL5220Q data sheet for more details.

Getting Started on the Design

To get started on a logic array design, the following sequence of preliminary steps is suggested.

1. The complete system is partitioned into LSI building blocks. An effort should be made to minimize the I/O count when partitioning between circuits. Each functional block to be implemented in a logic array is then converted to a logic schematic. The user can describe his logic using LSI LOGIC's macrofunction/macrocell libraries or 7400/4000/2900 series functions. The use of hierarchical design techniques on the LDS design system allows design expression at these various levels. Ultimately, when the logic is compiled on LDS, it is "flattened" into macrocells. It is advisable to structure the complete schematic as a set of functional sub-systems such as a 16-bit ALU, a data receiver, a programmable timer or a register file, to allow comprehensible and easy hierarchical simulation.
2. The base clock frequency and the critical path timing are necessary to make the correct choice of technology. The LL5000 series can support designs operating up to 25MHz. The critical path timing is determined based on macrocell propagation delays (see the "Propagation Delays" and "AC Characteristics" sections). To verify the capability of a technology under the unique environmental and system conditions of a user application, an evaluation device such as the LL5220Q may be used.
3. The next step is an estimation of the gate count and I/O requirements of the logic to establish the complexity of the array required. For gate count equivalence tables for the 7400/4000/2900 series or LSI LOGIC macrocells/macrofunctions, see LSI Application Note A31. The gate utilization actually achieved in a given array for a specific design depends on the gate count, pin requirements, and factors that affect routability. For example, block-oriented logic with minimum inter-block interaction provides high utilization, whereas wide, extensive bussing lowers it.
4. Finally, a choice of array size, package, temperature range, performance, etc., is made.

During all these steps, the customer usually consults LSI LOGIC to ensure compatibility and completeness.

A set of specifications is then submitted to LSI LOGIC. After their acceptance, the logic designer takes the one week LDS training class and starts his design. The design process and the user interface to LDS are oriented toward the skills of a system designer rather than a semiconductor device or VLSI designer.

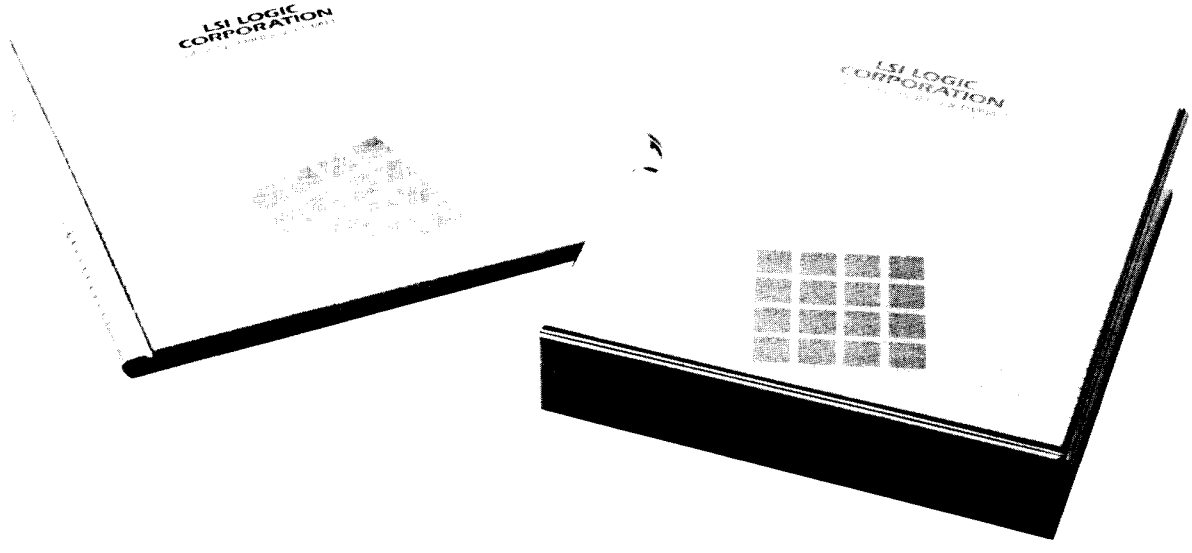
Alternatively, the customer can contract LSI LOGIC for a turnkey design.

Design Support and Interface

The LDS System may be used for logic specification, basic network verification (gate usage, I/O pad usage, average fanout per net, estimated automatic wireability), logic simulation and performance analysis, automatic placement and routing, resimulation with actual wire-lengths to verify the AC performance, mask, P.G. tape generation and test tape generation. The basic design flow is outlined in Figure 7.

Workstations

LSI LOGIC Corporation can provide complete support packages for Daisy, Mentor, Valid and FutureNet Data Systems. This permits LL5000 series logic elements to be entered schematically, design verified and simulated on these popular workstations (schematic entry only on FutureNet). See the LSI LOGIC Design Workstation Software Brochure for more details.



Design Verifier 5K Series

V_{DD} and V_{SS} Requirements

HCMOS is a fast technology rivaling Schottky TTL speeds. High-speed operation places stringent requirements on the ground bussing and the number of power and ground pads required to avoid current spikes when the output buffers charge and discharge their output capacitance.

To increase noise immunity, two ground busses (V_{SS} and V_{SS2}) are used on the array. All inputs and interior logic are on the V_{SS2} bus, all output buffers on the V_{SS}.

More than two power (V_{DD}) and ground (V_{SS}) pins may be required to support several high-drive outputs switching simultaneously at fast speeds. For example, the type B1 buffer has a low impedance for high drive capability and may provide a peak transient current of 50mA. If sixteen B1 buffers switch simultaneously, a peak current of nearly one amp is generated through the V_{SS} bus, bonding wire, package and out to the PC board. There are therefore guidelines on the number of V_{SS} and V_{DD} pins based on three factors:

- the driver capability of the buffer,
- the number of buffers switching simultaneously,
- the location of power and ground relative to the outputs.

Each V_{SS} pad can support a maximum of 16 B1 equivalent buffers (8 on each side of the V_{SS} pad). Each V_{DD} pad can support up to 32 B1 equivalent buffers (16 on each side). The number of V_{SS2} pads required depends on the array size and on the number of output buffers used. Figure 4 shows the minimum number of V_{SS2} pads required by each array size.

Output types can be mixed: high drive when needed, low drive when acceptable to reduce noise and power dissipation. Note that inputs may be ignored when calculating power pins since CMOS inputs sink and source minimal current. Figure 5 shows the current drive capabilities of some of the more common output buffer types compared to the B1 buffer.

Array	Minimum Number of V_{SS2} Pads Required
LL5050	2
LL5080	2
LL5140	2
LL5170	2
LL5220	2
LL5320	4
LL5420	4
LL5600	4

Figure 4. Minimum Allowable V_{SS2} Pads Required by Each Array Size

Buffer Type			B1 Equivalent Drive Capability
B14	BTS14		0.25
B18	BTS18		0.5
B1	BTS1	BTS7	1
B2	BTS2	BTS8	2
B3	BTS3	BTS9	3

Figure 5. Current Drive Capabilities of Output Buffer Types

Figure 6 shows the footprint for the LL5600. Dedicated V_{SS}, V_{SS2}, and V_{DD} power pads are separated into primary and secondary pads.The primary pads are grouped together in sets of 3 at the midpoint of each of the four sides. The secondary pads are located individually near the four corners of the chip. All primary pads must be used first. Primary pads cannot be used as signal pads. If additional power pads are required, then the secondary pads will be used. All secondary pads not used for power may be used as a signal pad. Similar footprints for other array sizes are available from LSI LOGIC.

Power Dissipation

Power dissipation in CMOS circuits is made up of four basic elements.

The first is due to leakage. It constitutes the quiescent power dissipation and is essentially negligible (few microwatts) for CMOS technology.

The second is DC current through ON transistors. This can be from a variety of sources:

- a low on an input with a pullup resistor (all TTL inputs have nominal 880kΩ pullup resistors),
- outputs which sink or source current,
- any unconnected inputs without a pullup or pulldown,
- any internal gates whose inputs are floating (e.g., a data bus with all the lines disabled),
- inputs at worst-case levels, particularly TTL inputs at 2V.

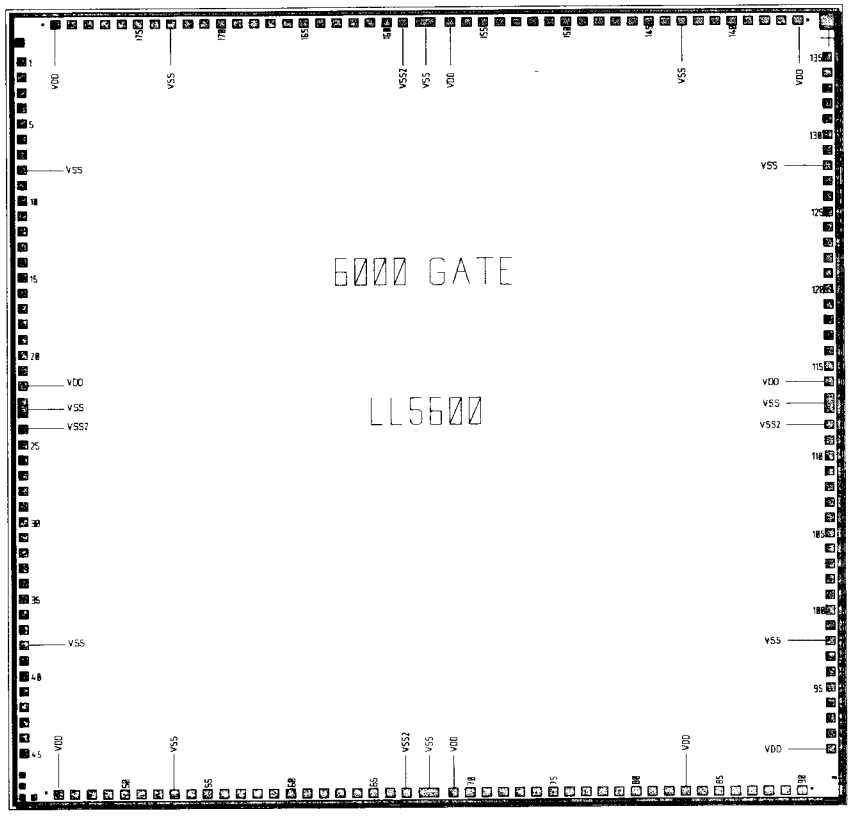


Figure 6. LL5600 Footprint

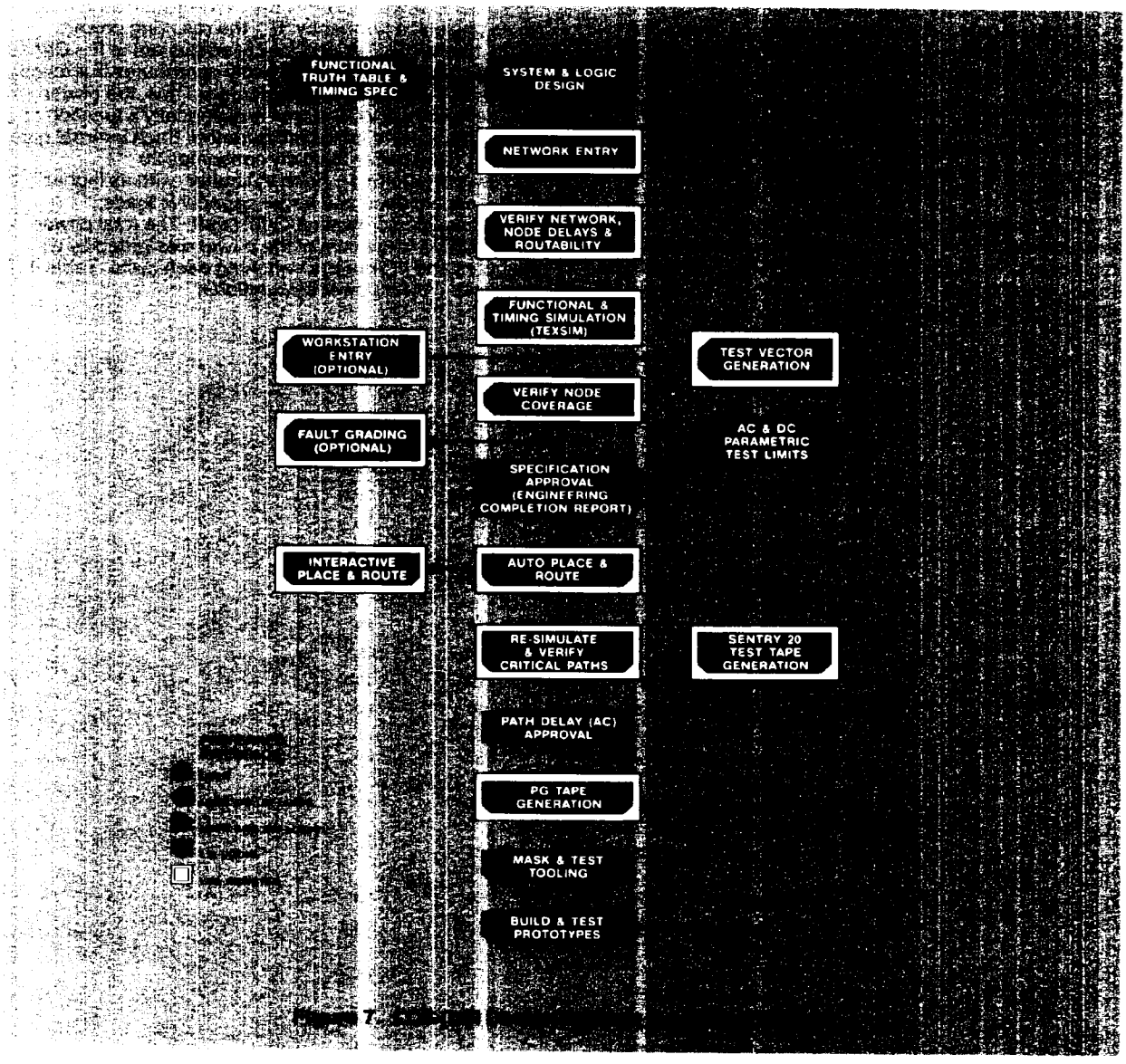
Care should be exercised during logic design to make sure that there is a test condition in which all this DC current may be turned off, so that DC leakage may be easily measured.

The third source of power dissipation is due to overlap currents when the P- and N-transistors are switching from the high-to-low state or vice-versa. This contributes less than 10% of the power dissipated and occurs for the transition period when $V_{TH(N)} < V_{IN} < V_{DD} - V_{TH(P)}$.

The fourth and the most important factor is the charging and discharging of circuit capacitance. The charging of a capacitor C to a voltage V through a P-channel device builds up a charge CV and stores energy CV^2. This energy is later discharged through an N-channel transistor in the CMOS P-N pair. When such switching takes place at a frequency "f", the resulting power dissipated in the CMOS circuit is equivalent to $P = CV^2 f$. This AC power dissipation usually contributes in excess of 90% of the total power dissipated. Thus, the power dissipation in a CMOS circuit is essentially a function of the frequency and logic configuration. Each internal gate in the LL5000 series typically consumes 20 microwatts/gate/MHz. Each I/O buffer, with its higher output capacitance and larger capacitive loads, consumes 25 microwatts/I/O/MHz/pF. The total power consumption is the sum of the power dissipated by all the gates and I/O buffers switching each cycle. Table 4 illustrates typical power calculations.

Parameter	Array Type	
	LL5220	LL5600
Number of available gates	2224	5902
Percentage of gates utilized (%)	85	75
Number of gates utilized	1890	4427
Number of gates switching each cycle (15%)	284	664
Dissipation/gate/MHz (μW)	20	20
Total core dissipation/MHz (mW)	5.7	13.3
Number of available I/O buffers	106	168
Percentage of I/O buffers utilized (%) as outputs	50	50
Number of I/O buffers utilized as outputs	53	84
Number of I/O outputs switching each cycle (20%)	11	17
Dissipation/output buffer/MHz/pF (μW)	25	25
Output capacitive load (pF)	50	50
Dissipation/output buffer/MHz (mW)	1.25	1.25
Total output buffer dissipation/MHz (mW)	13.8	21.3
Total dissipation/MHz (mW)	19.5	34.6
Total dissipation at 10MHz clock speed (mW)	195	346
Total dissipation at 25MHz clock speed (mW)	487	865

Table 4. Power Dissipation Calculation Example



Reliability and Quality Assurance

The reliability department provides LSI LOGIC with a number of programs to define product reliability levels. Among these programs are: (1) qualification, (2) monitor, (3) failure analysis, and (4) data collection and presentation. The reliability monitor program is designed to assure that all products manufactured and shipped to customers comply with corporate reliability policy.

The reliability plan is implemented during the development phase when actual test structures and working devices are implemented in silicon. High stress tests are performed to identify and quantify potential failure mechanisms. High stress reliability testing is continued during limited production on units manufactured using defined processes. See Figure 8 for the qualification process.

Reporting and Publication of Data

Qualification test reports are prepared and distributed by reliability for all products or processes which are approved by formal qualification testing for use in the manufacture of LSI LOGIC products. These reports contain a statement of qualification that certifies the process or product for use in LSI LOGIC.

New packages are approved and released for production by reliability after prescribed environmental tests have been successfully completed. All testing is done according to the applicable methods of MIL-STD-883, Level B and/or C. Testing methods used include, but are not limited to, the following:

Operating Life	Method 1005
Temperature Cycling	Method 1010
Constant Acceleration	Method 2001
Salt Atmosphere	Method 1009
Lead Integrity	Method 2004
Solderability	Method 2003

In addition, the following are performed on plastic devices:

Biased Humidity	85°C/85% Relative Humidity
Pressure Cooker	T_A = 121°C, 15 psig 100% Relative Humidity

See Reliability Data Summary RD01 for more details.

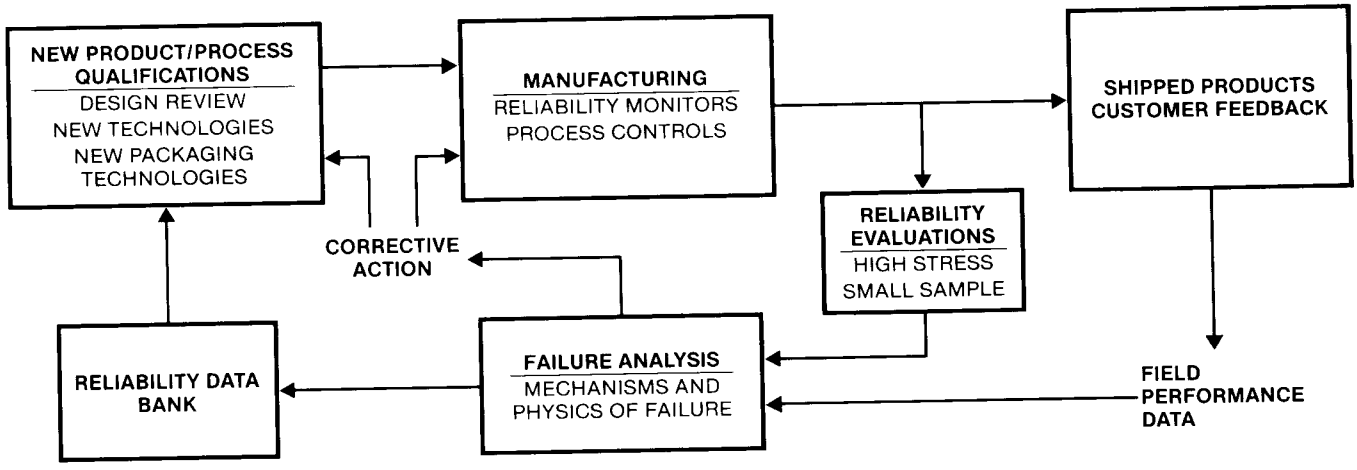


Figure 8. Qualification Process

Operating Characteristics

Absolute Maximum Ratings (Referenced to V_{SS})

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
DC Input Current	I_I	±10	mA
Storage Temperature Range (Ceramic)	T_{STG}	−65 to +150	°C
Storage Temperature Range (Plastic)	T_{STG}	−40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	+3 to +6	V
Operating Ambient Temperature Range Military	T_A	−55 to +125	°C
Industrial Range	T_A	−40 to +85	°C
Commercial Range	T_A	0 to +70	°C

DC Characteristics

Specified at V_{DD} = 5V ± 5% ambient temperature over the specified temperature range(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage					
	TTL Inputs				0.8	V
	CMOS Levels				1.5	V
V_{IH}	High Level Input Voltage					
	TTL Inputs, Commercial Temperature Range		2.0	1.7		V
	TTL Inputs, Military and Industrial Temperature Range		2.25	1.7		V
	CMOS Levels		3.5	3.0		V
V_{T+}	Schmitt-Trigger, Positive-going Threshold			3.0	4.0	V
V_{T-}	Schmitt-Trigger, Negative-going Threshold		1.0	1.5		V
π	Hysteresis, Schmitt Trigger	V_{IL} to V_{IH} V_{IH} to V_{IL}	1.0	1.5		V
I_{IN}	Input Current, CMOS, TTL Inputs	$V_{IN} = V_{DD}$	−10	±1	10	μA
	Inputs with Pulldown Resistors	$V_{IN} = V_{DD}$		5	20	μA
	CMOS Inputs	$V_{IN} = V_{SS}$	−10	±1	10	μA
	TTL Inputs & Inputs with Pullup Resistors	$V_{IN} = V_{SS}$	−20	−5		μA
V_{OH}	High Level Output Voltage	Comm / Mil				
	Type B14	I_{OH} = −1mA / −0.8mA	2.4	4.5		V
	Type B18	I_{OH} = −2mA / −1.6mA				
	Type B1	I_{OH} = −4mA / −3.2mA				
	Type B2 (2)	I_{OH} = −8mA / −6.4mA				
	Type B3 (3)	I_{OH} = −12mA / −9.6mA				
V_{OL}	Low Level Output Voltage	Comm / Mil				
	Type B14	I_{OL} = 1mA / 0.8mA		0.2	0.4	V
	Type B18	I_{OL} = 2mA / 1.6mA				
	Type B1	I_{OL} = 4mA / 3.2mA				
	Type B2 (2)	I_{OL} = 8mA / 6.4mA				
	Type B3 (3)	I_{OL} = 12mA / 9.6mA				
I_{OZ}	Three-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	−10	±1	10	μA
I_{OS}	Output Short Circuit Current (4)	V_{DD} = Max $V_O = V_{DD}$ V_{DD} = Max, V_O = 0V	25 −7		90 −28	mA mA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	User-Design Dependent			
C_{IN}	Input Capacitance	Any Input (5)	2			pF
C_{OUT}	Output Capacitance	Any Output (6)	4			pF

Notes:

1. Military temperature range is −55°C to +125°C, ±10% power supply (ceramic packages only); industrial temperature range is −40°C to +85°C, ±5% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Requires two output pads.
3. Requires three output pads.
4. Type B1 output. Output short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
5. Not applicable to assigned bidirectional buffer (excluding package).
6. Output using single buffer structure (excluding package).

AC Characteristics

$V_{DD} = 5V$, $T_A = 25°C$

Note: Delays through interconnect are included. Interconnect wirelengths are assumed from statistical distributions for given fanouts.

Macrocell	Input Transition	Propagation Delays: Output Load Capacitance 15pF	50pF	85pF	100pF	Equivalent Gate Count
UNIDIRECTIONAL BUFFERS						
3-state Output Buffer with 1mA Drive (BTS14)	t_{PHL} t_{PLH}	10.9 8.3	25.6 16.4	40.4 24.6	46.8 28.1	5
3-state Output Buffer with 12mA Drive (BTS3)	t_{PHL} t_{PLH}	6.6 6.1	7.9 7.2	9.1 8.3	9.7 8.7	11
THREE-STATE BIDIRECTIONAL BUFFERS						
3-state I/O Buffers with 4mA Drive (BTS7)	t_{PHL} t_{PLH}	5.3 5.7	8.7 9.0	12.1 12.2	13.6 13.6	7
3-state I/O Buffers with Pullup (BTS7U)/ Pulldown (BTS7D)	t_{PHL} t_{PLH}	5.3 5.7	8.7 9.0	12.1 12.2	13.6 13.6	7
OUTPUT BUFFERS						
Output Buffer with 1mA Drive (B14)	t_{PHL} t_{PLH}	9.0 5.9	23.7 13.9	38.5 22.1	44.8 25.6	1
Output Buffer with 12mA Drive (B3)	t_{PHL} t_{PLH}	5.9 5.9	7.2 7.0	8.5 8.1	9.0 8.6	2

		Fanout 1	2	3	4	8	Equivalent Gate Count
INPUT RECEIVERS							
Input Buffers with CMOS Inputs (IBUF)	t_{PHL} t_{PLH}	2.6 2.4	2.7 2.5	2.7 2.6	2.8 2.7	3.1 3.1	0
Input Buffer with Schmitt Trigger (SCHMIT1)	t_{PHL} t_{PLH}	7.2 4.4	7.4 4.8	7.5 5.1	7.7 5.5	8.2 6.8	3
Input Buffer with TTL Inputs (TLCHT)	t_{PHL} t_{PLH}	4.4 1.7	4.5 1.9	4.6 2.1	4.7 2.3	5.0 3.2	0
INTERNAL BUFFERS							
Single Inverter (IV)	t_{PHL} t_{PLH}	0.8 2.0	1.1 2.7	1.3 3.4	1.6 4.0	2.6 6.7	1
Power Inverter (IVP)	t_{PHL} t_{PLH}	0.7 1.4	0.8 1.7	0.9 2.1	1.1 2.4	1.6 3.8	1
LOGIC GATES							
2-input Exclusive OR (EO)	t_{PHL} t_{PLH}	4.2 3.5	4.4 3.8	4.5 4.1	4.7 4.5	5.3 5.9	3
2-input NAND (ND2)	t_{PHL} t_{PLH}	1.2 2.4	1.6 3.1	2.0 3.7	2.4 4.4	4.1 7.1	1
3-input NAND (ND3)	t_{PHL} t_{PLH}	2.0 3.1	2.6 3.7	3.2 4.4	3.8 5.1	6.1 7.8	2
4-input NAND (ND4)	t_{PHL} t_{PLH}	2.7 3.3	3.5 4.0	4.3 4.7	5.1 5.4	8.2 8.1	2
8-input NAND (ND8)	t_{PHL} t_{PLH}	6.3 4.8	6.5 5.1	6.7 5.4	6.8 5.8	7.4 7.2	6
2-input NOR (NR2)	t_{PHL} t_{PLH}	1.0 3.5	1.2 4.8	1.5 6.2	1.7 7.5	2.7 12.8	1
3-input NOR (NR3)	t_{PHL} t_{PLH}	1.0 6.0	1.3 8.0	1.5 10.0	1.8 12.0	2.7 20.0	2
4-input NOR (NR4)	t_{PHL} t_{PLH}	1.0 8.4	1.3 11.0	1.5 13.7	1.8 16.3	2.8 27.0	2
8-input NOR (NR8)	t_{PHL} t_{PLH}	3.4 9.3	3.5 9.6	3.7 10.0	3.8 10.3	4.4 11.7	6

AC Characteristics (Continued)

V_{DD} = 5V, T_A = 25°C

Macrocell	Input Transition	Fanout 1	2	3	4	8	Equivalent Gate Count
FLIP-FLOPS							
D Flip-flop (FD1)	t_{PHL}	4.4	4.8	5.3	5.7	7.5	5
	t_{PLH}	5.8	6.5	7.2	7.9	10.6	
	t_S	1.5	1.5	1.5	1.5	1.5	
	t_H	1.0	1.0	1.0	1.0	1.0	
D Flip-flop with Scan Test Inputs (FD1S)	t_{PHL}	6.2	6.6	7.1	7.5	9.1	8
	t_{PLH}	5.8	6.5	7.2	7.9	10.6	
	t_S	5.0	5.0	5.0	5.0	5.0	
	t_H	1.0	1.0	1.0	1.0	1.0	
D Flip-flop with Set Direct, Clear Direct (FD3)	t_{PHL}	4.4	4.8	5.3	5.7	7.5	7
	t_{PLH}	5.8	6.5	7.2	7.9	10.6	
	t_S	1.5	1.5	1.5	1.5	1.5	
	t_H	1.0	1.0	1.0	1.0	1.0	
D Flip-flop with Set Direct, Clear Direct, and Scan Test Inputs (FD3S)	t_{PHL}	6.2	6.6	7.1	7.5	9.1	10
	t_{PLH}	5.8	6.5	7.2	7.9	10.6	
	t_S	4.0	4.0	4.0	4.0	4.0	
	t_H	1.5	1.5	1.5	1.5	1.5	
J-K Flip-flop (FJK1)	t_{PHL}	5.2	5.6	6.1	6.5	8.3	8
	t_{PLH}	6.7	7.4	8.1	8.8	11.5	
	t_S	3.5	3.5	3.5	3.5	3.5	
	t_H	0	0	0	0	0	
J-K Flip-flop with Scan Test Inputs (FJK1S)	t_{PHL}	6.5	6.9	7.3	7.7	9.3	10
	t_{PLH}	6.6	7.3	7.9	8.6	11.3	
	t_S	6.0	6.0	6.0	6.0	6.0	
	t_H	0	0	0	0	0	
LATCHES							
Gated D Latch (LD1)	t_{PHL}	4.2	4.5	4.7	4.9	5.9	3
	t_{PLH}	4.7	5.4	6.1	6.8	9.5	
	t_S	0	0	0	0	0	
	t_H	4.0	4.0	4.0	4.0	4.0	
S-R Latch with Separate Input Gates, Set Direct and Reset Direct (LSR1)	t_{PHL}	5.7	6.3	6.9	7.5	10.0	4
	t_{PLH}	6.7	8.0	9.3	10.6	15.8	
D Latch with Scan Test Inputs (LS1)	t_{PHL}	8.9	9.2	9.5	9.7	10.8	6
	t_{PLH}	5.5	6.2	6.9	7.6	10.4	
	t_S	3.5	3.5	3.5	3.5	3.5	
	t_H	2.0	2.0	2.0	2.0	2.0	
MISCELLANEOUS							
2-to-1 Multiplexer (MUX21LA)	t_{PHL}	2.3	2.4	2.6	2.7	3.2	2
	t_{PLH}	2.3	2.6	3.0	3.3	4.7	

AC Characteristics (Continued)

$V_{DD} = 5V$, $T_A = 25°C$

Macrofunctions		Performance	Gate Count
16-Bit Barrel Shifter		16ns	116
32-Bit Barrel Shifter		20ns	281
8-Bit Barrel Shifter		14ns	55
16-Bit Adder		35ns	248
16-Bit 74181 Type ALU	Any Input to F	48ns	363
16-Bit 100181 Type ALU	Any Input to F	65ns	558
8 x 8 Multiplier		65ns	517
12 x 12 Multiplier		78ns	1102
16 x 16 Multiplier		83ns	1796
2901 4-Bit ALU Slice	Minimum Clock Period	55ns	720
2902 μProgram Sequencer		40ns	258
2910 μProgram Controller	Minimum Clock Period	60ns	856
8-Bit Magnitude Comparator		25ns	87
8-Bit Priority Encoder		18ns	37
16 x 4 FIFO (Fall-thru type)		—	324

Note 1: Delay for worst-case path with typical interconnection length under normal conditions ($V_{DD} = 5V$, $T_A = 25°C$).