National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM108A-X REV 1A1

Original Creation Date: 06/26/95
Last Update Date: 02/11/99
Last Major Revision Date: 07/21/98

OPERATIONAL AMPLIFIERS

General Description

The LM108A is a precision operational amplifier having specifications a factor of ten better than FET amplifiers over a -55 C to +125 C temperature range.

The device operates with supply voltages from ±2V to ±20V and has sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with, and uses the same compensation as, the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise, and to make supply bypass capacitors unnecessary.

The low current error of the LM108A makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 Mohms source resistances, introducing less error than devices such as the 709 with 10 Kohms sources. Integrators with drifts less than 500 uV/sec, and analog time delays in excess of one hour, can be made using capacitors no larger than 1uF.

Industry Part Number

LM108A

Prime Die

LM108

NS Part Numbers

LM108AH/883
LM108AJ-8/883
LM108AJ/883
LM108AW/883
LM108AWG/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Maximum input bias current of 3.0 nA over temperature.
- Offset current less than 400 pA over temperature.
- Supply current of only 300 uA, even in saturation.
- Guraranteed drift characteristics.

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage		±20V
Input Voltage (Note 4)		±15V
Power Dissipation (Note 2)		500mW
Maximum Junction Temperature		150 C
Differential Input Current (Note 3)		±10mA
Output Short-Circuit Duration		Continuous
Operating Temperature Range		-55 C to +125 C
Storage Temperature Range		-65 C to +150 C
Thermal Resistance		
ThetaJA		
METAL CAN	(Still Air)	159 C/W
	(500LF/Min Air flow)	86 C/W
CERDIP, 14 Lead	(Still Air)	94 C/W
	(500LF/Min Air flow)	55 C/W
CERDIP, 8 Lead	(Still Air)	123 C/W
	(500LF/Min Air flow)	68 C/W
CERPACK, 10 Lead	(Still Air)	225 C/W
	(500LF/Min Air flow)	142 C/W
CERAMIC SOIC	(Still Air)	225 C/W
	(500LF/Min Air flow)	142 C/W
ThetaJC		
METAL CAN		38 C/W
CERDIP, 14 Lead		13 C/W
CERDIP, 8 Lead		17 C/W
CERPACK, 10 Lead		21 C/W
CERAMIC SOIC		21 C/W
Package Weight (Typical)		
METAL CAN		990mg
CERDIP, 14 Lead		2180mg
CERDIP, 8 Lead		1090mg
CERPACK, 10 Lead		225mg
CERAMIC SOIC		210mg
Lead Temperature (Soldering, 10 seconds)		260 C
H-Pkg (Soldering, 10 seconds)		300 C
ESD Tolerance (Note 5)		2000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 4: For supply voltages less than $\pm$15V, the absolute maximum input voltage is equal to the supply voltage.

Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±20V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vcm = -15V			-0.5	0.5	mV	1
					-1.0	1.0	mV	2, 3
		Vcm = 15V			-0.5	0.5	mV	1
					-1.0	1.0	mV	2, 3
					-0.5	0.5	mV	1
					-1.0	1.0	mV	2, 3
		Vcc = ±5V			-0.5	0.5	mV	1
		Vcc = ±5V			-1.0	1.0	mV	2, 3
Iio	Input Offset Current	Vcm = -15V			-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
		Vcm = 15V			-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
					-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
		Vcc = ±5V			-0.2	0.2	nA	1
		Vcc = ±5V			-0.4	0.4	nA	2, 3
Iib+	Input Bias Current	Vcm = -15V			-0.1	2	nA	1
					-1.0	3.0	nA	2
					-0.1	3.0	nA	3
		Vcm = 15V			-0.1	2	nA	1
					-1.0	3.0	nA	2
					-0.1	3.0	nA	3
					-0.1	2	nA	1
					-1.0	3.0	nA	2
					-0.1	3.0	nA	3
		Vcc = ±5V			-0.1	2	nA	1
		Vcc = ±5V			-1.0	3.0	nA	2
		Vcc = ±5V			-0.1	3.0	nA	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±20V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib-	Input Bias Current	Vcm = -15V			-0.1	2	nA	1
					-1.0	3.0	nA	2
					-0.1	3.0	nA	3
		Vcm = 15V			-0.1	2	nA	1
					-1.0	3.0	nA	2
					-0.1	3.0	nA	3
					-0.1	2	nA	1
					-1.0	3.0	nA	2
					-0.1	3.0	nA	3
		Vcc = ±5V			-0.1	2	nA	1
		Vcc = ±5V			-1.0	3.0	nA	2
		Vcc = ±5V			-0.1	3.0	nA	3
PSRR	Power Supply Rejection Ratio	±20V <= Vcc <= ±5V			96		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	-15V <= VCM <= 15V			96		dB	1, 2, 3
Ios+	Short Circuit	Vcc = ±15V			-30	-1.0	mA	1, 2, 3
Ios-	Short Circuit	Vcc = ±15V			1	30	mA	1, 2, 3
Icc	Power Supply Current					0.6	mA	1
						0.4	mA	2
						0.8	mA	3
Rin	Input Resistance		2		30		M	1
Vin	Input Voltage Range	Vcc = ±15V	1		±14		V	1, 2
		Vcc = ±15V	1		±13.5		V	3
			1		±15		V	1, 2, 3
Delta Vio/Delta T	Temperature Coeffient of Input Offset Voltage		2			5	uV/C	1, 2, 3
Delta Iio/Delta T	Temperature Coeffient of Input Offset Current		2			2.5	pA/C	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±20V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vop+	Output Voltage Swing	Vcc=±15V, Rl=10K Ohms			13		V	4, 5, 6
Vop-	Output Voltage Swing	Vcc=±15V, Rl=10K Ohms				-13	V	4, 5, 6
Avs+	Open Loop Voltage Gain	Vcc=±15V, Rl=10K Ohms, Vout= 0 to 10V	3		80		V/mV	4
		Vcc=±15V, Rl=10K Ohms, Vout= 0 to 10V	3		40		V/mV	5, 6
Avs-	Open Loop Voltage Gain	Vcc=±15V, Rl=10K Ohms, Vout= 0 to -10V	3		80		V/mV	4
		Vcc=±15V, Rl=10K Ohms, Vout= 0 to -10V	3		40		V/mV	5, 6
TR	Transient Response Rise Time		2		1		uS	7

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±20V, Vcm = 0V. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Vio	Input Offset Voltage	Vcm = 15V			-0.25	0.25	mV	1
Iib+	Input Bias Current	Vcm = 15V			-1	1	nA	1
Iib-	Input Bias Current	Vcm = 15V			-1	1	nA	1

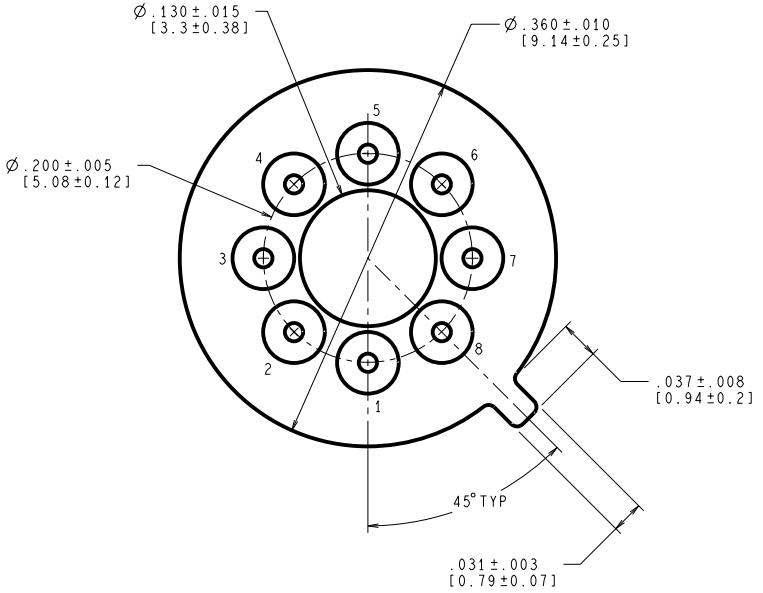
Note 1: Parameter tested go-no-go only.
Note 2: Guaranteed parameter not tested.
Note 3: Datalog in K = V/mV.

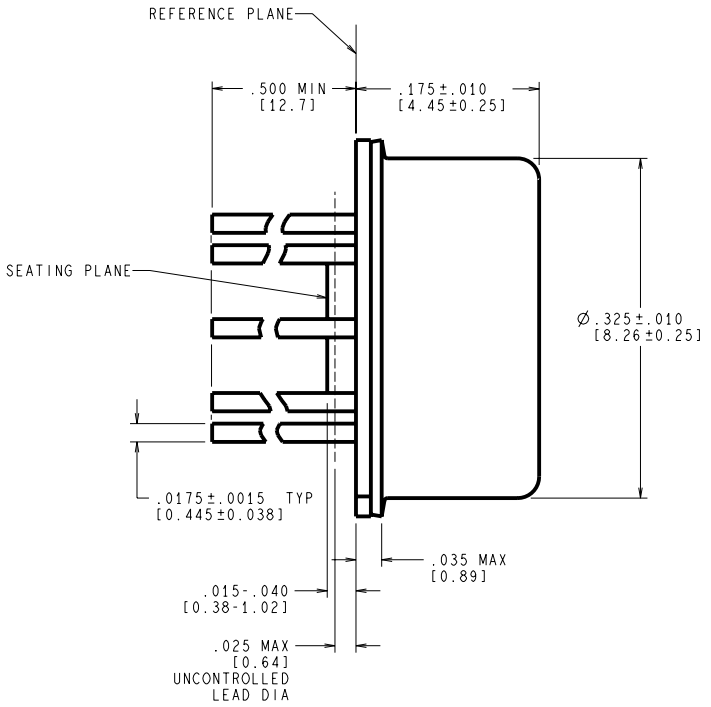
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06135HRA2	CERPACK (W), 10 LEAD (B/I CKT)
09556HR02	CERDIP (J), 14 LEAD (B/I CKT)
09557HRA4	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000253A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
P000310A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PINOUT)
P000311A	CERDIP (J), 14 LEAD (PINOUT)
P000312A	CERDIP (J), 8 LEAD (PINOUT)
P000431A	CERPACK (W), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

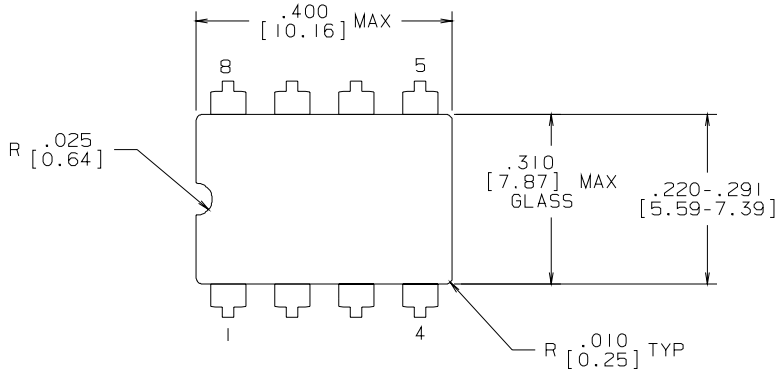
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

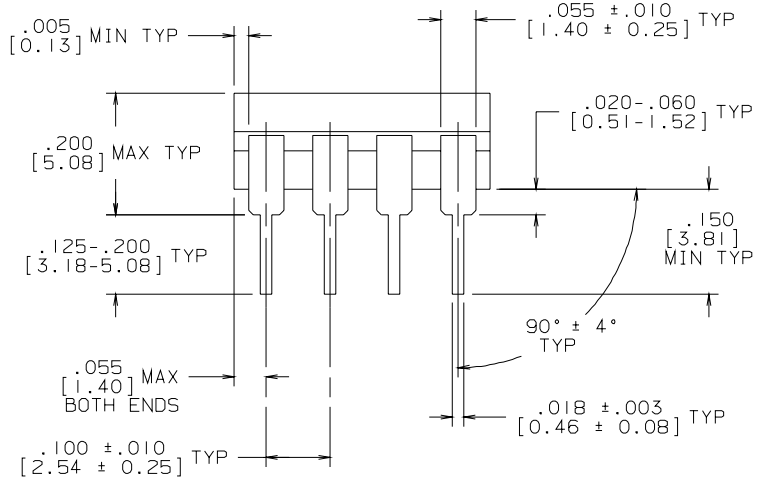
PROJECTION — INCH [MM]

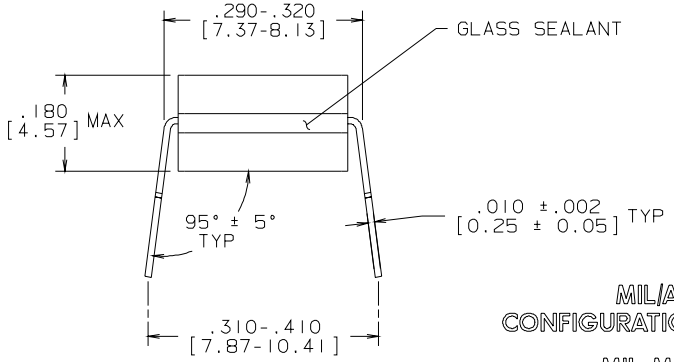
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
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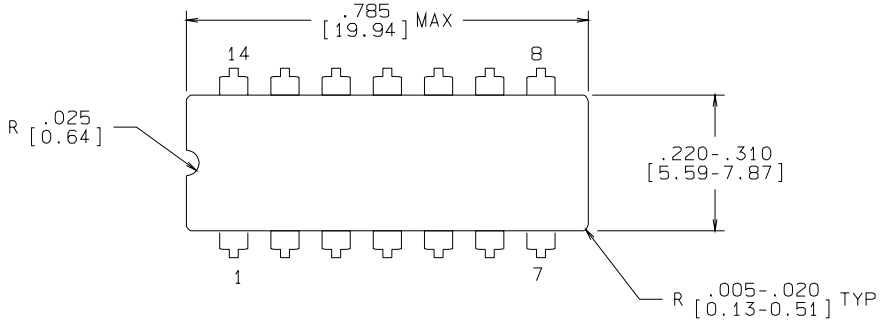
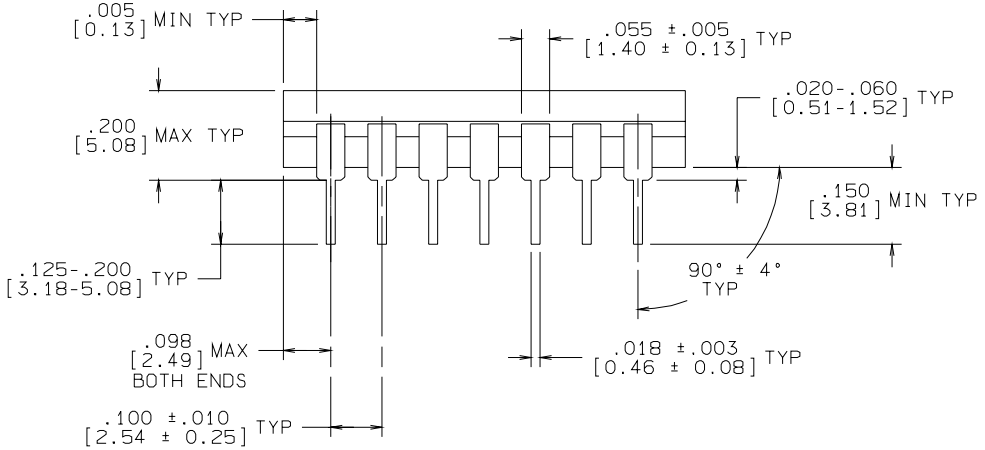
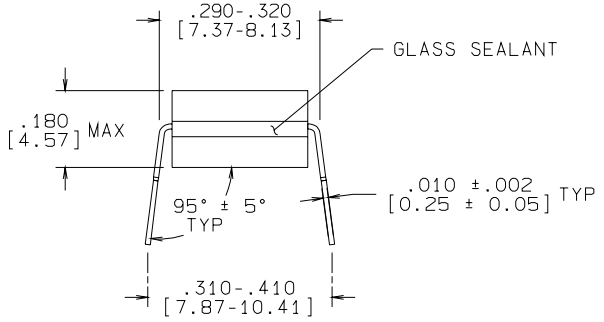






CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

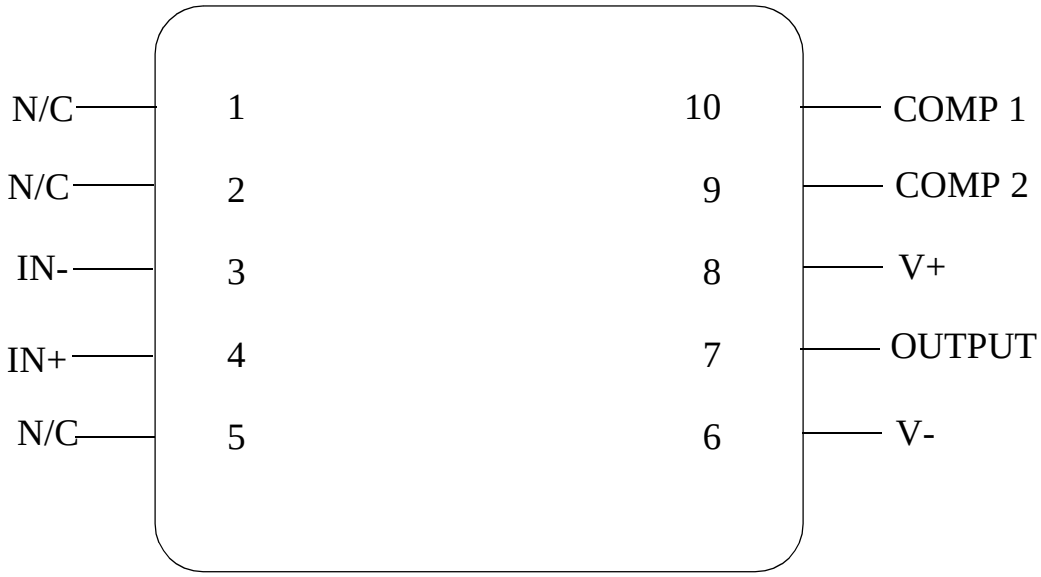
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM108AWG

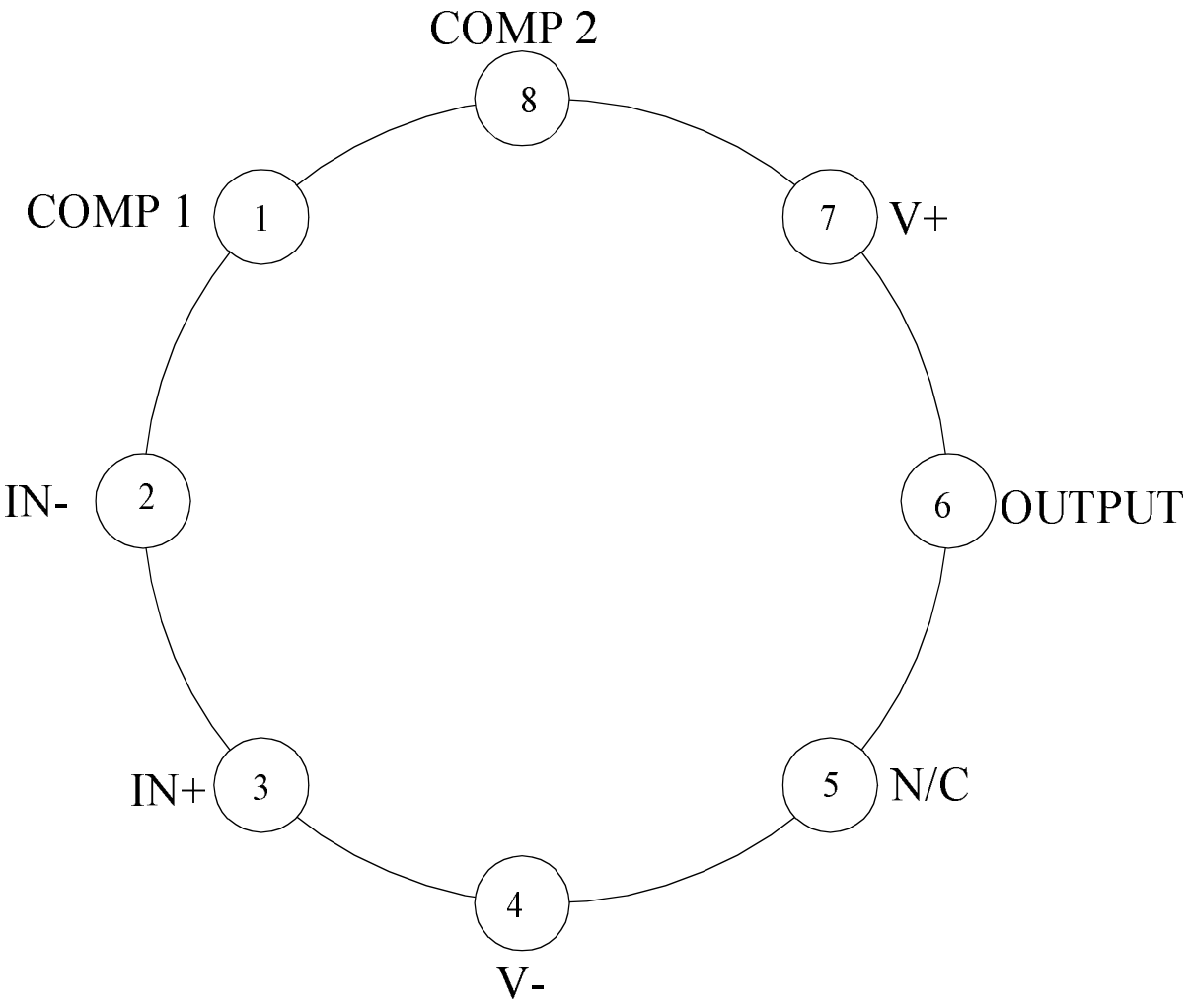
10 - LEAD CERAMIC SOIC

CONNECTION DIAGRAM

TOP VIEW

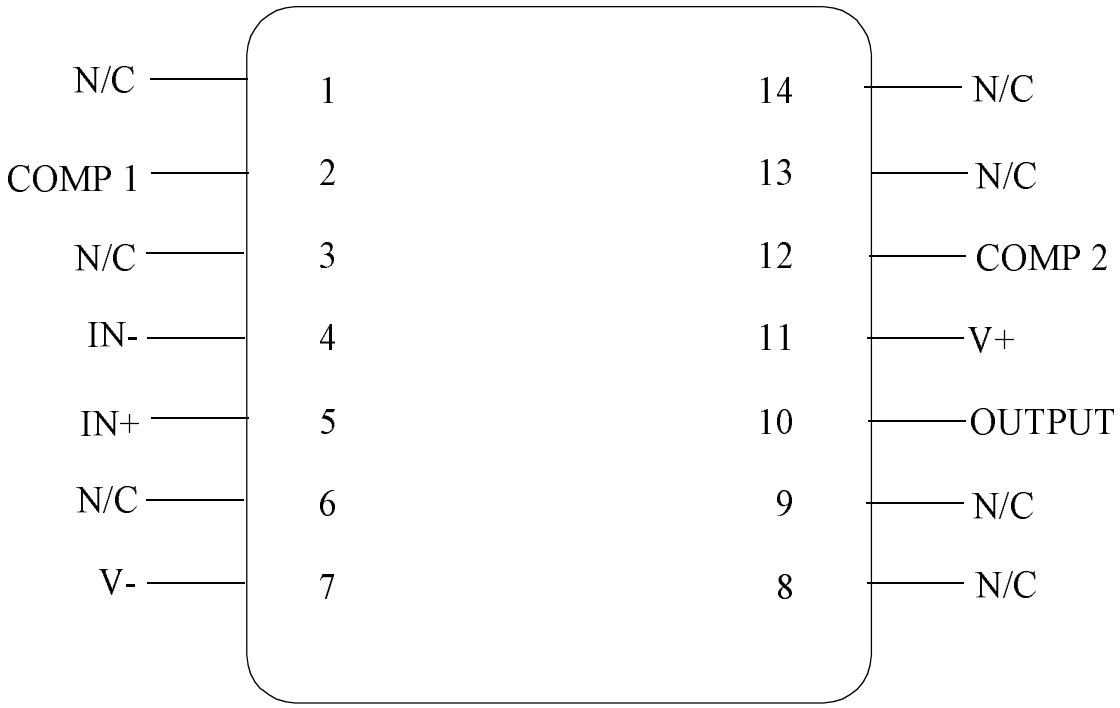
P000253A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



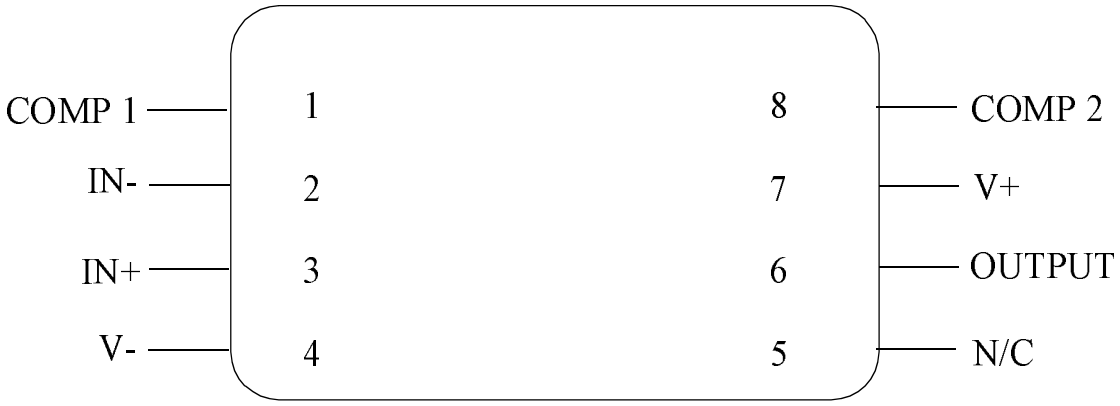
LM108AH, LM108H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000310A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM108AJ, LM108J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000311A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM108AJ-8, LM108J-8

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000312A

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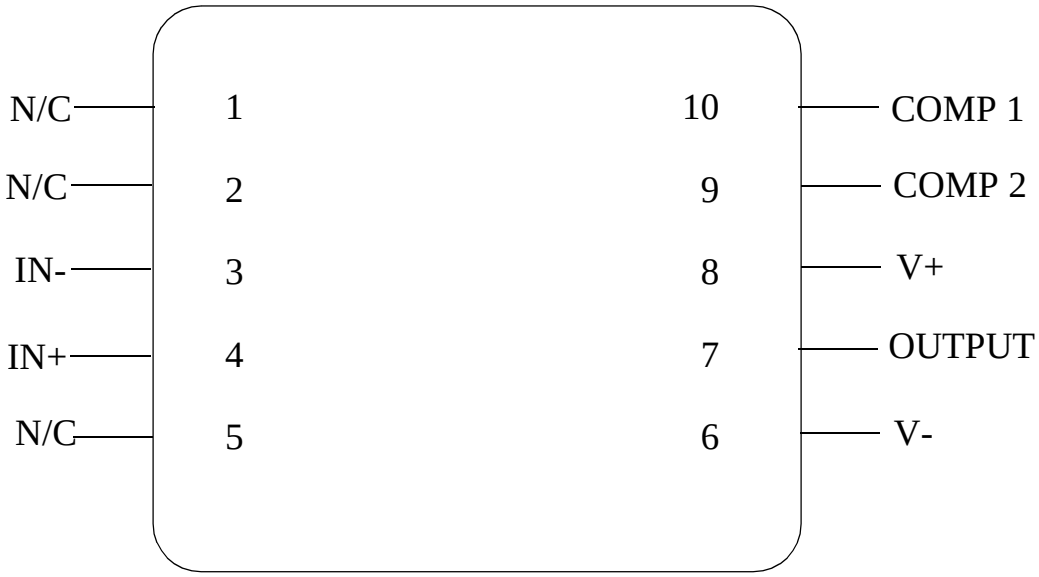
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM108AW

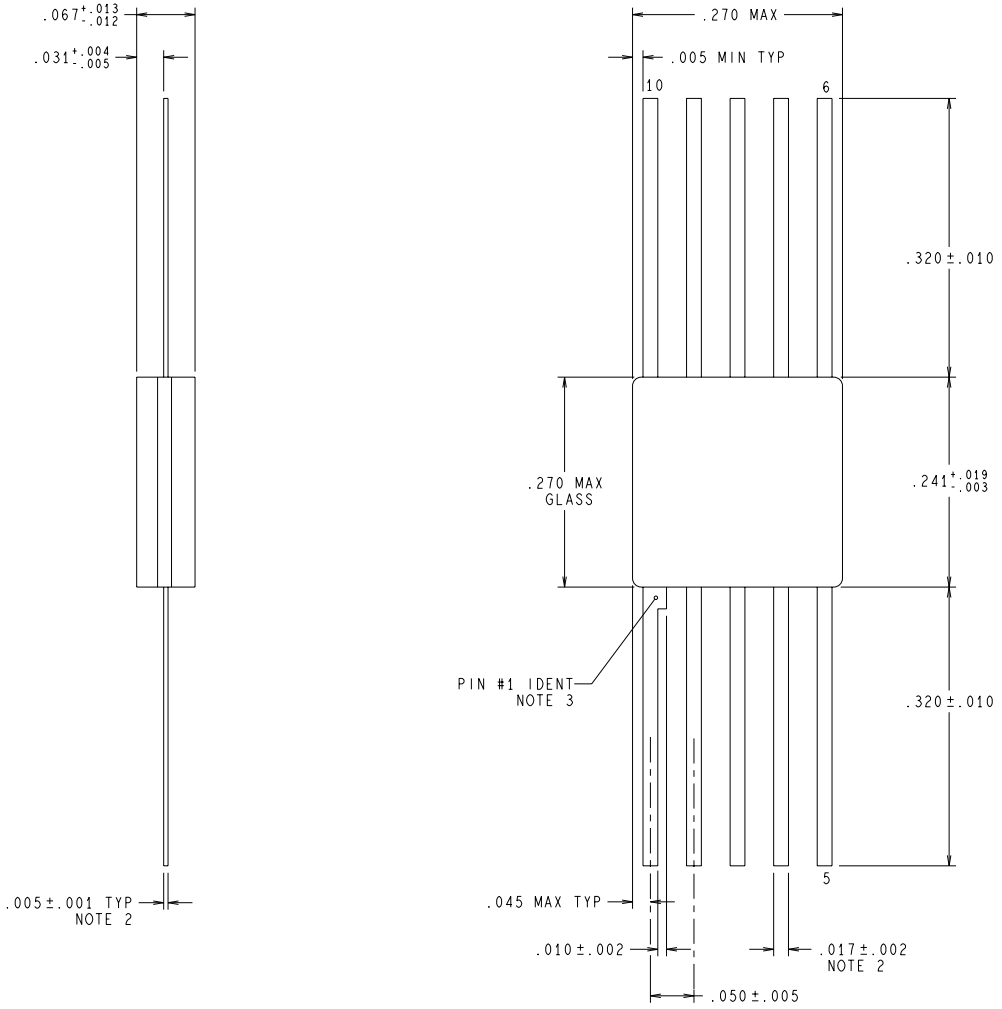
10 - LEAD CERPACK

CONNECTION DIAGRAM
TOP VIEW

P000431A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

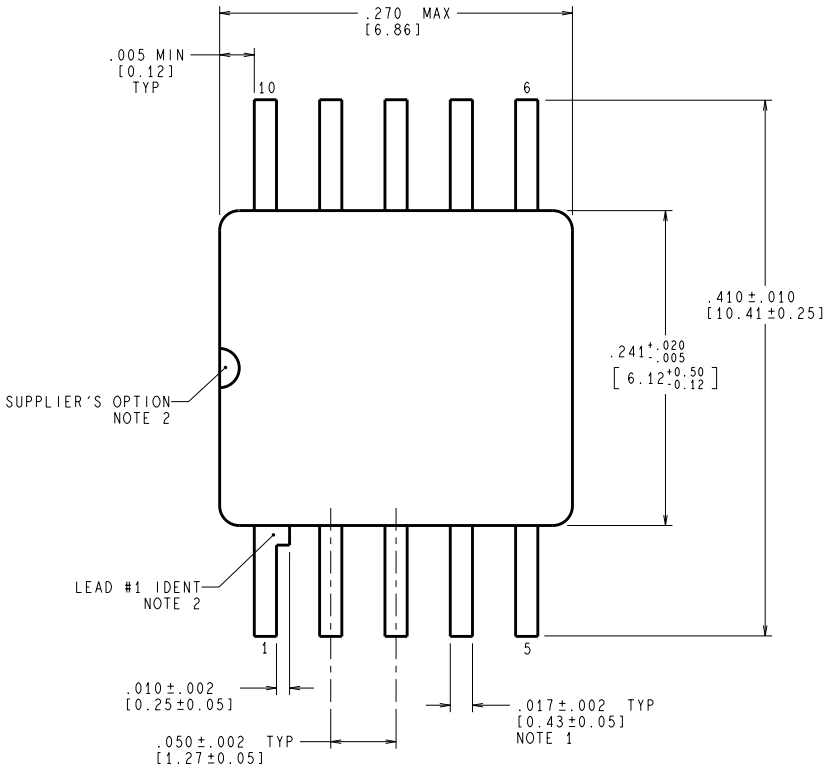
CERPACK, 10 LEAD

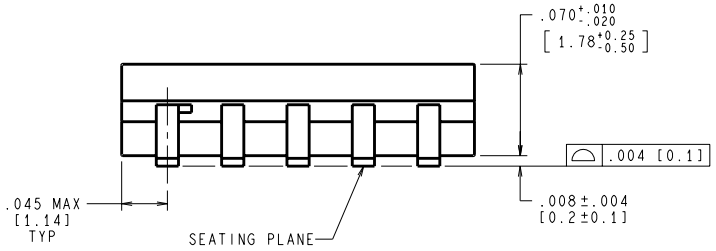
PROJECTION — INCH [MM]

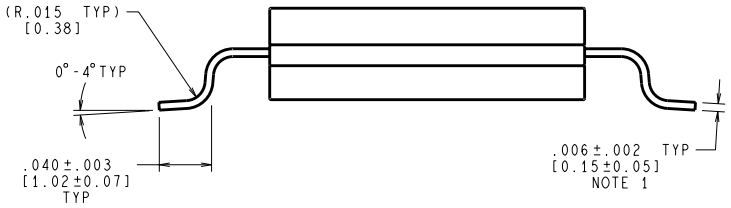
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0CL	M0001741	02/11/99	Barbara Lopez	Changed: MNLM108A-X Rev. 0BL to MNLM108A-X Rev. 0CL. On IIB± subgroup 3 was (-1.0min, 3.0max), corrected to read (-0.1min, 3.0max).
1A1	M0003235	02/11/99	Rose Malone	Updated MDS: MNLM108A-X, Rev. 0CL to MNLM108A-X, Rev. 1A1, Full Release. Added Pinout and B/I Ckt graphics and Thermal Data.