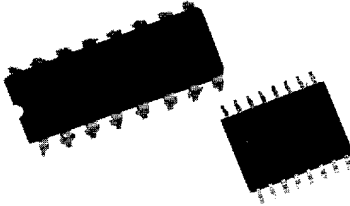


## ARINC 429 LINE DRIVER



### DESCRIPTION

The DD-03182 device is a Line Driver chip that transmits data on the serial data bus in accordance with the "ARINC Specification 429 Mark 33 Digital Information Transfer System" (ARINC 429). This device can be used with DDC's DD-03232 or DD-03296 discrete-to-digital device, used in conjunction with the DD-03282 transceiver chip or DD-42900 429 chip.

The Line Driver receives TTL information on the Data<sub>A</sub>/Data<sub>B</sub> input pins and transmits it out on the A<sub>OUT</sub>/B<sub>OUT</sub> output pins. The output voltage level is programmable via the V<sub>REF</sub> input pin. The output pins are also protected

against short circuits from aircraft power. The slew rate of the DD-03182 can be programmed for either HIGH (100 kbit) or LOW (12.5 kbit) speed via two external timing capacitors connected to C<sub>A</sub>/C<sub>B</sub> input pins.

### APPLICATIONS

The DD-03182 can be used for many different applications from flight critical to nonessential. Surface mount, DIP and PLCC configurations are available. Military temperature range is also available if required.

### FEATURES

- **Harris/Holt/Raytheon Drop-in Compatible**
- **Programmable Output Voltage Level**
- **Short-Circuit Protection on Outputs**
- **Programmable Slew and Data Rates**
- **Plastic SOIC Package Available**

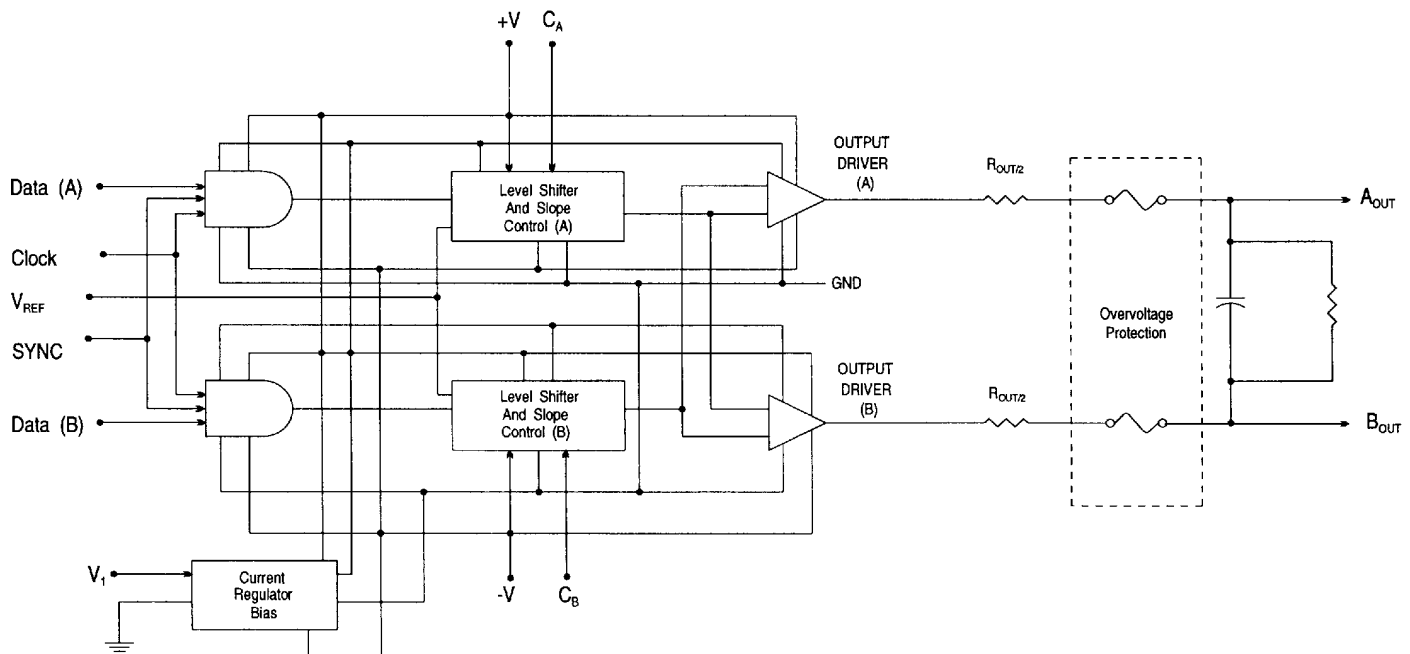


FIGURE 1. DD-03182 BLOCK DIAGRAM

TABLE 1. DD-03182 SPECIFICATIONS				
PARAMETER	UNITS	MIN	TYP	MAX
<b>ABSOLUTE MAXIMUM RATINGS</b>				
<b>VOLTAGE BETWEEN PINS</b>				
■ +V & -V	V			40
■ V <sub>1</sub> & GND	V			7
■ V <sub>REF</sub> & GND	V			6
■ Output Short-circuit Protection		See Note 1		
■ Output Overvoltage Protection		See Note 2		
■ Power Dissipation		See TABLE 2		
<b>POWER SUPPLY REQUIREMENTS</b>				
■ +V	VDC	10.8	15	16.5
■ -V	VDC	-10.8	-15	-16.5
■ V <sub>1</sub>	VDC	4.75	5	5.25
■ V <sub>REF</sub> (for ARINC 429)	VDC	4.75	5	5.25
■ V <sub>REF</sub> (for other applications)	VDC	0		
<b>THERMAL</b>				
Operating Temperature	°C	-55		+125
Storage Temperature	°C	-65		+150
Lead Temperature (localized, 10 sec duration)	°C			+300
Thermal Resistance:				
Junction to Case $\theta_{jc}$	°C/W			35
Junction to Ambient $\theta_{ja}$	°C/W			75
<b>SIZE</b>				
DD-03182DC	in. (mm.)	0.785 x 0.291 x 0.160 (19.93 x 7.39 x 4.06)		
DD-03182GP		0.413 x 0.300 x 0.082 (10.49 x 7.62 x 2.08)		
DD-03182PP		0.454 x 0.454 x 0.155 (11.53 x 11.53 x 3.94)		

Notes:

1. Both outputs can be shorted to ground or to each other indefinitely.
2. Both outputs are fused between 0.5 Amp DC and 1.0 Amp DC to prevent an overvoltage fault from coupling onto the system power bus.

TABLE 2. DD-03182 POWER DISSIPATION						
DATA RATE (kbits)	LOAD	+V @ 15 V (mA)	-V @ 15 V (mA)	V <sub>1</sub> + V <sub>REF</sub> @ 5 V (mA)	429 POWER (mW)	LOAD POWER (mW)
0 TO 100	NONE	2.0	-5.0	4	125	0.0
12.5	HALF	4.0	-7.0	4	185	30
100	HALF	12.7	-15.7	4	447	162.5
12.5	FULL	6.0	-8.3	4	244	60
100	FULL	23.4	-26.5	4	769*	325

\* May require heat sink @ T<sub>A</sub> = 125° C

## GENERAL

The ARINC 429 standard is widely used in the civil aerospace market (commercial aircraft). ARINC 429A operates at either 12 to 14.5 or 100 kbits on a simplex bus. A simplex bus is one on which there is only one transmitter but multiple receivers (up to a maximum of 20 in the case of 429). If receipt of a message by a given sink R(n) is required by the source T, a separate bus with R(n) as the source and T as the sink is required. To those designers who focus on military systems a simplex bus may seem cumbersome, but it can be readily certified for civil aircraft.

Communications on 429 buses use 32-bit words with odd parity. The waveform is bipolar return-to-zero with each bit lasting either 70 or 83  $\mu$ s  $\pm$  2.5 percent or 10  $\mu$ s  $\pm$  2.5 percent depending on whether the bus low or high speed. A low-speed bus is used for general purpose, low criticality applications, and a high-speed bus is used for transmitting large quantities of data or flight-critical information.

ARINC 429 imposes relatively modest and readily achievable performance demands on the hardware. FIGURE 2 is a general schematic of a 429 bus. The transmitter output impedance should be in the range of 75 to 85  $\Omega$ , equally divided between the two leads. The output voltage V<sub>o</sub> is 10 1.0 V generated by imposing equal but opposite polarity voltages on the two leads. The null voltage is 0 0.5 V. For the receiver, the input resistance shall be greater than 12,000  $\Omega$  and the input differential capacitance and the capacitance to ground shall, in both cases, be less than 50 pF. The 12,000  $\Omega$  minimum input resistance ensures that up to 20 receivers can be on the bus without overloading it and minimizes receiver interaction under fault conditions. In order to preclude continued receiver operation in a lead-to-ground fault condition, 429 has established the range of acceptable receiver voltage levels to be +6.5 to +13.0 V and -6.5 to -13.0 V and null levels from +2.5 to -2.5 V. Any signals falling outside of these levels will be ignored. Also note that a lead-to-ground fault will produce a differential voltage swing up 5.5 V. FIGURE 4 shows the waveforms required by 429 and permissible levels for transmitter and receiver voltages.

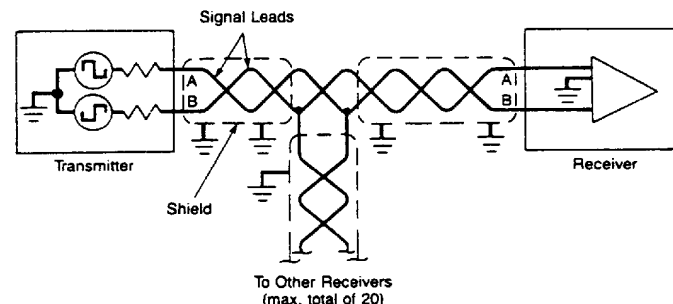


FIGURE 2. GENERALIZED 429 BUS

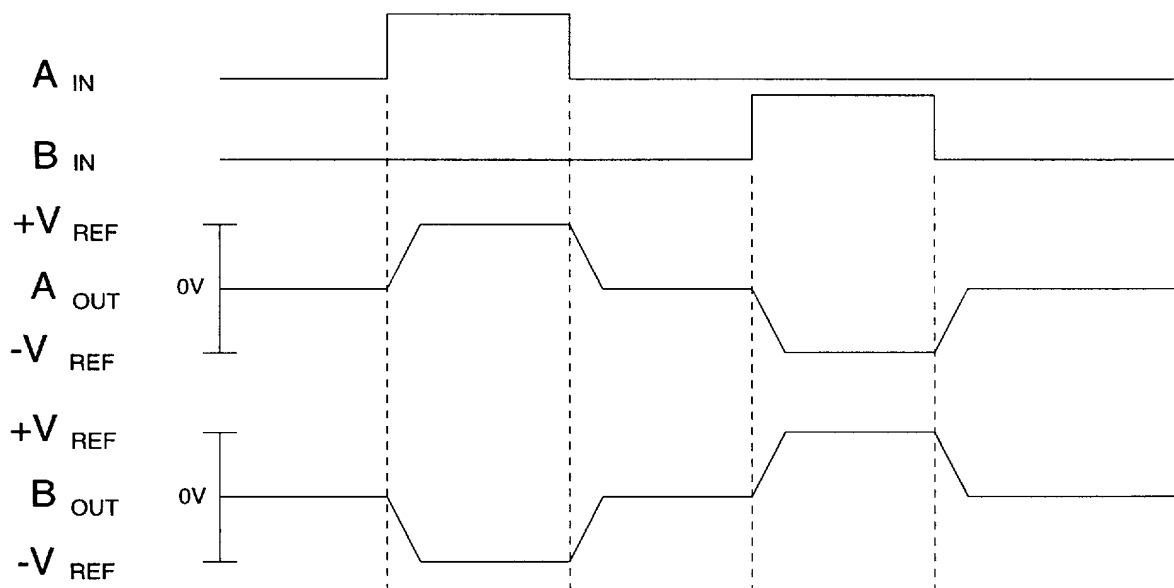
TABLE 3. DD-03182 DC ELECTRICAL CHARACTERISTICS					
CONDITIONS: Ambient Temperature = -55° C to +125° C; +V = +10.8 VDC to +16.5 VDC; -V = -10.8 VDC to -16.5 VDC; V <sub>1</sub> = V <sub>REF</sub> = +5 VDC ±5%					
PARAMETER (SYMBOL)	UNITS	MIN	TYP	MAX	TEST CONDITIONS
Quiescent +V Supply Current (I <sub>Q+V</sub> )	mA		2		No load, 429 mode. DATA=CLOCK=SYNC=L
Quiescent -V Supply Current (I <sub>Q-V</sub> )	mA		5		No load, 429 mode. DATA=CLOCK=SYNC=L
Quiescent V <sub>1</sub> Supply Current (I <sub>QV<sub>1</sub></sub> )	mA		4		No load, 429 mode. DATA=CLOCK=SYNC=L
Quiescent V <sub>REF</sub> supply current (I <sub>QV<sub>REF</sub></sub> )	μA		10		No load, 429 mode. DATA=CLOCK=SYNC=L
Logic 1 input V (V <sub>IH</sub> )	V	2.0			No load
Logic 1 input I (I <sub>IH</sub> )	μA			10	No load
Logic 0 input V (V <sub>IL</sub> )	V			0.6	No load
Logic 0 input I (I <sub>IL</sub> )	μA			-20	No load (Pin 15 I <sub>IL</sub> = -2 mA max.)
Output voltage high: +1 (V <sub>OH</sub> )	V	V <sub>REF</sub> -250mV	V <sub>REF</sub>	V <sub>REF</sub> +250mV	No load, 429 Mode.
Output voltage null: 0 (V <sub>NULL</sub> )	mV	-250		+250	No load, 429 Mode.
Output voltage low: -1 (V <sub>OL</sub> )	V	-V <sub>REF</sub> -250mV	-V <sub>REF</sub>	-V <sub>REF</sub> +250mV	No load, 429 Mode.
Timing capacitor charge current: C <sub>A</sub> [+1] C <sub>B</sub> [-1] (I <sub>CT+</sub> ) C <sub>A</sub> [-1] C <sub>B</sub> [+1] (I <sub>CT-</sub> )	μA μA		+200 -200		No load, 429 Mode. SYNC=CLOCK=H C <sub>A</sub> and C <sub>B</sub> held at 0 V
+V Short-circuit supply current (I <sub>SC</sub> [+V])	mA			+150	Output short to GND.
-V Short-circuit supply current (I <sub>SC</sub> [-V])	mA			-150	Output short to GND.
Output resistance each output (R <sub>OUT</sub> )	ohms	30	37.5	45	
Input capacitance (C <sub>IN</sub> )	pF			15	

The DD-03182 line driver is designed to take data from a box and place it on the data bus. The serial data is presented on DATA(A) and Data(B) inputs in a dual rail format. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V<sub>REF</sub> input and is normally tied to +5 VDC along with V<sub>1</sub> to produce output levels of +5 V, 0 V, and -5 V on each output for 10 V differential outputs. (See FIGURE 3.)

The outputs are fused for fail-safe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on C<sub>A</sub> and C<sub>B</sub>. Typical Values are 75 pF for 100 kHz data and 500 pF for 12.5 kHz data.

The cable used in 429 buses is a twisted, shielded pair of 20- to 26-gauge conductors. The shield is grounded at both ends of the cable run and at all production breaks. Although there is no specification placed on the cable impedance, it generally falls in the range of 60 to 80 Ω.†

† This information was taken from Cary Spitzer's book  
"Digital Avionics System Principles & Practice."



Note: The output slew rates are controlled by timing capacitors  $C_A$  and  $C_B$ . They are charged by  $\pm 200 \mu A$  (nominal). Slew rate (SR) is calculated by  $SR = 200/C$  (V/us) where C is in pF.

**FIGURE 3. ARINC 429 WAVEFORM**

TABLE 4. DD-03182 TRUTH TABLE						
SYNC (Note 1)	CLOCK (Note 1)	DATA (A) (Note 1)	DATA (B) (Note 1)	A <sub>OUT</sub> (Note 2)	B <sub>OUT</sub> (Note 2)	COMMENTS
L	X	X	X	0	0	Null
X	L	X	X	0	0	Null
H	H	L	L	0	0	Null
H	H	H	H	0	0	Null
H	H	H	L	+1	-1	Logic 1
H	H	L	H	-1	+1	Logic 0

Notes:

1. X = Don't care.
2. The A<sub>OUT</sub>/B<sub>OUT</sub> notation is as follows:  
+1 = V<sub>REF</sub> volts  
0 = 0

## DD-03182 PIN DESCRIPTION

Refer to FIGURE 4 and 5 for package pin configurations. Pin descriptions for the DD-03182DC, GP and PP follow. The DD-03182PP package pin numbers are in parenthesis.

Pin 1(1):  $V_{REF}$  (Input) - The voltage on  $V_{REF}$  sets the output voltage levels on  $A_{OUT}$  and  $B_{OUT}$ . The output logic levels swing between  $+V_{REF}$  volts, 0 volts and  $-V_{REF}$  volts.

Pins 2, 10, 15 (2, 5, 7, 8, 10, 11, 12, 18, 19, 20, 21, 24, 26, 27): N/C - No Connect

Pin 3 (4): SYNC (Input) - Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

Pin 14 (25): CLOCK (Input) - Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

Pins 4, 13 (6, 23): DATA(A)/DATA(B) (Inputs) - These signals contain the serial data to be transmitted on the ARINC 429 data bus.

Pins 5, 12 (9, 22):  $C_A/C_B$  (Analog) - External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typically,  $C_A = C_B = 75$  pF for 100 kHz data and  $C_A = C_B = 500$  pF for 12.5 kHz data.

Pins 6, 11 (13, 17):  $A_{OUT}/B_{OUT}$  (Output) - These are the line driver outputs which are connected to the aircraft serial data bus.

Pin 7 (14):  $-V$  (Input) - This is the negative supply input (-15 VDC nominal).

Pin 8 (3, 15): GND - Ground

Pin 9 (16):  $+V$  (Input) This is the positive supply input (+15 VDC nominal).

Pin 16 (28):  $V_1$  (Input) This is the logic supply input (+5 VDC nominal).

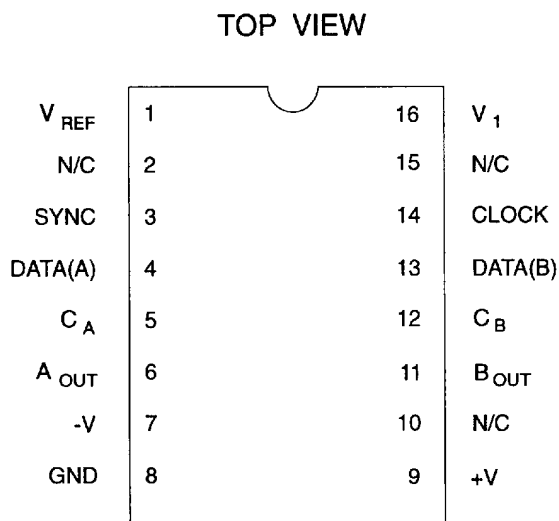


FIGURE 4. DD-03182DC AND GP  
PIN CONFIGURATION

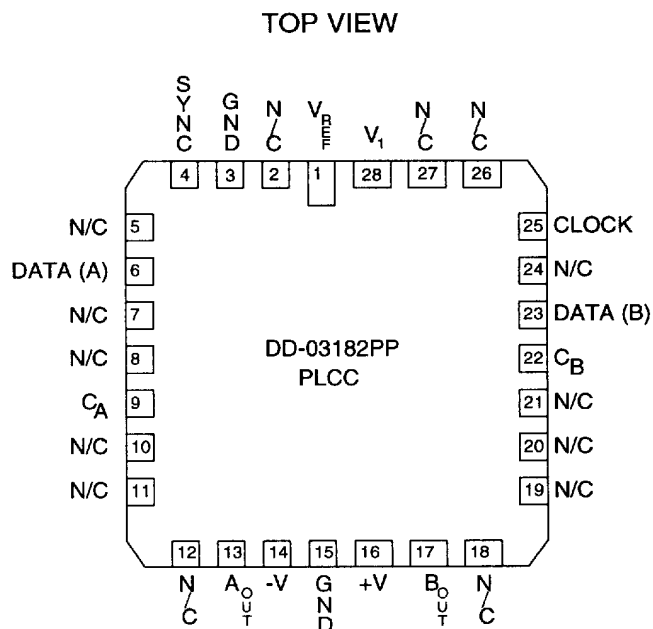


FIGURE 5. DD-03182PP PIN CONFIGURATION

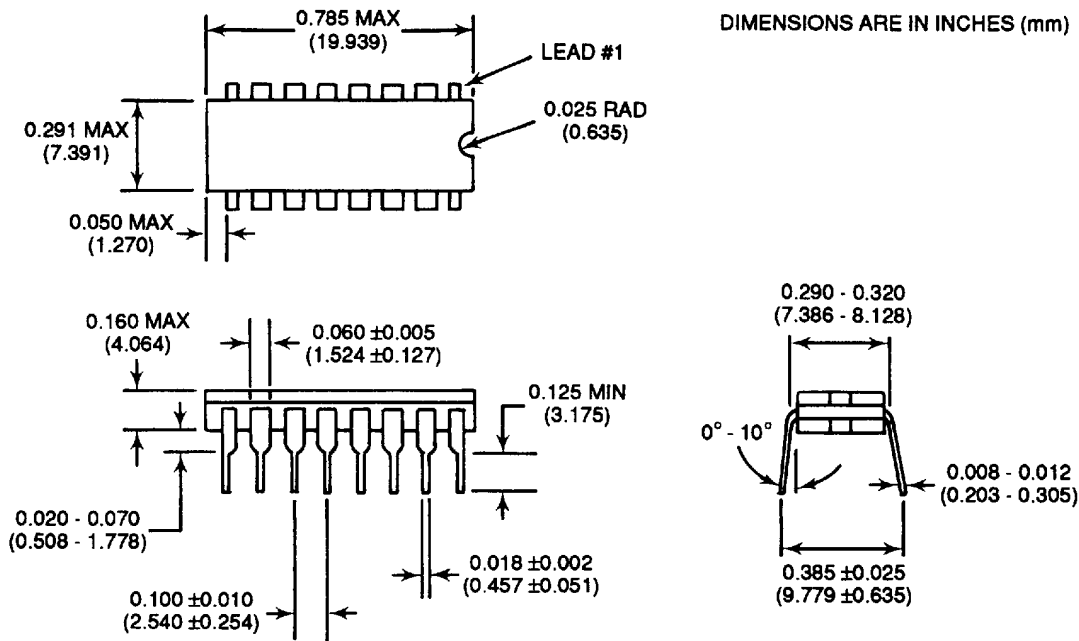


FIGURE 6. DD-03182DC: CERDIP MECHANICAL OUTLINE

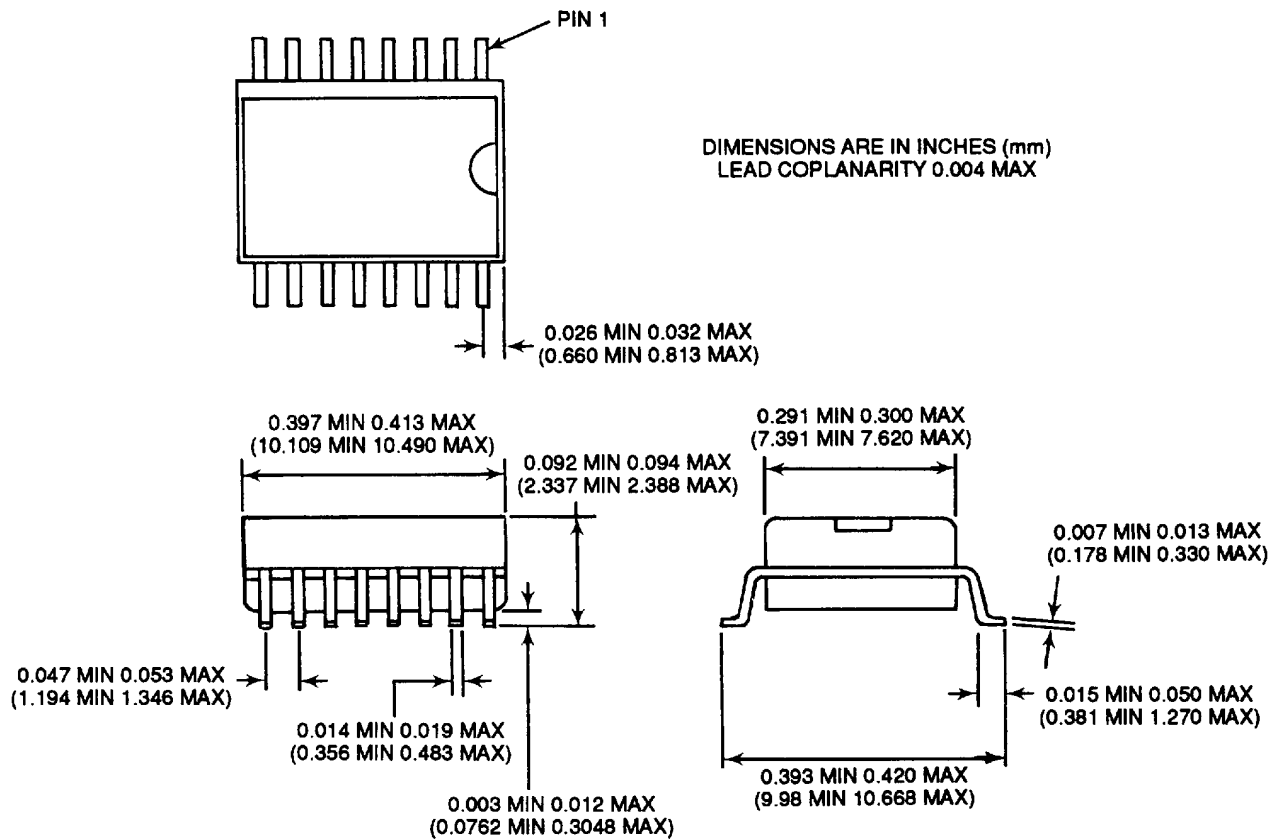


FIGURE 7. DD-03182GP: SURFACE MOUNT (SOIC) PACKAGE MECHANICAL OUTLINE

MECHANICAL DRAWING OF A 24-PIN CONNECTOR. The drawing includes top, side, and end views with the following dimensions and callouts:

- Top View Dimensions:**
  - Overall width:  $0.490 \pm 0.005$  [12.45]
  - Pin pitch (center-to-center):  $0.050 \pm 0.002$  [11.53]
  - Pin width:  $0.029$  [0.74] (TYP)
  - Lead width:  $0.050$  [1.27] (TYP)
- Side View Dimensions:**
  - Overall height:  $0.490 \pm 0.005$  [12.45]
  - Pin height:  $0.454 \pm 0.002$  [11.53]
- End View Dimensions:**
  - Pin spacing (center-to-center):  $0.175$  [4.45]
  - Pin width:  $0.100$  [2.54]
  - Pin thickness:  $0.020$  [0.51] MIN
  - Pin height:  $0.410 \pm 0.020$  [10.41]
  - Pin width:  $0.018$  [0.457]
- Callouts and Notes:**
  - ORIENTATION MARK DENOTES PIN 1
  - 6 EQ. SP @  $0.050 = 0.300$  (TOL NONCUM) (TYP)
  - 1 (Pin 1)
  - 1 (Lead cluster to be centralized about case centerline within  $\pm 0.010$ )

## ORDERING INFORMATION

### OTHER APPLICABLE DOCUMENTS