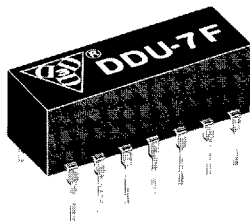


Fast Logic Digital Delay Units

SERIES: DDU-7F

**10 Taps (14 pins DIP)
TTL Interfaced**

**data
delay
devices, inc.**



Features:

- Auto-insertable.
- Completely interfaced for TTL
- No external components required
- P.C. board space economy achieved
- Fits standard 14 pins DIP socket

Specifications:

- **No. Taps:** 10 equally spaced.
- **Total Delay Tolerance:** $\pm 5\%$ or better, or 2 ns whichever is greater.
- **Rise time:** 2 ns typically.
- **Temperature coefficient:** 100 PPM/ $^{\circ}\text{C}$.
- **Temperature range:** 0° to $+70^{\circ}\text{C}$. (-55°C to $+125^{\circ}\text{C}$ on request.)*
- **Supply voltage:** 4.75 to 5.25 V.
- **Supply Current:**
I_{ccL}: 50 ma.
I_{ccH}: 15 ma.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.

*Add "M" to Part No.: Ex. DDU-7F-100ME5.
Case size: E5.

Part No.	Total Delay (ns)	Delay Per Tap (ns)
*DDU-7F-10	9	1 $\pm$.4
*DDU-7F-20	18	2 $\pm$.5
*DDU-7F-25	22.5	2.5 $\pm$.7
DDU-7F-50	50	5.0 $\pm$ 1.5
DDU-7F-100	100	10.0 $\pm$ 2
DDU-7F-150	150	15.0 $\pm$ 2
DDU-7F-200	200	20.0 $\pm$ 2
DDU-7F-250	250	25.0 $\pm$ 2
DDU-7F-300	300	30.0 $\pm$ 3
DDU-7F-400	400	40.0 $\pm$ 4
DDU-7F-500	500	50.0 $\pm$ 5

*Time delay referenced to 1st tap.
3.5 ns $\pm$ 1 ns inherent delay.

Test Conditions:

- Input Pulse Width: $\geq 150\%$ of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Unless otherwise specified all time-delays are referenced to input of delay line.
- Rise-time is measured from .75 V to 2.4 V of leading edge.
- All measurements made @ $V_{cc} = 5\text{V}$; $T_A = +25^{\circ}\text{C}$.

