



Dual Power MOSFET Drivers

General Description

The MAX626/7/8 are dual monolithic power MOSFET drivers designed to translate TTL inputs to high voltage/current outputs. The MAX626 is a dual inverting power MOSFET driver, and the MAX627 contains one inverting section and one non-inverting section. Delay times are nearly independent of V_{DD} (See Typical Operating Characteristics). High current output drivers rapidly charge and discharge the gate capacitance of even the largest power MOSFETs to within millivolts of the supply rail. This produces the power MOSFET's minimum ON resistance. The MAX626/7/8's high speed minimizes power losses in switching power supplies and DC-DC converters.

Applications

Switching Power Supplies
DC-DC Converters
Motor Controllers
Pin Diode Drivers
Charge Pump Voltage Inverters

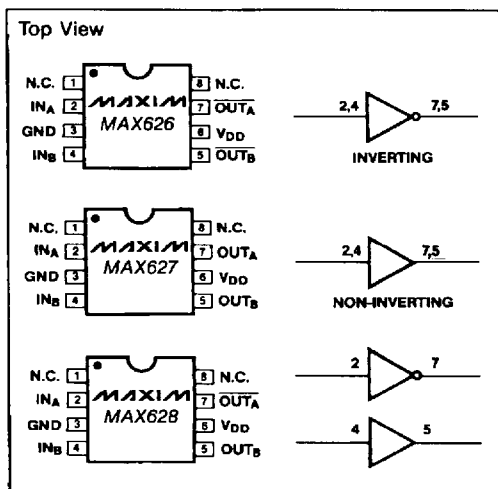
Features

- ◆ Improved Second Source For TSC426/7/8
- ◆ Fast Rise and Fall Times: Typically 20ns with 1000pF Load
- ◆ Wide Supply Range: $V_{DD} = 4.5$ to 18 Volts
- ◆ Low Power Consumption:
7mW with Inputs Low
150mW with Inputs High
- ◆ TTL/CMOS Input Compatible
- ◆ Low R_{OUT} : Typically 4Ω
- ◆ MAX626 is Pin Equivalent to TSC426, DS0026/DS0056

Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|-----------|-----------------|--------------------|
| MAX626CPA | 0°C to +70°C | 8 Lead Plastic DIP |
| MAX626CSA | 0°C to +70°C | 8 Lead SO |
| MAX626C/D | 0°C to +70°C | Dice |
| MAX626MJA | -55°C to +125°C | 8 Lead CERDIP |
| MAX627CPA | 0°C to +70°C | 8 Lead Plastic DIP |
| MAX627CSA | 0°C to +70°C | 8 Lead SO |
| MAX627C/D | 0°C to +70°C | Dice |
| MAX627MJA | -55°C to +125°C | 8 Lead CERDIP |
| MAX628CPA | 0°C to +70°C | 8 Lead Plastic DIP |
| MAX628CSA | 0°C to +70°C | 8 Lead SO |
| MAX628C/D | 0°C to +70°C | Dice |
| MAX628MJA | -55°C to +125°C | 8 Lead CERDIP |
| TSC426CPA | 0°C to +70°C | 8 Lead Plastic DIP |
| TSC426CBA | 0°C to +70°C | 8 Lead SO |
| TSC426MJA | -55°C to +125°C | 8 Lead CERDIP |
| TSC427CPA | 0°C to +70°C | 8 Lead Plastic DIP |
| TSC427CBA | 0°C to +70°C | 8 Lead SO |
| TSC427MJA | -55°C to +125°C | 8 Lead CERDIP |
| TSC428CPA | 0°C to +70°C | 8 Lead Plastic DIP |
| TSC428CBA | 0°C to +70°C | 8 Lead SO |
| TSC428MJA | -55°C to +125°C | 8 Lead CERDIP |

Pin Configurations



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MAX626/7/8-TSC426/7/8

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ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|------------------------------|---|-----------------|
| Supply Voltage V_{DD} to GND | +20V | CERDIP (derate above 70°C by 8.0mW/°C) | 640mW |
| Input Voltage | $V_{DD} + 0.3V$ to GND -0.3V | Maximum Chip Temperature | +150°C |
| Package Dissipation | | Storage Temperature | -55°C to +160°C |
| Plastic DIP (derate above 70°C by 6.25mW/°C) | 500mW | Lead Temperature (10 seconds) | +300°C |
| Small Outline (derate above 70°C by 5.88mW/°C) | 450mW | | |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX626/7/8 and TSC426/7/8

($V_{DD} = 4.5V$ to 18V, Over Temperature unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------|-----------------------|--|--------------------------|----------------|-----------------------|----------|
| Logic 1 Input Voltage | V_{IH} | | 2.4 | | | V |
| Logic 0 Input Voltage | V_{IL} | | | | 0.8 | V |
| Input Current | I_{IN} | $V_{IN} = 0V$ to 18V, $T_A = 25^\circ C$ $V_{IN} = 0V$ to 18V | -1 -10 | | 1 10 | μA |
| Output High Voltage | V_{OH} | No Load | $V_{DD} - 25$ | | | V |
| Output Low Voltage | V_{OL} | No Load | | | +25 | mV |
| Output Resistance | R_{OUT} (Note 1) | $V_{DD} = 18V$, $T_A = 25^\circ C$ $I_{LOAD} = 10mA$ | MAX626/7/8 TSC426/7/8 | 4 10 | 15 15 | Ω |
| | | $V_{DD} = 18V$ Over Temp $I_{LOAD} = 10mA$ | MAX626/7/8 TSC426/7/8 | 6 13 | 20 20 | |
| | R_{OUT} (Note 2) | $V_{DD} = 18V$, $T_A = 25^\circ C$ $I_{LOAD} = 10mA$ | MAX626/7/8 TSC426/7/8 | 4 6 | 10 10 | |
| | | $V_{DD} = 18V$ Over Temp $I_{LOAD} = 10mA$ | MAX626/7/8 TSC426/7/8 | 6 8 | 15 15 | |
| | | | | | | |
| | | | | | | |
| Peak Output Current | I_{PK} | MAX626/7/8, $V_{DD} = 18V$ TSC426/7/8, $V_{DD} = 18V$ | | 2 1.5 | | A |
| Power Supply Current | I_{SUPP} | $V_{IN} = +3V$ both inputs, $T_A = 25^\circ C$ $V_{IN} = +3V$ both inputs $V_{IN} = +0V$ both inputs, $T_A = 25^\circ C$ $V_{IN} = +0V$ both inputs | | | 8 12 0.4 0.6 | mA |
| Rise Time | t_R (Note 3) | $T_A = 25^\circ C$ Over Temp | | 20 25 25 | 30 40 60 | ns |
| Fall Time | t_F (Note 3) | $T_A = 25^\circ C$ Over Temp | | 20 25 | 30 40 | |
| Delay Time | t_{D1} (Note 3) | $T_A = 25^\circ C$ | MAX626/7/8 TSC426/7/8 | 20 20 | 30 40 | |
| | | Over Temp | MAX626/7/8 TSC426/7/8 | 25 25 | 40 60 | |
| Delay Time | t_{D2} (Note 3) | $T_A = 25^\circ C$ | MAX626/7/8 TSC426/7/8 | 25 25 | 50 75 | |
| | | Over Temp | MAX626/7/8 TSC426/7/8 | 30 30 | 60 120 | |

Note 1: $V_{IN} = 0.8V$ for inverting stages, $V_{IN} = 2.4V$ for non-inverting stages.

Note 2: $V_{IN} = 2.4V$ for inverting stages, $V_{IN} = 0.8V$ for non-inverting stages.

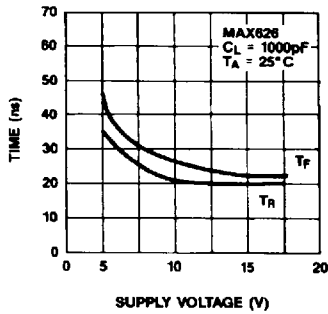
Note 3: Switching times guaranteed by design, not tested.

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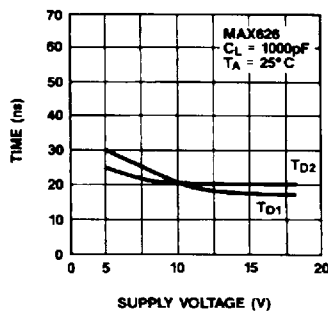
Typical Operating Characteristics

MAX626/7/8-TSC426/7/8

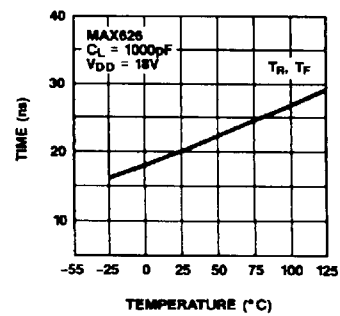
RISE AND FALL TIME
vs. SUPPLY VOLTAGE



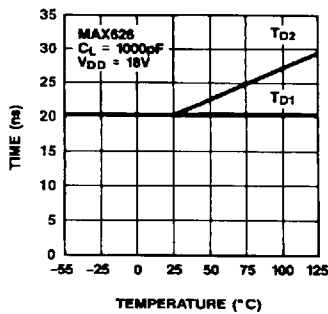
DELAY TIME vs.
SUPPLY VOLTAGE



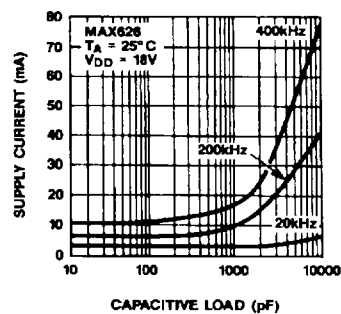
RISE AND FALL TIME
vs. TEMPERATURE



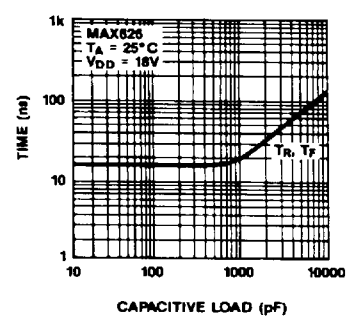
DELAY TIME
vs. TEMPERATURE



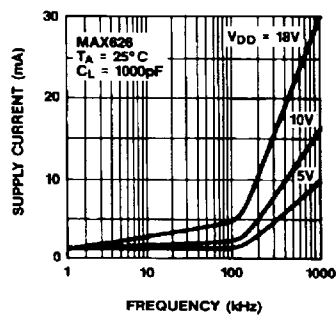
SUPPLY CURRENT vs.
CAPACITIVE LOAD



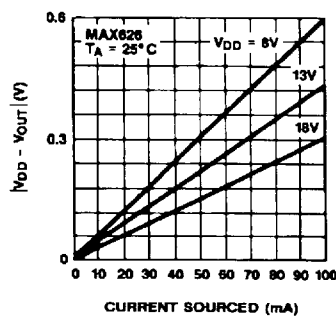
RISE AND FALL TIME
vs. CAPACITIVE LOAD



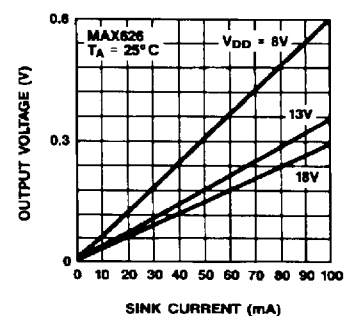
SUPPLY CURRENT
vs. FREQUENCY



HIGH OUTPUT VOLTAGE



LOW OUTPUT VOLTAGE



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Application Hints

The MAX626/7/8 have an easy to drive input, however, the input must never be allowed to stay between V_{IH} and V_{IL} for more than 50ns. Unused inputs should always be connected to ground to minimize supply current. Drivers can be paralleled on the MAX626 or MAX627 by tying both inputs together and both outputs together.

Supply bypassing and grounding are extremely important with the MAX626/7/8 as the peak supply and output currents can be greater than 2 Amps. Ground drops are a form of negative feedback with inverters and, hence, will degrade the delay and transition time of the MAX626/8. Ringing may also be a problem with large dV/dt and/or large AC currents.

Suggested bypass capacitors are a $4.7\mu F$ (low ESR) capacitor in parallel with a $0.1\mu F$ ceramic capacitor, mounted as close as possible to the MAX626/7/8. Use a ground plane if possible, or separate ground returns for inputs and outputs. Ringing can be minimized with a $5-20\Omega$ resistor in series with the output but this may degrade output transition time.

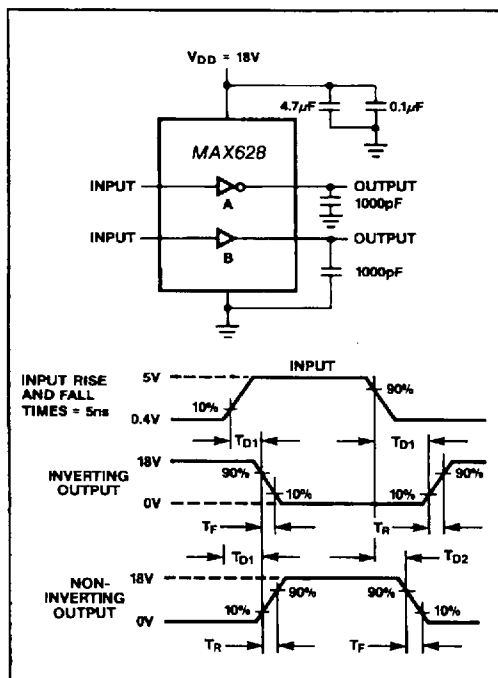


Figure 1. Inverting and Non-inverting Test Circuit

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Power Dissipation

Power dissipation of the MAX626/7/8 consists of:

- 1) Input inverter losses;
- 2) Crowbar current through the output devices;
- 3) Output current (either capacitive or resistive).

The sum of these must be kept below the maximum power dissipation limit.

The DC input inverter losses are 0.4mA when both inputs are low and 4mA when both inputs are high.

The Crowbar current through an output device making a transition is approximately 100mA for a few nanoseconds. This is a small portion of the total supply current, except for high switching frequencies or a small load capacitance (100pF).

The MAX626/7/8 power dissipation when driving a ground referenced resistive load is:

$$P = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where D is the percentage of time the MAX626/7/8 output pulls high, $R_{ON(MAX)}$ is the maximum on resistance of the inverting sections of MAX626/8 with $V_{IN} = V_{IH}$ ($V_{IN} = V_{IL}$ for non-inverting sections), the I_{LOAD} is the load current of the MAX626/7/8.

For capacitive loads, the power dissipation is:

$$P = C_{LOAD} \times V_{DD}^2 \times FREQ$$

where C_{LOAD} is the capacitive load, V_{DD} is the MAX626/7/8 supply voltage, and $FREQ$ is the toggle frequency.

Chip Topography

