# Monolithic Dual SPST CMOS Analog Switch

## FEATURES

- ±15 V Input Signal Range
- 44-V Maximum Supply Ranges
- On-Resistance: 45 Ω
- TTL and CMOS Compatibility

## BENEFITS

- Wide Dynamic Range
- Simple Interfacing
- Reduced External Component Count

## APPLICATIONS

- Servo Control Switching
- Programmable Gain Amplifiers
- Audio Switching
- Programmable Filters



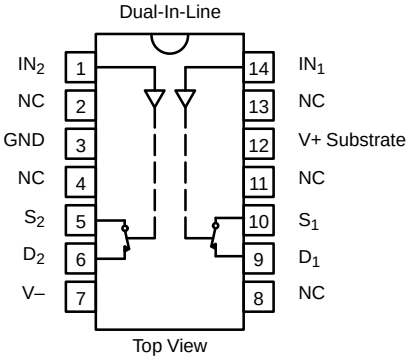
## DESCRIPTION

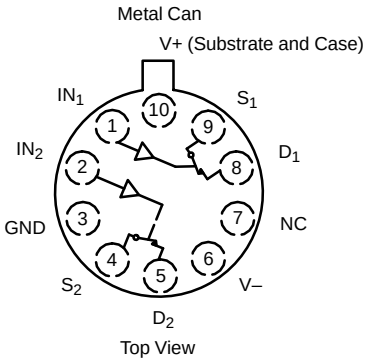
The DG200A is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low on-resistance.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. In the on condition, this bi-directional switch introduces no offset voltage of its own.

The DG200A is designed on Vishay Siliconix' improved PLUS-40 CMOS process. An epitaxial layer prevents latchup.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION




| TRUTH TABLE | |
|---|---|
| **Logic** | **Switch** |
| 0 | ON |
| 1 | OFF |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp Range** | **Package** | **Part Number** |
| 0 to 70°C | 14-Pin Plastic DIP | DG200ACJ |
| –25 to 85°C | 14-Pin CerDIP | DG200ABK |
| | 10-Pin Metal Can | DG200ABA |
| –55 to 125°C | 14-Pin CerDIP | DG200AAK |
| | | DG200AAK/883, JM38510/12301BCA, 5962-9562901QCA |
| | 10-Pin Metal Can | DG200AAA |
| | | DG200AAA/883, JM38510/12301BIC |
| | 14-Pin Sidebraze | JM38510/12301BCC |

## ABSOLUTE MAXIMUM RATINGS

V+ to V– . . . . . 44 V

GND to V– . . . . . 25 V

Digital Inputs[a], $V_S$, $V_D$ . . . . . (V–) –2 V to (V+) +2 V or 30 mA, whichever occurs first

Current (Any Terminal) Continuous . . . . . 30 mA

Current S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 100 mA

Storage Temperature (AX, BX Suffix) . . . . . –65 to 150°C
(CJ Suffix) . . . . . –65 to 125°C

Power Dissipation (Package)[b]
10-Pin Metal Can[c] . . . . . 450 mW
14-Pin CerDIP[d] . . . . . 825 mW
14-Pin Plastic DIP[e] . . . . . 470 mW

Notes:
a. Signals on $S_X$, $D_X$, or $IN_X$ exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 11 mW/°C above 75°C
e. Derate 6.5 mW/°C above 25°C

## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

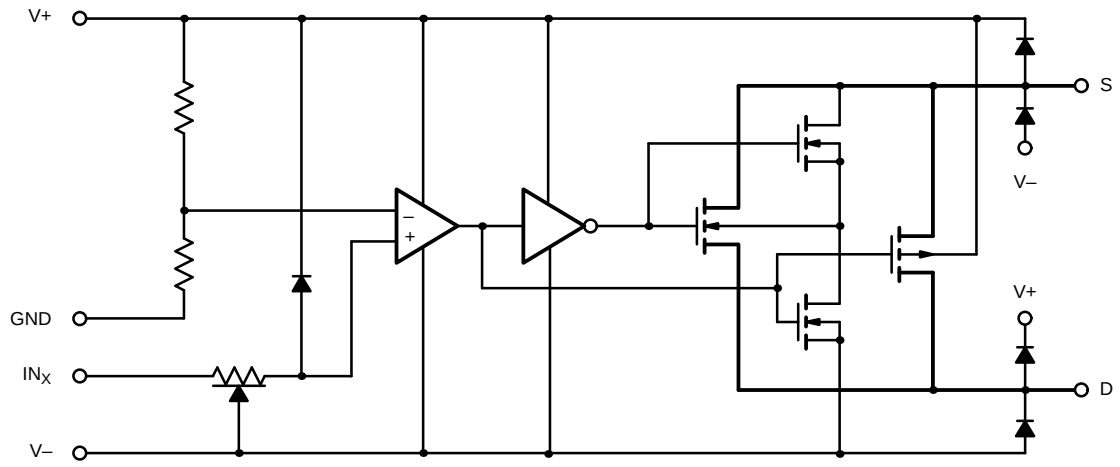



**FIGURE 1.**

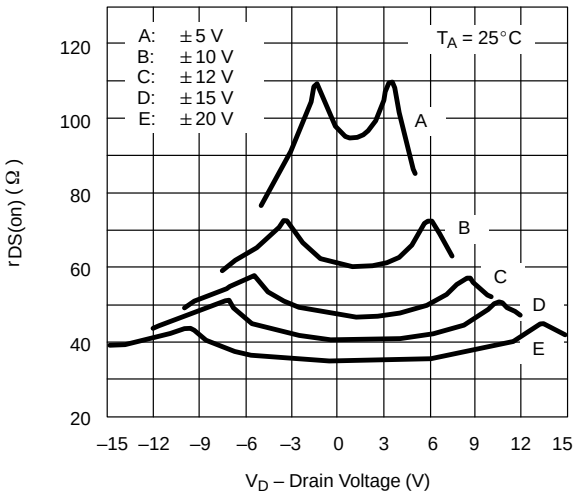
## SPECIFICATIONS[a]

| Parameter | Symbol | Test Conditions Unless Otherwise Specified<br>V+ = 15 V, V– = –15 V<br>$V_{IN}$ = 2.4 V, 0.8 V[f] | | Temp[b] | Typ[c] | A Suffix –55 to 125°C | | B, C Suffix | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min[d] | Max[d] | Min[d] | Max[d] | |
| **Analog Switch** | | | | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | | Full | | –15 | 15 | –15 | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_D$ = ±10 V, $I_S$ = –1 mA | | Room<br>Full | 45 | | 70<br>100 | | 80<br>100 | Ω |
| Source Off Leakage Current | $I_{S(off)}$ | $V_S$ = ±14 V, $V_D$ = ∓14 V | | Room<br>Full | ±0.01 | –2<br>–100 | 2<br>100 | –5<br>–100 | 5<br>100 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | $V_D$ = ±14 V, $V_S$ = ∓14 V | | Room<br>Full | ±0.01 | –2<br>–100 | 2<br>100 | –5<br>–100 | 5<br>100 | |
| Channel On Leakage Current[f] | $I_{D(on)}$ | $V_S$ = $V_D$ = ±14 V | | Room<br>Full | ±0.1 | –2<br>–200 | 2<br>200 | –5<br>–200 | 5<br>200 | |
| **Digital Control** | | | | | | | | | | |
| Input Current with Input Voltage High | $I_{INH}$ | $V_{IN}$ = 2.4 V | | Room<br>Full | 0.0009 | –0.5<br>–1 | | –1<br>–10 | | µA |
| | | $V_{IN}$ = 15 V | | Room<br>Full | 0.005 | | 0.5<br>1 | | 1<br>10 | |
| Input Current with Input Voltage Low | $I_{INL}$ | $V_{IN}$ = 0 V | | Room<br>Full | –0.0015 | –0.5<br>–1 | | –1<br>–10 | | |
| **Dynamic Characteristics** | | | | | | | | | | |
| Turn-On Time | $t_{ON}$ | See Switching Time Test Circuit | | Room | 440 | | 1000 | | 1000 | ns |
| Turn-Off Time | $t_{OFF}$ | | | Room | 340 | | 425 | | 425 | |
| Charge Injection | Q | $C_L$ = 1000 pF, $V_g$ = 0 V<br>$R_g$ = 0 Ω | | Room | –10 | | | | | pC |
| Source-Off Capacitance | $C_{S(off)}$ | f = 140 kHz<br>$V_{IN}$ = 5 V | $V_S$ = 0 V | Room | 9 | | | | | pF |
| Drain-Off Capacitance | $C_{D(off)}$ | | $V_D$ = 0 V | Room | 9 | | | | | |
| Channel-On Capacitance | $C_{D(on)}$ + $C_{S(On)}$ | $V_D$ = $V_S$ = 0 V, $V_{IN}$ = 0 V | | Room | 25 | | | | | |
| Off Isolation | OIRR | $V_{IN}$ = 5 V, $R_L$ = 75 Ω<br>$V_S$ = 2 V, f = 1 MHz | | Room | 75 | | | | | dB |
| Crosstalk (Channel-to-Channel) | $X_{TALK}$ | | | Room | 90 | | | | | |
| **Power Supplies** | | | | | | | | | | |
| Positive Supply Current | I+ | Both Channels On or Off<br>$V_{IN}$ = 0 V and 2.4 V | | Room | 0.8 | | 2 | | 2 | mA |
| Negative Supply Current | I– | | | Room | –0.23 | –1 | | –1 | | |

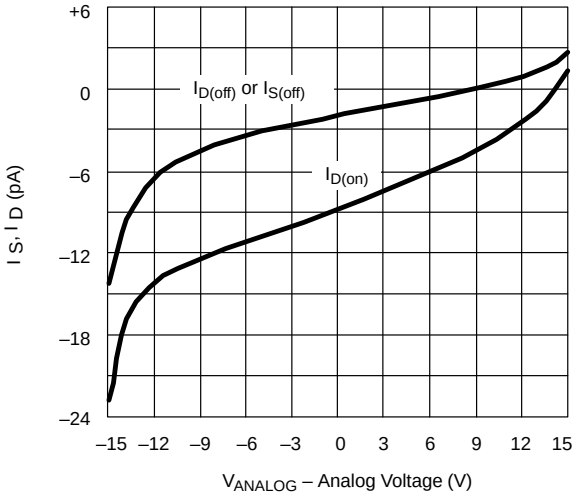
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is aminimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

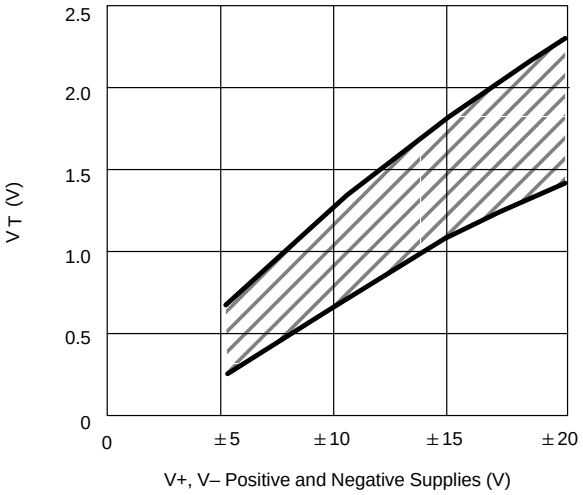
**$r_{DS(on)}$ vs. $V_D$ and Power Supply Voltage**



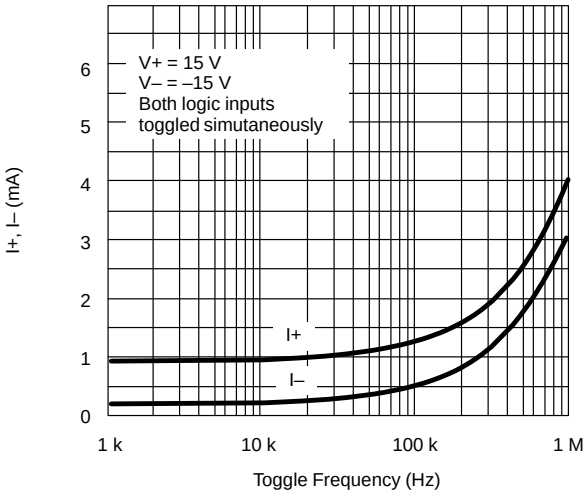

**Leakage Currents vs. Analog Voltage**




**Input Switching Threshold vs. V+ and V– Supply Voltages**




**Supply Currents vs. Toggle Frequency**



## TEST CIRCUITS

$V_O$ is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

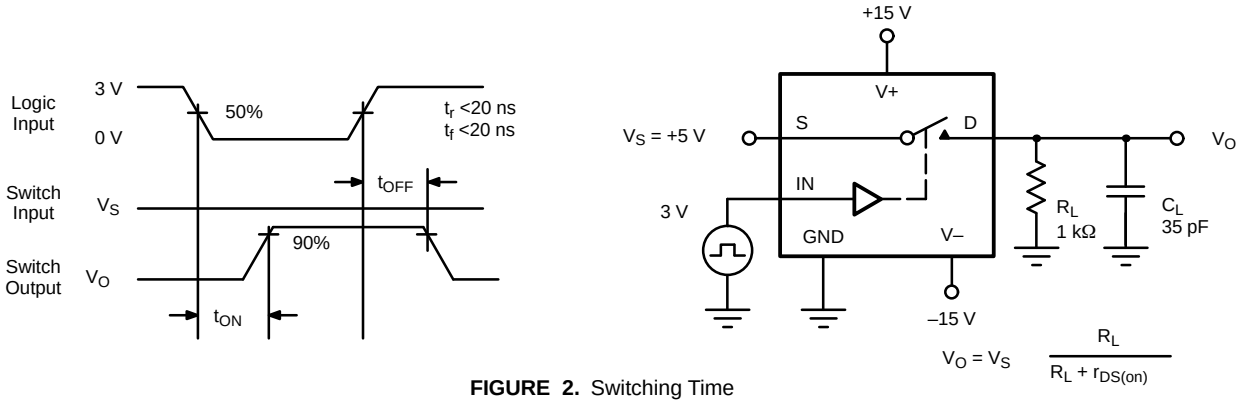



**FIGURE 2.** Switching Time

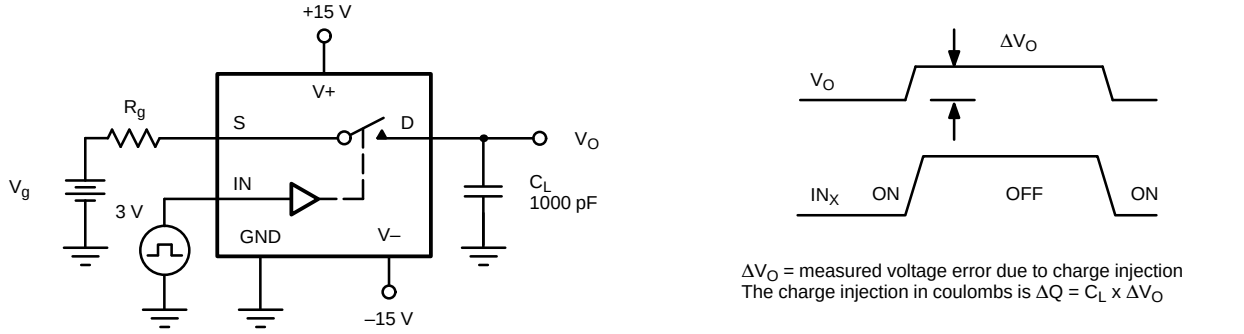



**FIGURE 3.** Charge Injection

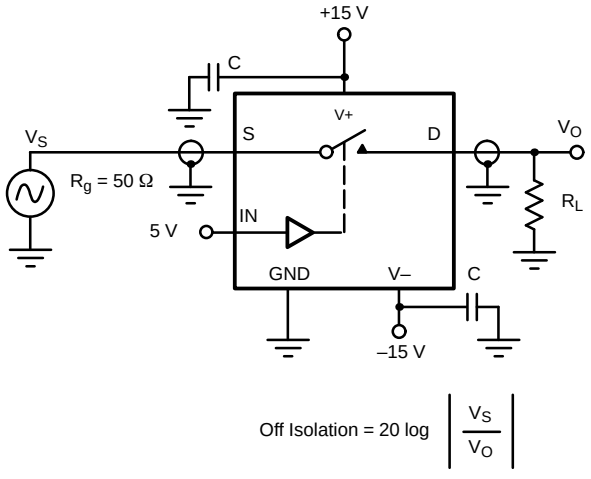



**FIGURE 4.** Off Isolation

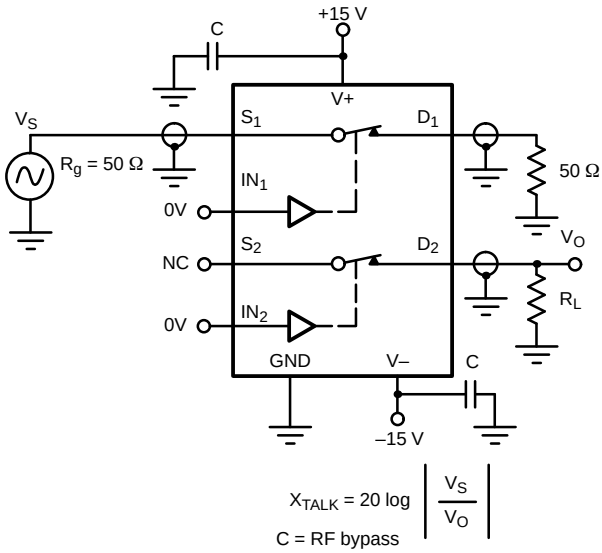



**FIGURE 5.** Channel-to-Channel Crosstalk