19-0041; Rev 0; 6/92

MAXIM

Quad, SPST, CMOS, TTL-Compatible Analog Switches

1.0 SCOPE

1.1 This specification covers the detail requirements for two quad, SPST, CMOS switches. These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	DG201AA(X)/883B
-2	DG202A(X)/883B

1.3 Package

(X)	Package	Description
K	K-16	16-Pin Ceramic Dual-In-Line Package (CERDIP)
L	F-16	16-Pin Ceramic Flat Pack (FP)
Z	Z-20	20-Pin Ceramic Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V+ to V- 44V
V+ to GND 25V
Digital Input Overvoltage Range ..... -2V to (V+ + 2V)
Current (any terminal except S or D) 30mA
Continuous Current (S or D) 20mA
Peak Current (pulsed at 1ms, 10% duty cycle max) 70mA
Power Dissipation (T_A = +70°C, T_j = +150°C)
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin FP (derate 6.60mW/°C above +70°C) 485mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Quad, SPST, CMOS, TTL-Compatible Analog Switches

1.5 Thermal Resistance

Θ_{JC} = 50°C/W for K-16
Θ_{JC} = 55°C/W for Z-20
Θ_{JC} = 65°C/W for F-16
Θ_{JA} = 100°C/W for K-16
Θ_{JA} = 110°C/W for Z-20
Θ_{JA} = 165°C/W for F-16

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS		DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Analog-Signal Range	V_{ANALOG}	V_S = ±15V		All	1, 2, 3	-15	15	V
Drain-Source On Resistance	$r_{DS(ON)}$	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	I_S = -1mA, V_D = 10V	All	1, 3		175	Ω
					2		250	
			I_S = -1mA, V_D = -10V		1, 3		175	
					2		250	
Source-Off Leakage Current	$I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	All	1		1	nA
					2		100	
			V_S = -14V, V_D = 14V		1	-1		
					2	-100		
Drain-Off Leakage Current	$I_{D(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	All	1		1	nA
					2		100	
			V_S = -14V, V_D = 14V		1	-1		
					2	-100		
Drain-On Leakage Current	$I_{D(ON)}$	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	V_S = V_D = 14V	All	1		2	nA
					2		200	
			V_S = V_D = -14V		1	-2		
					2	-200		
Input Current with Voltage High	I_{INH}	V_{IN} = 2.4V		All	1, 2, 3	-1		µA
		V_{IN} = 15V			1, 3		1	
					2		10	
Input Current with Voltage Low	I_{INL}	V_{IN} = 0V		All	1, 3	-1		µA
					2	-10		

Quad, SPST, CMOS, TTL-Compatible Analog Switches

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Positive Supply Current	I+	All channels on or off	All	1, 2		0.5	mA
				3		1.0	
Negative Supply Current	I-	All channels on or off	All	1, 3	-10		µA
				2	-100		
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1	All	9		600	ns
				10, 11		1000	
Turn-Off Time	t_{OFF}	Figure 1	All	9		450	ns
				10, 11		650	

Note 1: V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, unless otherwise noted.

3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 2.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.
(2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.

3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

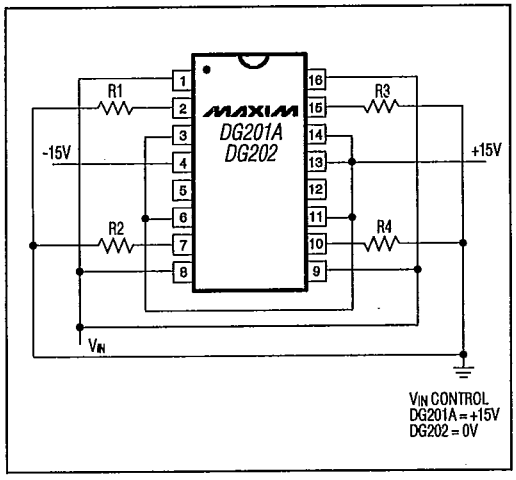
Quad, SPST, CMOS, TTL–Compatible Analog Switches

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 9, 10,** 11**
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

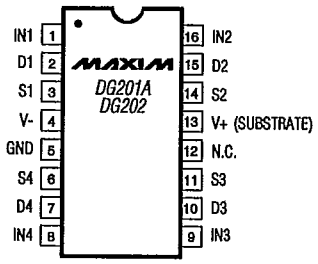
4.0 Life Test/Burn-In Circuit



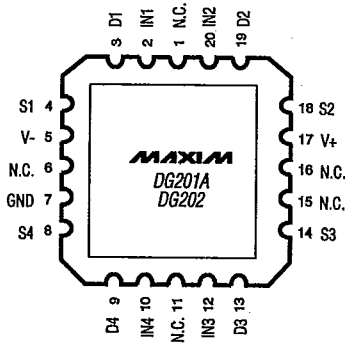
Quad, SPST, CMOS, TTL-Compatible Analog Switches

4.1 Pin Configurations

TOP VIEW

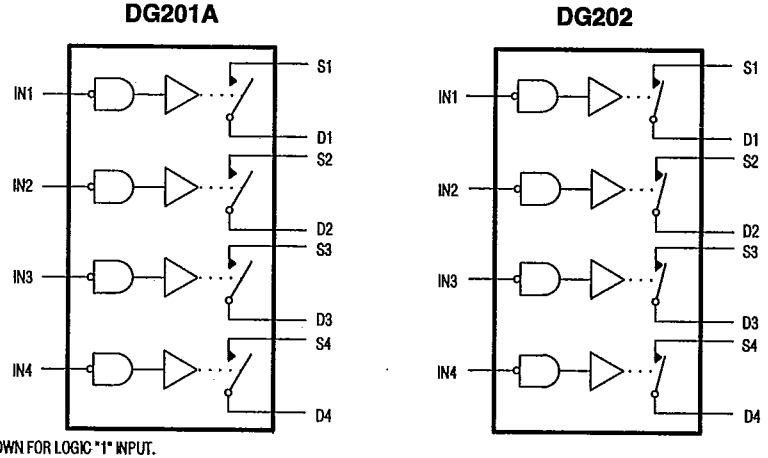


16-PIN CERDIP/ FP



20-PIN LCC

4.2 Functional Diagrams



NOTE: SWITCHES SHOWN FOR LOGIC "1" INPUT.

Quad, SPST, CMOS, TTL-Compatible Analog Switches

4.3 Truth Tables

DG201A	
Logic	**Switch**
0	ON
1	OFF

DG202	
Logic	**Switch**
0	OFF
1	ON

4.4 Timing Diagrams

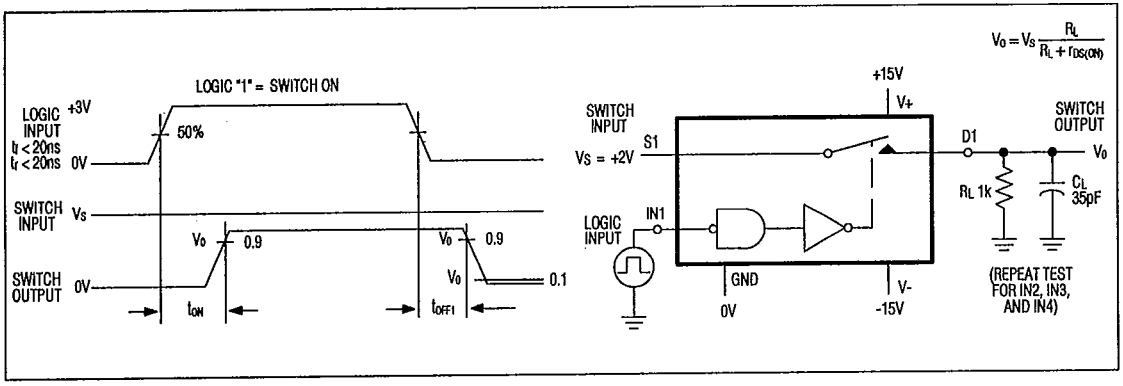


Figure 1. Switching-Time Test Circuit