19-0048; Rev 0; 12/92

MAXIM

Precision Quad, SPST, CMOS Analog Switches

1.0 SCOPE

1.1 This specification covers the detail requirements for three quad SPST CMOS switches. These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	DG411A(X)/883B
-2	DG412A(X)/883B
-3	DG413A(X)/883B

1.3 Package

(X)	Package	Description
K	J-16	16-Pin Ceramic Dual-In-Line Package (CERDIP)
Z	L-20	20-Pin Ceramic Leadless Chip Carrier

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V+ to V- 44V
GND to V- 25V
V_L ..... (GND - 0.3V) to 44V
Digital Input Overvoltage Range ..... (V- - 2V) to (V+ + 2V)
Continuous Current, Any Terminal 30mA
Current, S or D
(pulsed at 1ms, 10% duty cycle max) 100mA
Power Dissipation (T_A = +70°C, Tj = +150°C)
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

1.5 Thermal Resistance

Θ_{JC} = 50°C/W for K-16
Θ_{JC} = 55°C/W for L-20
Θ_{JA} = 100°C/W for K-16
Θ_{JA} = 110°C/W for L-20

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2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS—Dual Supplies (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
SWITCH							
Analog-Signal Range	V_{ANALOG}	V_S = ±15V (Note 2)	All	1, 2, 3	-15	15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	All	1, 3		35	Ω
				2		45	
$r_{DS(ON)}$ Matching Between Channels (Note 3)	$\Delta r_{DS(ON)}$	I_S = -10mA, V_D = ±10V, V+ = 13.5V, V- = -13.5V	All	1		15	Ω
Source-Off Leakage Current	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_S = 15.5V, V_D = 15.5V	All	1	-0.25	0.25	nA
				2	-20	20	
Drain-Off Leakage Current	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, VS = -15.5V, V_D = 15.5V	All	1	-0.25	0.25	nA
				2	-20	20	
Channel-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_S = ±15.5V, V_D = ∓15.5V	All	1	-0.4	0.4	nA
				2	-40	40	
INPUT							
Input Current with Voltage Low	I_{INL}	IN_ = 0.8V, all others = 2.4V	All	1, 2, 3	-0.5	0.5	µA
Input Current with Voltage High	I_{INH}	IN_ = 2.4V, all others = 0.8V	All	1, 2, 3	-0.5	0.5	µA
SUPPLY							
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0 or 5V	All	1		1	µA
				2		5	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0 or 5V	All	1	-1		µA
				2	-5		
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0 or 5V	All	1		1	µA
				2		5	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0 or 5V	All	1	-1		µA
				2	-5		
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1, V_S = ±10V	All	9		175	ns
				10, 11		220	
Turn-Off Time	t_{OFF}	Figure 1, V_S = ±10V	All	9		145	ns
				10, 11		160	

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TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS—Single Supply (Note 4)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
SWITCH							
Analog-Signal Range	V_{ANALOG}	Note 2	All	1, 2, 3	0	12	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA, V_D = 3.8V, V+ = 10.8V	All	1, 3		80	Ω
				2		100	
SUPPLY							
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, V_{IN} = 0V or 5V	All	1		1	µA
				2		5	
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, V_{IN} = 0V or 5V	All	1	-1		µA
				2	-5		
Logic Supply Current	I_L	All channels on or off, V_L = 5.00V, V_{IN} = 0V or 5V	All	1		1	µA
				2		5	
Ground Current	I_{GND}	All channels on or off, V_L = 5.00V, V_{IN} = 0V or 5V	All	1	-1		µA
				2	-5		
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1, V_S = 8V	All	9		250	ns
				10, 11		315	
Turn-Off Time	t_{OFF}	Figure 1, V_S = 8V	All	9		125	ns
				10, 11		140	

Note 1: V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} =2.4V, V_{INL} = 0.8V, unless otherwise noted.
Note 2: Guaranteed by design.
Note 3: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}$ MAX - $\Delta r_{DS(ON)}$ MIN.
Note 4: V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, unless otherwise noted.

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3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 2.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.
(2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.

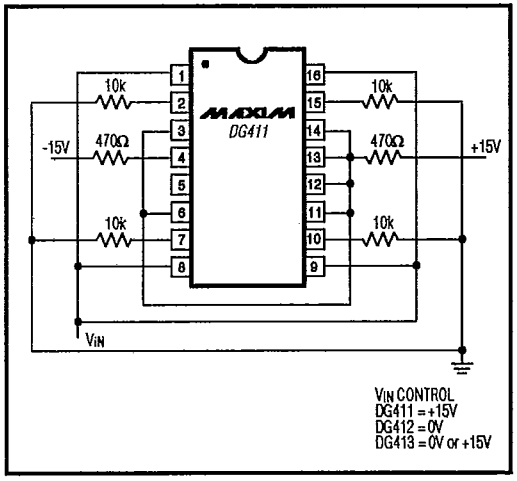
3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 9, 10,** 11**
Groups C and D End-Point Electrical Parameters (Method 5005)	1

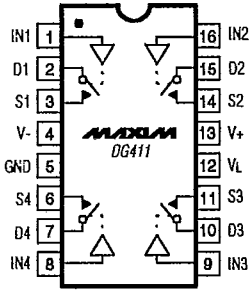
* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

4.0 Life Test/Burn-In Circuit

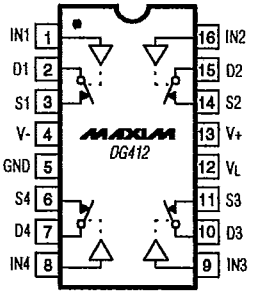


4.1 Pin Configurations/Functional Diagrams

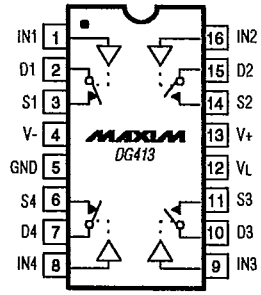
TOP VIEW



16-PIN CERDIP



16-PIN CERDIP



16-PIN CERDIP

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4.2 Truth Table

DG411		DG412	DG413	
LOGIC	SWITCH	SWITCH	SWITCH 1, SWITCH 4	SWITCH 2, SWITCH 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

4.3 Timing Diagram/Test Circuit

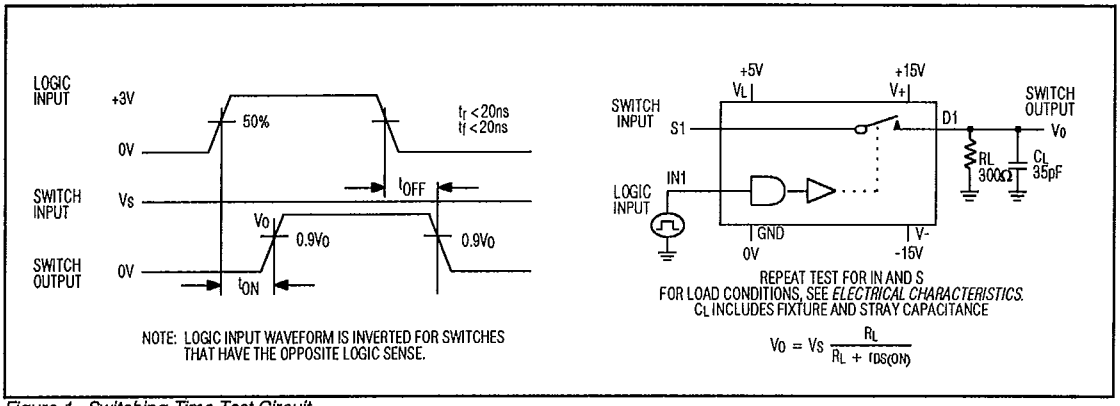

Figure 1. Switching-Time Test Circuit