

**DG5040-5045**

Monolithic General Purpose CMOS Analog Switches

T-51-11

FEATURES

- ± 15 Volt Input Range
- ON Resistance < 50 Ω
- Break-Before-Make Switching
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Sample and Hold Circuits

DESCRIPTION

The DG5040 family of solid state analog switches are recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS 40 high voltage CMOS monolithic process, these devices provide ease-of-use and performance advantages to the system designer. Key performance features of the 5040 series are 1 μ s switching, low power supply requirements, and break-before-make switching which guarantees that an ON channel will be turned OFF before an OFF channel can turn ON. Each switch conducts equally in either direction, when ON, and blocks up to 30 volts peak-to-peak when OFF. OFF leakage

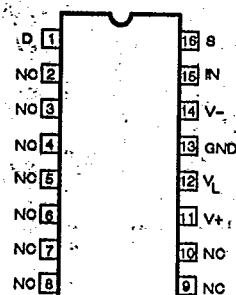
current is 1 nA maximum. A epitaxial layer prevents latch up.

There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and CerDIP. Temperature grades include commercial, C suffix (0 to 70°C), and military, A suffix (-55 to 125°C). For new designs, upgrade to the DG400-405 devices.

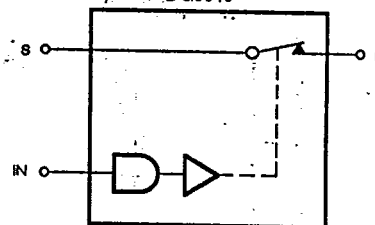
PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE

Dual-In-Line Package



Top View
Order Numbers:
CerDIP: DG5040AK
DG5040CK
Plastic: DG5040CJ

DG5040



One SPST Switch per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON

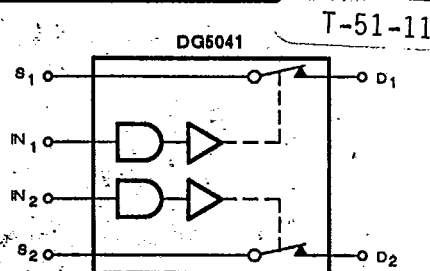
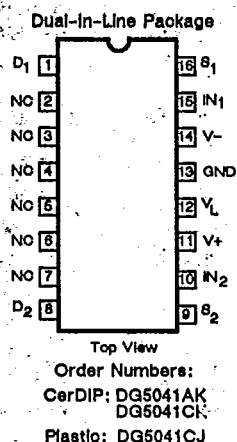
Logic "0" ≤ 0.8 VLogic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input.

DG5040-5045

Siliconix
Incorporated

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)

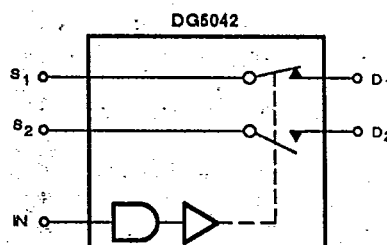
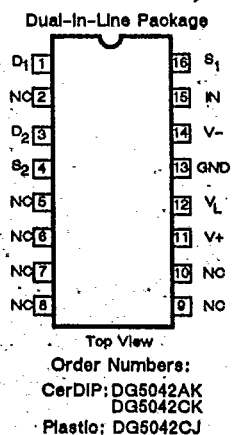


Two SPST Switches per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON

Loglo " 0 " 0.8 V
Loglo " 1 " 2.0 V

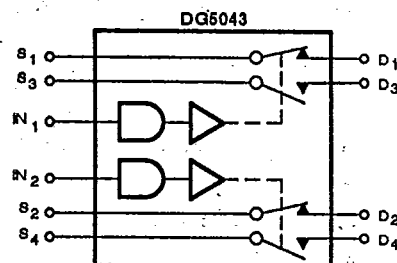
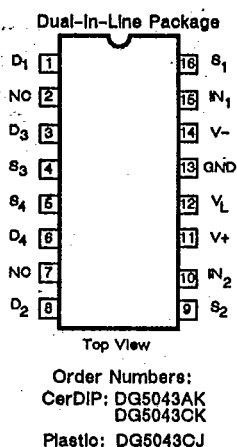


One SPDT Switch per Package

Truth Table*

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Loglo " 0 " 0.8 V
Loglo " 1 " 2.0 V



Two SPDT Switches per Package*

Truth Table*

LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Loglo " 0 " 0.8 V
Loglo " 1 " 2.0 V

*Switches Shown for Loglo "1" Input

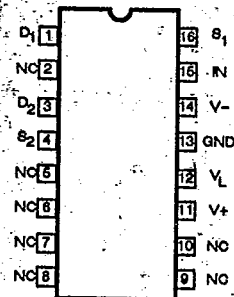


DG5040-5045

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)

T-51-11

Dual-In-Line Package



Top View

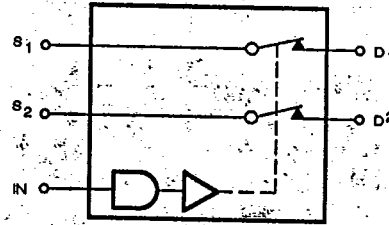
Order Numbers:

CerDIP: DG5044AK

DG5044CK

Plastio: DG5044CJ

DG5044

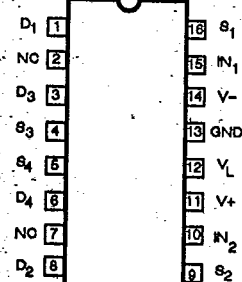


One DPST Switch per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON
Logic "0"	0.8 V
Logic "1"	2.0 V

Dual-In-Line Package



Top View

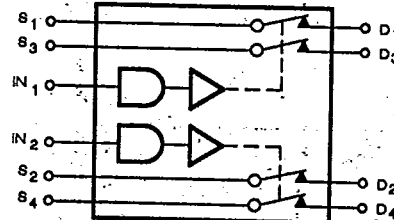
Order Numbers:

CerDIP: DG5045AK

DG5045CK

Plastio: DG5045CJ

DG5045



Two DPST Switches per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON
Logic "0"	0.8 V
Logic "1"	2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44V

VL (GND - 0.3 V) to 44 V

GND 25V

Digital Inputs^f V_S, V_D ... (V- minus 2 V) to (V+ plus 2 V)
or 30 mA, whichever occurs first

Current (any terminal except S or D) 30 mA

Continuous Current (S or D) 30 mA

Peak Current (S or D)

Pulsed 1 ms 10% duty cycle max 100 mA

Storage Temperature (A Suffix) -65 to 150°C
(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C
(C Suffix) 0 to 70°C

Power Dissipation*

16-Pin Plastic DIP** 450 mW

16-Pin Ceramic DIP*** 900 mW

* All leads welded or soldered to PC board.

** Derate 6 mW/°C above 75°C

*** Derate 12 mW/°C above 75°C

DG5040-5045**B** Siliconix
Incorporated

T-51-11

ELECTRICAL CHARACTERISTICS ^a										T-51-11
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V ₊ = 15 V V ₋ = -15 V V _L = 5 V GND = 0 V V _{IN} = 2.0 V, 0.8 V ^e	LIMITS						UNIT	
			1=25°C 2=125,70°C 3=-55,0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C			
			TEMP	TYP ^d	MIN ^b	MAX ^b	MIN ^b	MAX ^b		
SWITCH										
Analog Signal Range ^o	V _{ANALOG}		1,2,3		-15	15	-15	15	V	
Drain-Source ON Resistance	r _{DS(ON)}	I _S = -10 mA, V _D = ±10 V	1,3 2			50 75		50 75	Ω	
Switch OFF Leakage Current	I _{S(OFF)}	V _D = -14 V, V _S = 14 V V _D = 14 V, V _S = -14 V	1 2		-1 -100	1 100	-1 -100	1 100	nA	
	I _{D(OFF)}		1 2		-1 -100	1 100	-1 -100	1 100		
Channel ON Leakage Current	I _{D(ON)} + I _{S(ON)}	V _S = V _D = 14 V	1 2			2 200		2 200		
		V _S = V _D = -14 V	1 2		-2 -200		-2 -200			
INPUT										
Input Current with V _{IN} LOW	I _{IL}	V _{IN} under test = 0.8 V	1,2		-1.0	1.0	-1.0	1.0	μA	
Input Current with V _{IN} HIGH	I _{IH}	V _{IN} under test = 2.0 V	1,2		-1.0	1.0	-1.0	1.0		
DYNAMIC										
Turn-ON Time	t _{ON}	V _S = ±10 V R _L = 1 kΩ, C _L = 35 pF See Figure 1A	1			1000		1200	ns	
Turn-OFF Time	t _{OFF}		1			500		700		
Charge Injection ^a	Q	C _L = 10,000 pF V _{gen} = 0 V, R _{gen} = 0 Ω	1	30					pC	
Off Isolation ^o		R _L = 75 Ω, C _L = 5 pF f = 1 MHz	1	75					dB	
Crosstalk ^o (Channel-to-Channel)		R _L = 75 Ω, V _S = 2 Vp-p f = 1 MHz	1	89						
Source-OFF Capacitance ^o	C _{S(OFF)}	V _D = V _S = 0 V f = 1 MHz	1	15					pF	
Drain-OFF Capacitance ^o	C _{D(OFF)}		1	17						
Channel ON Capacitance ^o	C _{D(ON)} + C _{S(ON)}		1	45						

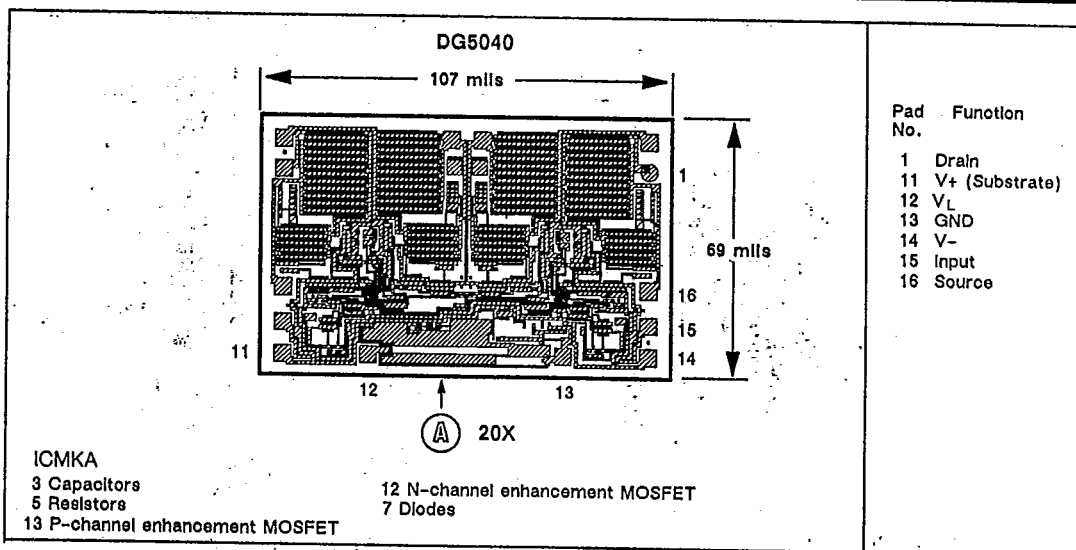
**DG5040-5045****ELECTRICAL CHARACTERISTICS^a**

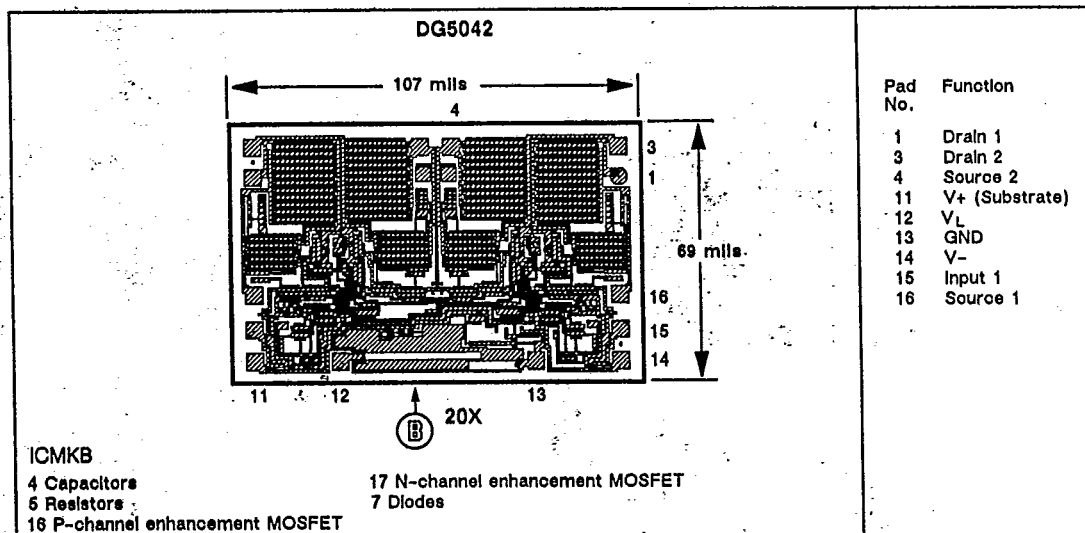
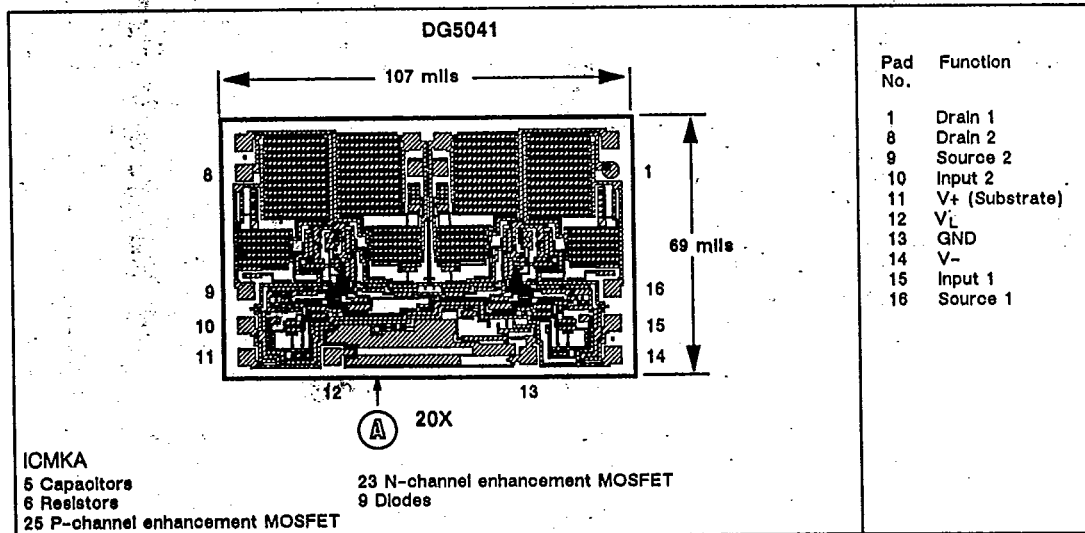
T-51-11

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V ₊ = 15 V V ₋ = -15 V V _L = 5 V GND = 0 V V _{IN} = 2.0 V, 0.8 V ^a	LIMITS						UNIT
			1=25°C		A SUFFIX		C SUFFIX		
			2=125,70°C		-55 to 125°C		0 to 70°C		
			TEMP	TYP ^d	MIN ^b	MAX ^b	MIN ^b	MAX ^b	
SUPPLY									
Positive Supply Current	I ₊	V _{IN} = 0.0 or 2.4 V	1,2			300		300	μA
Negative Supply Current	I ₋		1,2		-300		-300		
Logic Supply Current	I _L		1,2			300		300	
Ground Current	I _{GND}		1,2		-300		-300		

NOTES:

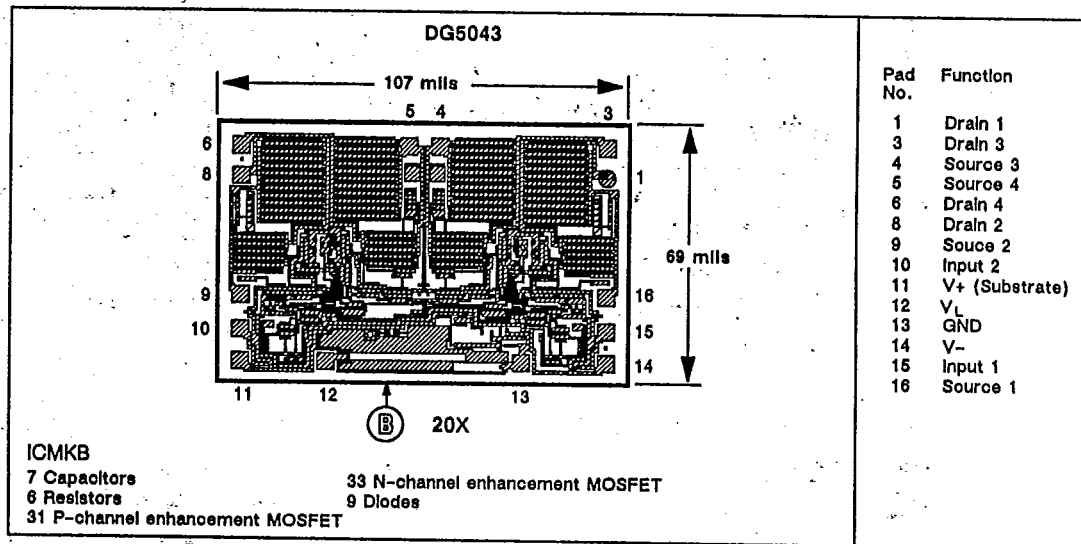
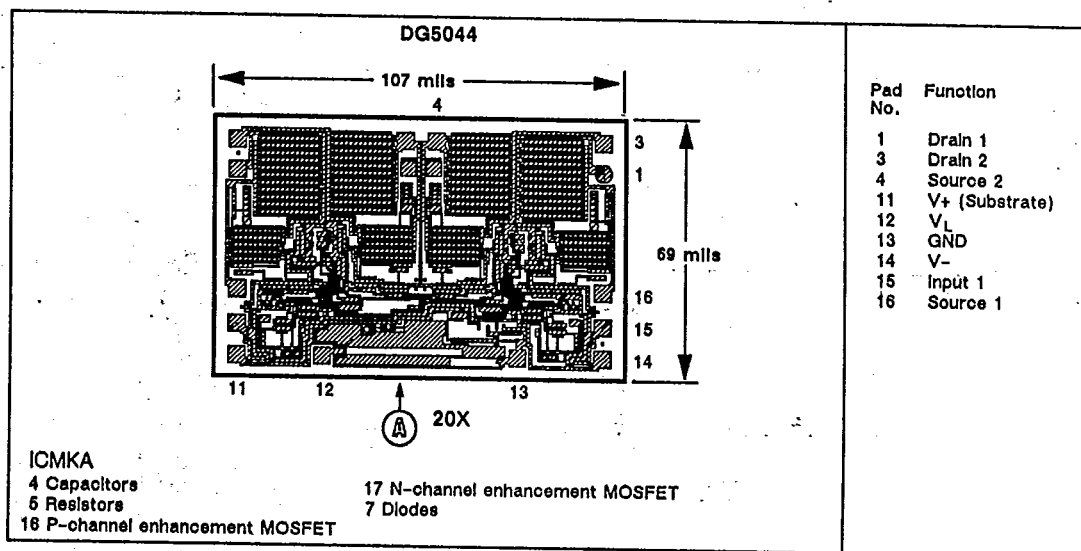
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
 b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
 c. Guaranteed by design, not subject to production test.
 d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
 e. V_{IN} = Input voltage to perform proper function.
 f. Signals on S_X, D_X or IN_X exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to 30 mA.

DIE TOPOGRAPHY

DG5040-5045**B** Siliconix
Incorporated**DIE TOPOGRAPHY (Cont'd)****T-51-11**

**DG5040-5045****DIE TOPOGRAPHY (Cont'd)**

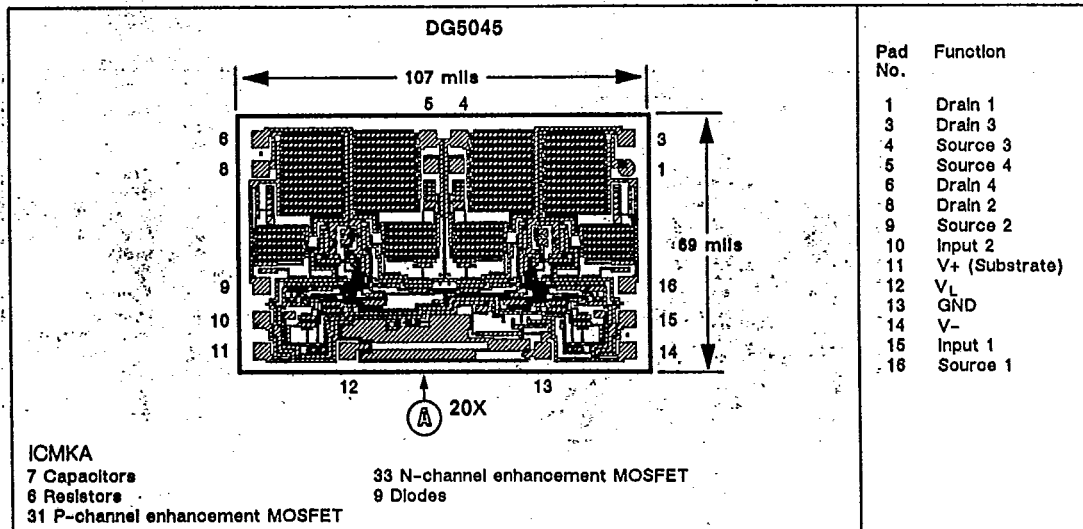
T-51-11

**5**

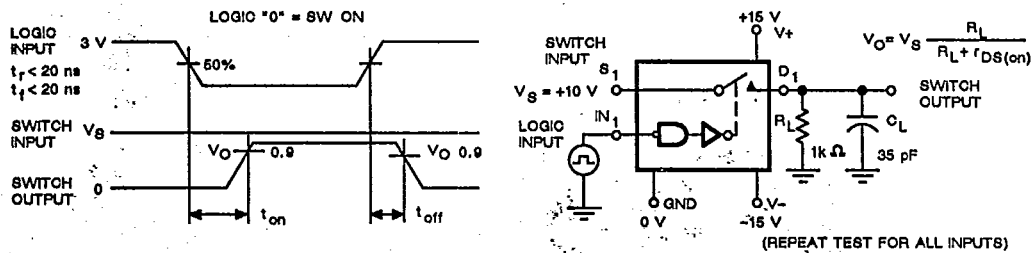
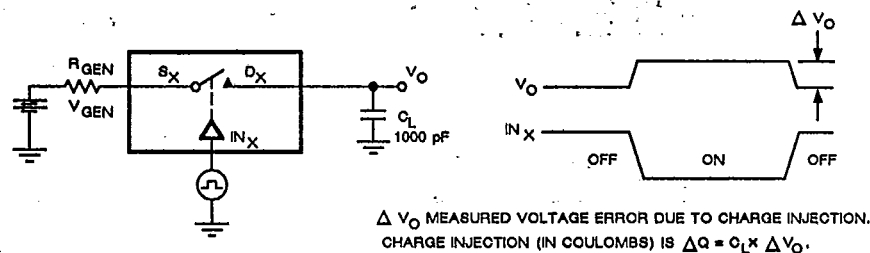
DG5040-5045**B** Siliconix Incorporated

DIE TOPOGRAPHY (Cont'd)

T-51-11

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for $V_S =$ constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

**CHARGE INJECTION TEST CIRCUIT**

**DG5040-5045**

SCHEMATIC DIAGRAM (Typical Channel)

T-51-11

