

4-/8-Channel Wideband Video Multiplexers

Features

- Wide Bandwidth: 500 MHz
- Very Low Crosstalk: -97 dB @ 5 MHz
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply
- Low $r_{DS(on)}$: $45\ \Omega$

Benefits

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

Applications

- Wideband Signal Routing and Multiplexing
- Video Switchers
- ATE Systems
- Infrared Imaging

Description

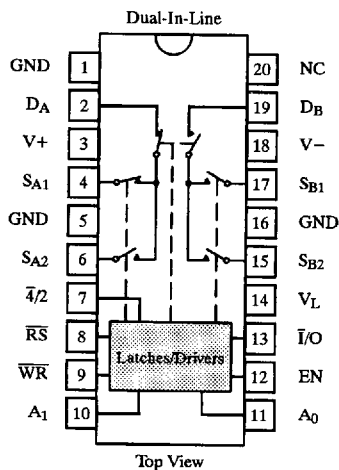
The DG534 is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538 is an 8-channel or dual 4-channel multiplexer. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low on-resistance and low capacitance of these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG534/DG538 are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of off isolation. Crosstalk is reduced to -97 dB at 5 MHz by including a ground line between each adjacent signal path.

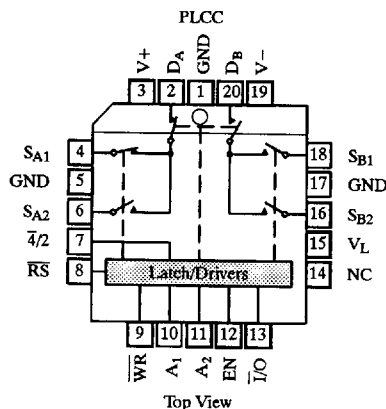
The DG534A/DG538A are recommended for new designs.

Functional Block Diagrams and Pin Configurations

DG534DJ

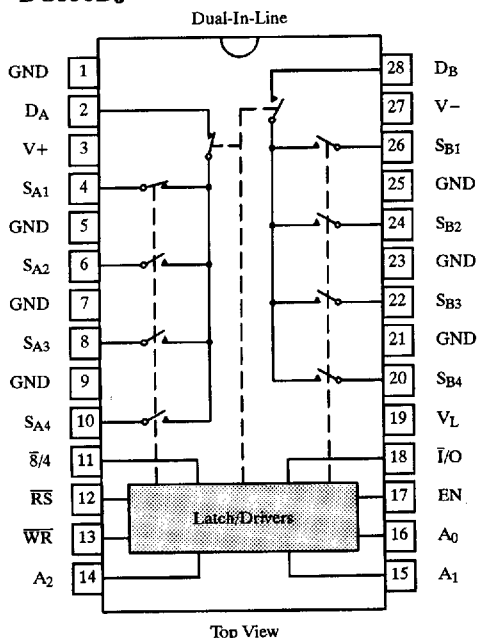


DG534DN

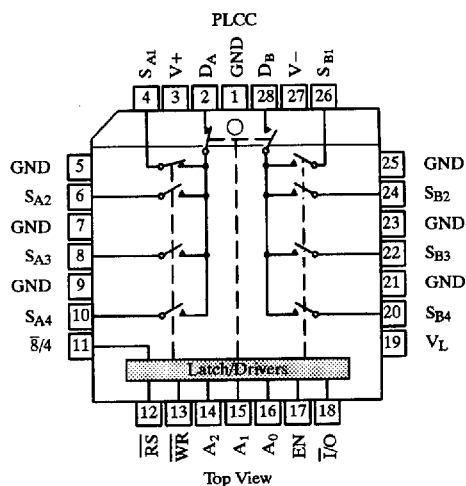


Functional Block Diagrams and Pin Configurations (Cont'd)

DG538DJ



DG538DN



Truth Tables and Ordering Information

Ordering Information — DG534

Temp Range	Package	Part Number
-40 to 85°C	20-Pin Plastic DIP	DG534DJ
	20-Pin PLCC	DG534DN
-55 to 125°C	20-Pin Sidebraz	DG534AP
		DG534AP/883

Truth Table — DG534

I/O	A ₁	A ₀	EN	WR	RS	4/2 ^a	On Switch	
X	X	X	X	1	1	1	Maintains previous state	
X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	0	0	1	X	None	
0	0	0	1	0	1	0	SA ₁	D _A and D _B may be connected externally Latches Transparent
0	0	1	1	0	1	0	SA ₂	
0	1	0	1	0	1	0	SB ₁	
0	1	1	1	0	1	0	SB ₂	
0	X	0	1	0	1	1	SA ₁ and SB ₁	
0	X	1	1	0	1	1	SA ₂ and SB ₂	
1	Note b			1	1	Note c		

Logic "0" = $V_{AL} \leq 0.8 V$

Logic "1" = $V_{AH} \geq 2 V$

X = Don't Care

Notes:

- Connect D_A and D_B together externally for single-ended operation.
- With I/O high, A_n pin becomes output and reflects latch contents. See timing diagrams for more detail.
- 4/2 can be either "1" or "0" but should not change during these operations.

Truth Tables and Ordering Information (Cont'd)

Ordering Information — DG538

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG538DJ
	28-Pin PLCC	DG538DN
-55 to 125°C	28-Pin Sidebraz	DG538AP
		DG538AP/883

Truth Table — DG538

I/O	A ₂	A ₁	A ₀	EN	WR	RS	8/4 ^a	On Switch		
X	X	X	X	X	1	1	1	Maintains previous state		
X	X	X	X	X	X	0	X	None (latches cleared)		
X	X	X	X	0	0	1	X	None		
0	0	0	0	1	0	1	0	SA ₁	D _A and D _B should be connected externally	Latches Transparent
0	0	0	1	1	0	1	0	SA ₂		
0	0	1	0	1	0	1	0	SA ₃		
0	0	1	1	1	0	1	0	SA ₄		
0	1	0	0	1	0	1	0	SB ₁		
0	1	0	1	1	0	1	0	SB ₂		
0	1	1	0	1	0	1	0	SB ₃		
0	1	1	1	1	0	1	0	SB ₄		
0	X	0	0	1	0	1	1	SA ₁ and SB ₁		
0	X	0	1	1	0	1	1	SA ₂ and SB ₂		
0	X	1	0	1	0	1	1	SA ₃ and SB ₃		
0	X	1	1	1	0	1	1	SA ₄ and SB ₄		
1	Note b				1	1	Note c			

Logic "0" = $V_{AL} \leq 0.8 V$

Logic "1" = $V_{AH} \geq 2 V$

X = Don't Care

Notes:

- Connect D_A and D_B together externally for single-ended operation.
- With I/O high, A_n pin becomes output and reflects latch contents. See timing diagrams for more detail.
- 8/4 can be either "1" or "0" but should not change during these operations.

Absolute Maximum Ratings

V ₊ to GND	-0.3 V to +21 V
V ₊ to V ₋	-0.3 V to +21 V
V ₋ to GND	-10 V to +0.3 V
V _L	0 V to (V ₊) + 0.3 V
Digital Inputs	(V ₋) -0.3 V to (V ₊) + 0.3 V or 20 mA, whichever occurs first
V _S , V _D	(V ₋) -0.3 V to (V ₋) + 14 V or 20 mA, whichever occurs first
Current (any terminal) Continuous	20 mA
Current(S or D) Pulsed 1 ms 10% Duty	40 mA

Storage Temperature	(A Suffix)	-65 to 150°C
	(D Suffix)	-65 to 125°C

Power Dissipation (Package)^a

Plastic DIP ^b	625 mW
PLCC ^c	450 mW
Sidebrazed ^d	1200 mW

Notes:

- All leads soldered or welded to PC board.
- Derate 8.3 mW/°C above 75°C.
- Derate 6 mW/°C above 75°C.
- Derate 16 mW/°C above 75°C.

Specifications^a

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -3 V, VL = 5 V WR = 0.8 V, RS, EN = 2 V	Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min ^d	Max ^d	Min ^d	Max ^d		
					Analog Switch					
Analog Signal Range ^g	V _{ANALOG}	V- = -5 V	Full		-5	8	-5	8	V	
Drain-Source On-Resistance	r _{DS(on)}	I _S = -10 mA, V _S = 0 V V _{AIL} = 0.8 V, V _{AIH} = 2 V Sequence Each Switch On	Room Full	45		90 120		90 120	Ω	
Resistance Match Between Channels	Δr _{DS(on)}		Room			9		9		
Source Off Leakage Current	I _{S(off)}	V _S = 8 V, V _D = 0 V, EN = 0.8 V	Room Full	0.05	-5 -50	5 50	-5 -50	5 50	nA	
Drain Off Leakage Current	I _{D(off)}	V _S = 0 V, V _D = 8 V, EN = 0.8 V	Room Full	0.1	-20 -500	20 500	-20 -100	20 100		
Drain On Leakage Current	I _{D(on)}	V _S = V _D = 8 V	Room Full	0.1	-20 -1000	20 1000	-20 -200	20 200		
Digital Control										
Input Voltage High	V _{AIH}		Full		2		2		V	
Input Voltage Low	V _{AIL}		Full			0.8		0.8		
Address Input Current	I _{AI}	V _{AI} = 0 V, or 2 V or 5 V	Room Full	-0.1	-1 -10	1 10	-1 -10	1 10	μA	
Address Output Current	I _{AO}	V _{AO} = 2.7 V V _{AO} = 0.4 V	Room	-300 300						
Dynamic Characteristics										
On State Input Capacitance ^g	C _{S(on)}		PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance ^g	C _{S(off)}		PLCC	Room	3		5		4	
			DIP	Room	4				5	
Off State Output Capacitance ^g	C _{D(off)}		PLCC	Room	6		10		8	
			DIP	Room	8				10	
Transition Time	t _{TRANS}		Room Full	170		300 500		300 500	ns	
Break-Before-Make Interval	t _{OPEN}		Room Full	80	50 25		50 25			
EN, WR Turn On Time	t _{ON}		Room Full	180		300 500		300 500		
EN, Turn Off Time	t _{OFF}		Room Full	95		175 300		175 300		
Charge Injection	Q _i		Room	-70					pC	
Chip Disabled Crosstalk ^f	X _{TALK(CD)}	R _L = 75 Ω, f = 5 MHz EN = 0.8 V	PLCC	Room	-75				dB	
			DIP	Room	-65					
Adjacent Input Crosstalk ^f	X _{TALK(AI)}	R _{IN} = 10 Ω, R _L = 10 kΩ f = 5 MHz	PLCC	Room	-97					
			DIP	Room	-87					
		R _{IN} = 75 Ω, R _L = 75 Ω f = 5 MHz	PLCC	Room	-80					
			DIP	Room	-70					

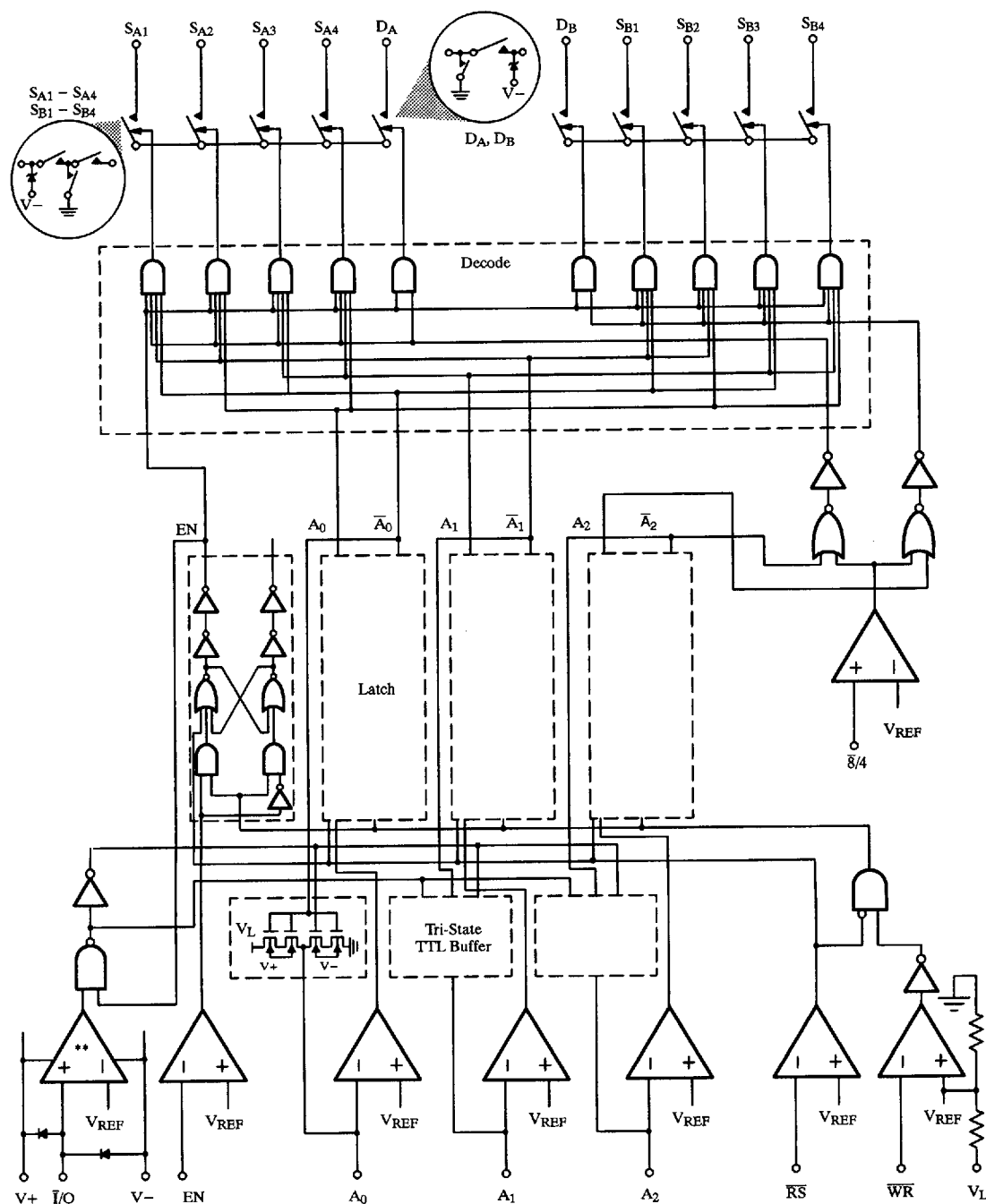
Specifications^a

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -3 V, VL = 5 V WR = 0.8 V, RS, EN = 2 V		Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min ^d	Max ^d	Min ^d	Max ^d	
Dynamic Characteristics (Cont'd)										
All Hostile Crosstalk	XTALK(AH)	RIN = 10 Ω, RL = 10 kΩ f = 5 MHz	PLCC	Room	-77					dB
			DIP	Room	-72					
		RIN = 75 Ω, RL = 75 Ω f = 5 MHz	PLCC	Room	-77					
			DIP	Room	-72					
Differential Crosstalk	XTALK(DIFF)	RIN = 10 Ω, RL = 10 kΩ f = 5 MHz		Room	-84					
		RIN = RL = 75 Ω f = 5 MHz		Room	-84					
Bandwidth	BW	RL = 50 Ω		Room	500					MHz
Power Supplies										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or V+		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I-			Room Full	0.6	-1.8 -2		-1.8 -2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V-	Functional Test Only		Full		10	21	10	21	V
	V- to GND			Full		-5.5	0	-5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	IL			Full	150		500		500	μA
Timing										
Reset to Write	tRW	See Figure 1		Full		50		50		ns
WR, RS Minimum Pulse Width	tMPW			Full		200		200		
A0, A1, EN Data Valid to Strobe	tDW			Full		100		100		
A0, A1, EN Data Valid after Strobe	tWD			Full		50		50		
Address Bus Tri-State ^e	tAZ			Room	25					
Address Bus Output	tAO			Room	95					
Address Bus Input	tAI			Room	110					

Notes:

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Defined by system bus requirements.
- Each individual pin shown as GND must be grounded.
- Guaranteed by design, not subject to production test.

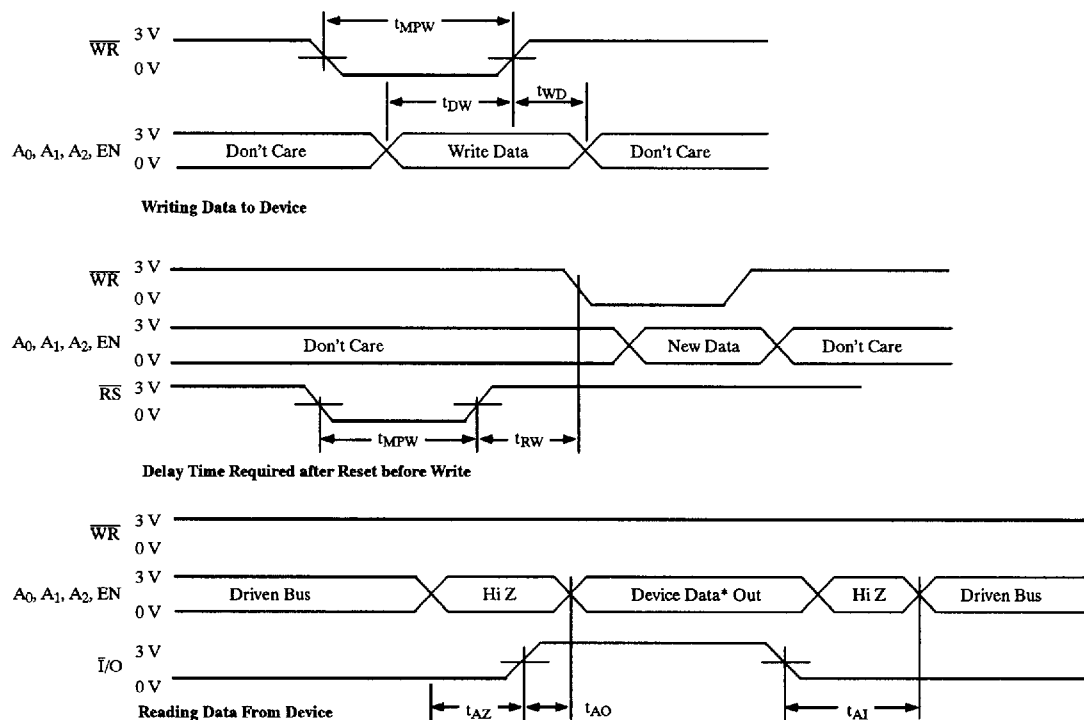
Control Circuitry



* Decode section includes delay circuitry in AND gating to ensure proper break-before-make operation.

** Typical all digital inputs.

Output Timing Requirements



* Enable must be latched high to read data, otherwise BUS is high Z. $V_- \leq -3$ V required for readback functionality.

Figure 1.

Applications

To protect against latchup V_L must not exceed V_+ by more than 0.3 V. This is easily achieved by generating V_L from V_+ using a Zener or a resistor divider network as shown in Figure 2. When an external V_L is available the alternative

simple protection circuit shown in Figure 3 should be used to prevent triggering the parasitic SCR during power up. The DG53XA does not require these protection diodes.

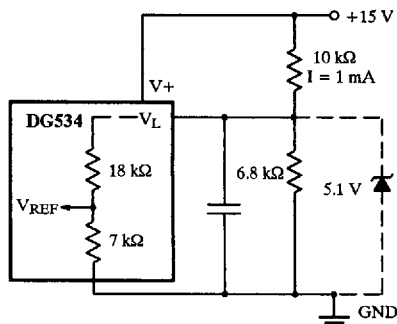


Figure 2. V_L Generated from V_+

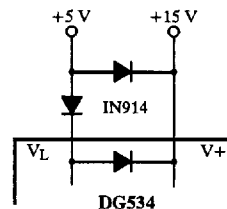


Figure 3. External Diodes Prevent Latchup

Not Recommended for New Designs