Siliconix incorporated

DG548/549

8-Channel and Dual 4-Channel CMOS Analog Multiplexers with Overvoltage Protection

T-51-11

FEATURES

- Analog/Digital Overvoltage Protection
- Fail Safe With Power Loss (No Latchup)
- Break-Before-Make Switching
- TTL and CMOS Compatible Inputs

BENEFITS

- Improved Ruggedness
- Power Loss Protected
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface

APPLICATIONS

- Data Acquisition Systems
- Industrial Process Control
- Avionics Test Equipment
- High Rel Control Systems

DESCRIPTION

The DG548 and DG549 are dielectrically isolated 8- and 4-channel analog multiplexers, respectively, incorporating overvoltage protection. They withstand analog input voltages greater than the supplies. This is advantageous in systems where the analog inputs originate outside the equipment. The DG548/DG549 can withstand continuous inputs up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are lost, while input signals are still present. These multiplexers can withstand brief input transient spikes of several hundred volts which otherwise would require complex external protection networks. Necessarily, ON resistance is higher than the DG508A/DG509A but very low leakage currents combine to produce low errors.

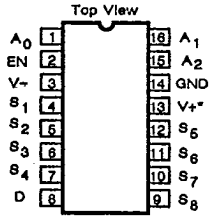
The DG548 and DG549 are pin compatible with the industry-standard DG508A and DG509A multiplexers.

The DG548 and DG549 are offered in 16-pin plastic and CerDIP packages for operation over the commercial, C suffix (0 to 70°C) and military, A suffix (–55 to 125°C) temperature ranges.

5

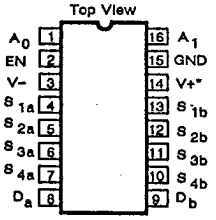
PIN CONFIGURATION

Dual-In-Line Package
Top View



Order Numbers:
DG548AK, DG548BK
DG548CK, DG548CJ

Dual-In-Line Package
Top View



Order Numbers:
DG549AK, DG549BK
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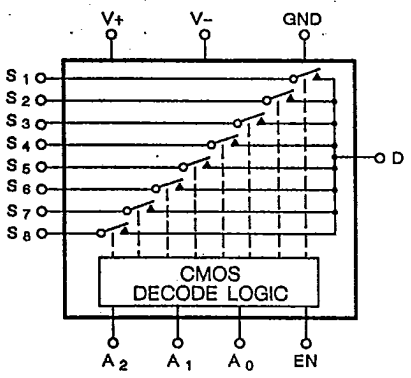
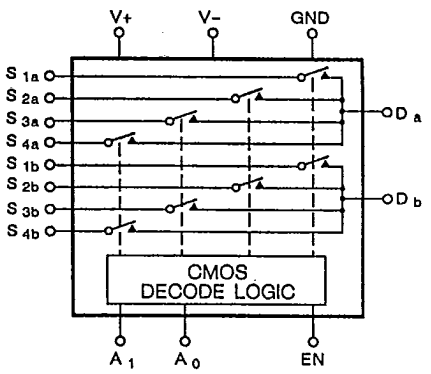
FUNCTIONAL BLOCK DIAGRAM



DG548
8 Channel Single Ended Multiplexer



DG549
Differential 4 Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

V_{EN}, V_A, Digital Input ..... (V-) -4 V to (V+) +4 V

V_S, Analog Input Overvoltage with Power ON ..... (V-) -20 V to (V+) +20 V

V_S, Analog Input Overvoltage with Power OFF ..... -35 V to +35 V

Continuous Current, S or D ..... 20 mA

Peak current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C
(C Suffix) ..... 0 to 70°C

Storage Temperature (A Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C

Power Dissipation (Package)*
16-Pin Ceramic DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 600 mW

* All leads soldered or welded to PC board.
** Derate 12 mW/°C above 75°C.
*** Derate 6.3 mW/°C above 25°C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{AH} = 4.0 V, V_{AL} = 0.8 V	LIMITS 1=25°C 2=125,70°C 3=-55,-0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH									
Analog Signal Range[c]	V_{ANALOG}		1,2,3		-15	15	-15	15	V
ON Resistance[e]	$r_{DS(ON)}$	V_D = ±10 V, I_D = -100 µA	1 2,3	1.2		1.5 1.8		1.8 2.0	kΩ
$r_{DS(ON)}$ Match Between Channels[f]	$\Delta r_{DS(ON)}$	V_S = 0 V, I_D = -100 µA	1	6					%

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DG548/549

T-51-11

ELECTRICAL CHARACTERISTICS [a]

PARAMETER		SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{AH} = 4.0 V, V_{AL} = 0.8 V		LIMITS 1=25°C 2=125,70°C 3=−55,−0°C TEMP	TYP[d]	A SUFFIX −55 to 125°C MIN[b]	A SUFFIX −55 to 125°C MAX[b]	C SUFFIX 0 to 70°C MIN[b]	C SUFFIX 0 to 70°C MAX[b]	UNIT
SWITCH (Cont'd)											
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V, V_D = ∓10 V	1 2,3	0.03	−0.5 −50	0.5 50	−0.5 −50	0.5 50	nA
Drain OFF Leakage Current	DG548	$I_{D(OFF)}$		V_D = ±10 V, V_S = ∓10 V	1 2,3	1	−5 −250	5 250	−5 −250	5 250	
	DG549			V_D = ±10 V, V_S = ∓10 V	1 2,3	0.5	−2.5 −125	2.5 125	−2.5 −125	2.5 125	
$I_{D(OFF)}$ with Input Overvoltage Applied		I_{DOV}	Analog Overvoltage = ±33 V (See Figure 1)		1 2,3	4	−20 −2000	20 2000	−20 −2000	20 2000	
Differential OFF Drain Leakage Current		I_{DIFF}	DG549 Only		1,2,3		−50	50	−50	50	
Drain ON Leakage Current	DG548	$I_{D(ON)}$	V_S = V_D = ± 10 V	Sequence Each Switch ON	1 2,3	0.1	−1 −250	1 250	−1 −250	1 250	
	DG549			V_{AL} = 0.8 V, V_{AH} = 2.4 V	1 2,3	0.05	−0.5 −125	0.5 125	−0.5 −125	0.5 125	
INPUT											
Input LOW Threshold		V_{AL}			1,2,3			0.8		0.8	V
Input HIGH Threshold		V_{AH}			1,2,3		2.4		2.4		
Logic Input Current		I_A	V_A = 2.4 V or 0.8 V		1,2,3		−1	1	−1	1	µA
DYNAMIC											
Access Time		t_A	See Figure 2		1	0.5		1		1	µs
Break-Before-Make Interval		t_{OPEN}	See Figure 3		1	80	25		25		ns
Enable Delay Turn ON Time		$t_{ON(EN)}$	See Figure 4		1 2,3	300		500 1000		500 1000	
Enable Delay Turn OFF Time		$t_{OFF(EN)}$			1 2,3	300		500 1000		500 1000	
Settling Time		t_s	0.1 %		1	1.2					µs
			0.025%		1	3.5					
OFF Isolation			V_{EN} = 7 V, R_L = 1 kΩ, C_L = 3 pF, V_S = 3 V_{RMS}, f = 500 kHz		1	68					dB
Logic Input Capacitance		C_{in}	f = 1 MHZ		1	5					pF

5

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T-51-11

ELECTRICAL CHARACTERISTICS [a]

PARAMETER		SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{AH} = 4.0 V, V_{AL} = 0.8 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		UNIT
				TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC (Cont'd)										
Source OFF Capacitance		$C_{S(OFF)}$		1	6					pF
Drain OFF Capacitance	DG548	$C_{D(OFF)}$		1	25					
	DG549			1	12					
ON State Input Capacitance	DG548	$C_{S(ON)}$		1	30					
	DG549			1	17					
Positive Supply Current		I+	V_{EN}= HIGH or LOW, V_A = 0 V	1,2,3	0.5		2.0		2.0	mA
Negative Supply Current		I-		1,2,3	-0.02	-1		-1		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

SWITCHING TIME TEST CIRCUITS

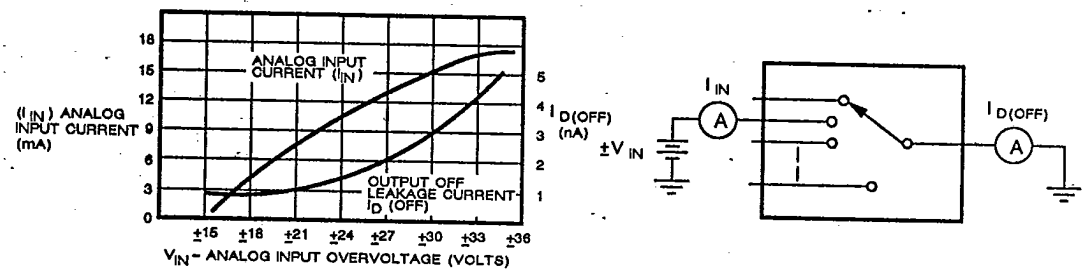

Figure 1. Analog Input Overvoltage Characteristics

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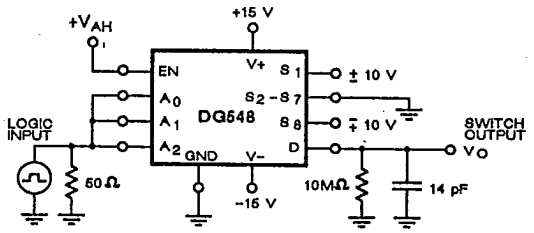
SWITCHING TIME TEST CIRCUITS (Cont'd)



* Similar Connection for DG549

Figure 2. Access Time vs. Logic Level (High)

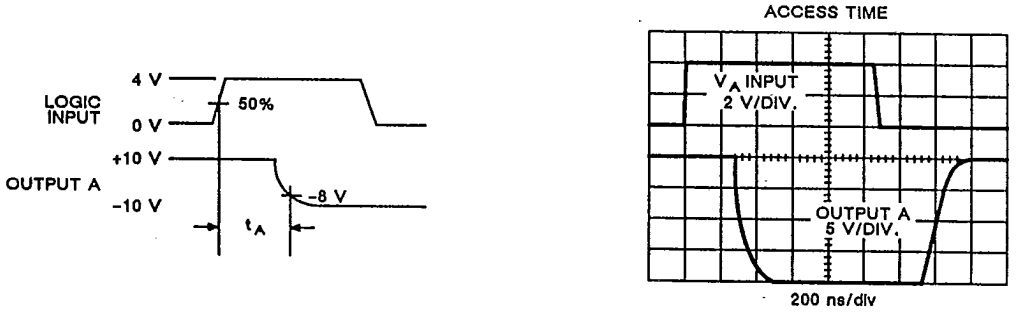
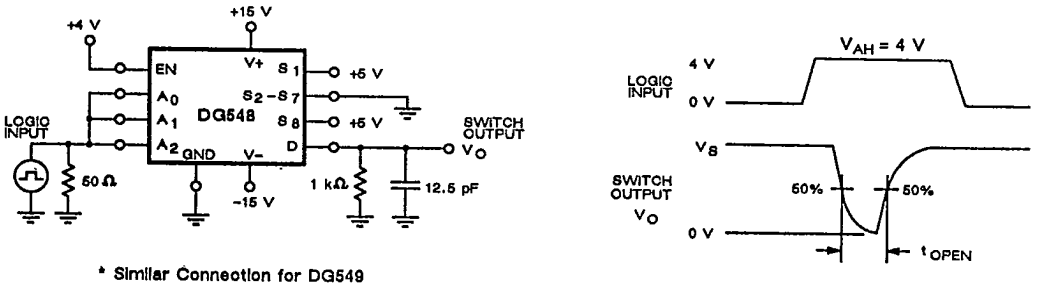


Figure 3. Access Time



* Similar Connection for DG549

Figure 4. Break-Before-Make Delay

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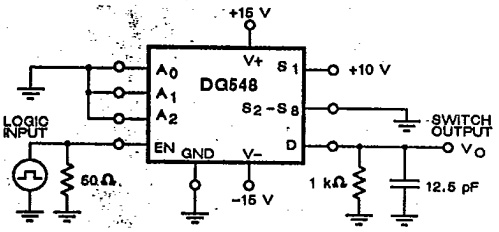
SWITCHING TIME TEST CIRCUITS (Cont'd)

T-51-11



* Similar Connection for DG549

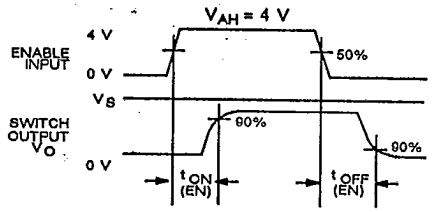


Figure 5. Enable Delay

TRUTH TABLES

DG548

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG549

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ Logic "1" = $V_{AH} \geq 2.4$ V