National Semiconductor Corporation

March 1987

DM10474A/DM10474A-10/DM10474A-8 4096-Bit (1024 x 4) ECL RAM

General Description

The DM10474A/DM10474A-10/DM10474A-8 is a fully decoded 4096-bit, 10KH compatible, ECL read/write random access memory designed for high-speed scratch pad and buffer storage applications. This device is organized as 1024 words by 4 bits and has separate Data In and Data Out pins. On-chip voltage compensation is provided for improved noise margin. The active-low Chip Select and unterminated emitter-follower outputs allow for easy expansion.

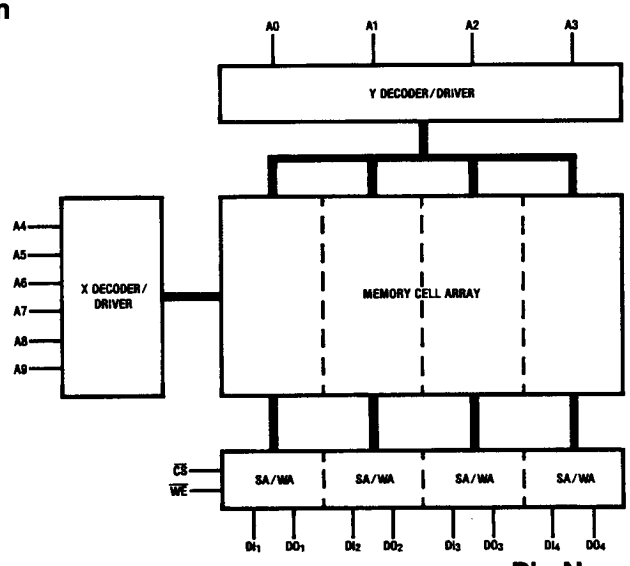
Features

- Three speed selected offerings for maximum cost-performance:

DM10474A	15 ns/−220 mA max
DM10474A-10	10 ns/−240 mA max
DM10474A-8	8 ns/−240 mA max

- 1024 words x 4 bit organization
- 10K and 10 KH logic compatible
- On-chip voltage compensation for improved noise margin
- Oxide isolation process
- Unterminated emitter-follower outputs for easy memory expansion
- Available in DIP and Flat Package
- Pin compatible with HM10474, MBM10474 and F10474

Block Diagram



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Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Pin Names

$\overline{CS}$	Chip Select Input
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Functional Description

Addressing the DM10474A/DM10474A-10/DM10474A-8 is achieved by means of the ten address lines (A0–A9). Each of the 2^{10} possible combinations of address inputs corresponds to a unique word location in memory. The memory array can be expanded by wire-ORing the unterminated emitter-follower outputs of two or more devices and using the active-low Chip Select ($\overline{CS}$) inputs as address lines.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. A 50Ω resistor to −2V (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The $\overline{CS}$ input is internally pulled low so that in cases where no memory expansion is needed, no external connections are required.

The read and write operations are controlled by the state of the active-low Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held low, the data at the Data Inputs (DI1–DI4) is written into the addressed location. $\overline{WE}$ low also disables the output. The termination will then pull the output low. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. The rising edge of $\overline{WE}$ causes data at the addressed location to be transferred to the Data Outputs (DO1–DO4). The Data presented at Data Outputs is non-inverted.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics $V_{EE} = -5.2V$, $R_T = 50\Omega$ to $-2.0V$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Conditions	T_A	Min	Max	Units
V_{OH}	Output Voltage High	$V_{IN} = V_{IH}$ Max or V_{IL} Min	0°C 25°C 75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	$V_{IN} = V_{IH}$ Max or V_{IL} Min	0°C 25°C 75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	$V_{IN} = V_{IH}$ Min or V_{IL} Max	0°C 25°C 75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IH}$ Min or V_{IL} Max	0°C 25°C 75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C 25°C 75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C 25°C 75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	$V_{IN} = V_{IH}$ Max	0°C to 75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	$V_{IN} = V_{IL}$ Min	0°C to 75°C	0.5 −50	170	μA
I_{EE}	Power Supply Current Pin 9 (Note 1)	All Inputs & Outputs Open	0°C to 75°C	(10474-8) −240 (10474-10) −240 (10474-15) −220		mA

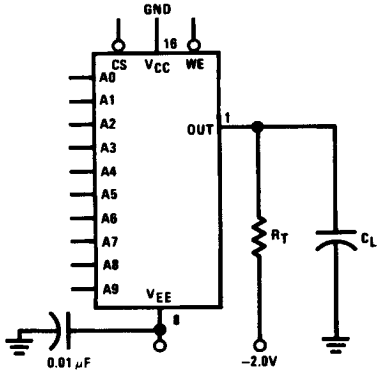
Note 1: Typical values at $T_A = 0°C$, $I_{EE} = -200$ mA; $T_A = 25°C$, $I_{EE} = -190$ mA, $T_A = 75°C$, $I_{EE} = -175$ mA, $V_{EE} = -5.2V$, output load = 50Ω and 30 pF to −2.0V.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, R_T = 50Ω to −2.0V, C_L = 30 pF, T_A = 0°C to +75°C

Test Circuit and Input Waveform

Loading Conditions



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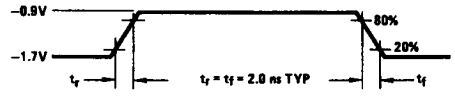
Input Levels



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All timing measurements referenced from 50% of input levels to 50% of input/output levels

C_L = 30 pF including jig and stray capacitance

R_T = 50Ω

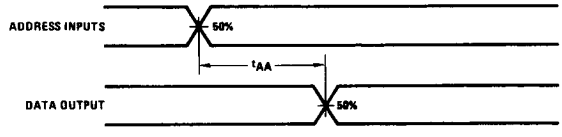
Read Cycle

Symbol	Parameter	Conditions	DM10474A		DM10474A-10		DM10474A-8		Units
			Min	Max	Min	Max	Min	Max	
t_{AA}	Address Access Time	Measured at 50% of Input to 50% of Output (Note 2)		15		10		8	ns
t_{ACS}	Chip Select Access Time			8		6		5	ns
t_{RCS}	Chip Select Recovery Time			8		6		5	ns

Note 2: The maximum address access time is guaranteed to be the worst-case bit in the memory using a pseudorandom testing pattern.

Read Cycle Timing Diagrams

Address Access Time



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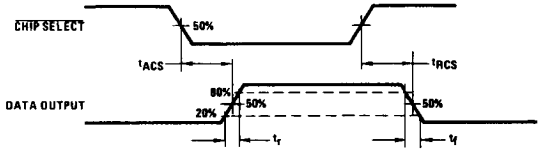
Chip Select Access Time



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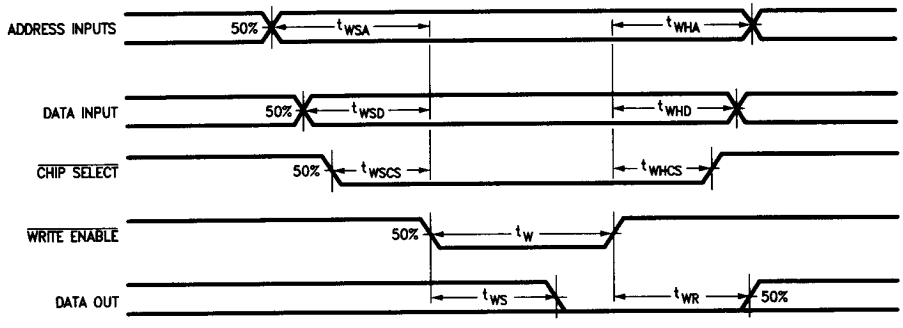
Write Cycle

Symbol	Parameter	DM10474A		DM10474A-10		DM10474A-8		Units
		Min	Max	Min	Max	Min	Max	
t_W	Write Pulse Width	15	—	10	—	6	—	ns
t_{WSD}	Data Set-Up Time Prior To Write	2	—	2	—	1	—	ns
t_{WHD}	Data Hold Time After Write	2	—	2	—	1	—	ns
t_{WSA}	Address Set-Up Time	3	—	3	—	1	—	ns
t_{WHA}	Address Hold Time	2	—	2	—	1	—	ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write	2	—	2	—	1	—	ns
t_{WHCS}	Chip Select Hold Time	2	—	2	—	1	—	ns
t_{WS}	Write Disable Time	—	8	—	8	—	5	ns
t_{WR}	Write Recovery Time	—	8	—	8	—	8	ns

Write Cycle Timing Diagram

Write Mode



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Rise Time and Fall Time

Symbol	Parameter	Conditions	DM10474A/DM10474A-10/DM10474A-8		Units
			Min	Max	
t_r	Output Rise Time	Measured Between 20% and 80% Points	1	3.5	ns
t_f	Output Fall Time		1	3.5	ns

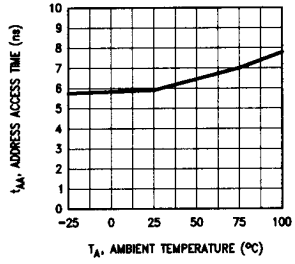
Capacitance

Symbol	Parameter	Conditions	DM10474A/DM10474A-10/DM10474A-8		Units
			Min	Max	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		5	pF
C_{OUT}	Output Pin Capacitance			8	pF

Typical Performance Characteristics

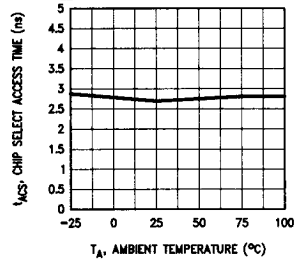
Address Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



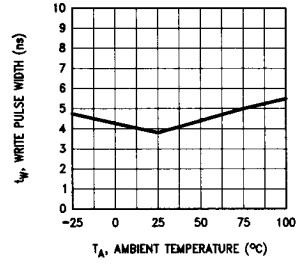
Chip Select Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Write Pulse Width vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



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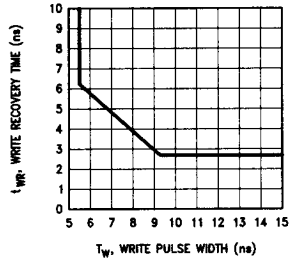
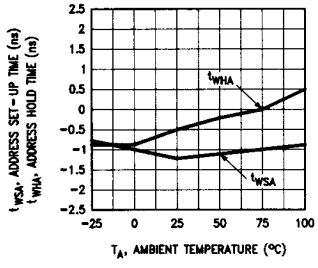
Write Recovery Time vs Write Pulse Width

25°C, NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



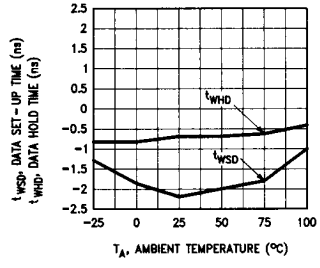
Address Set-Up and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



Data Set-Up and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



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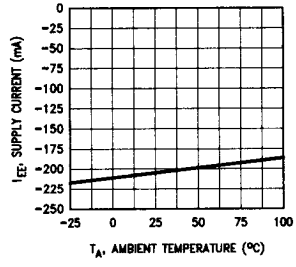
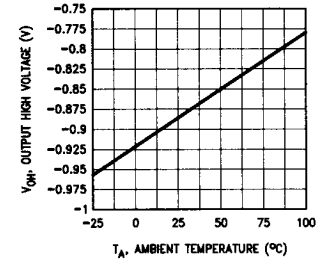
Supply Current (I_{EE}) vs Ambient Temperature

NOMINAL V_{EE}, INPUTS OPEN AND SPECIFIED AIRFLOW



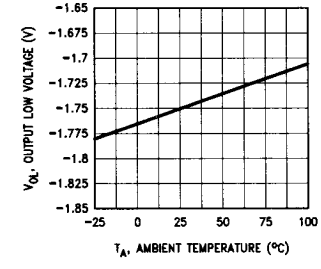
Output High Voltage (V_{OH}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Output Low Voltage (V_{OL}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



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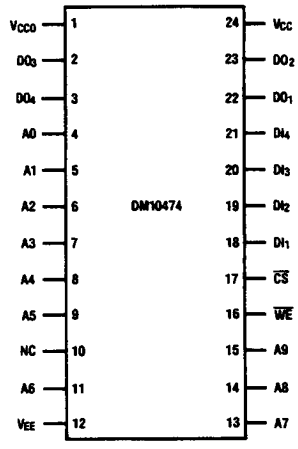
Connection Diagrams

Dual-In-Line Package



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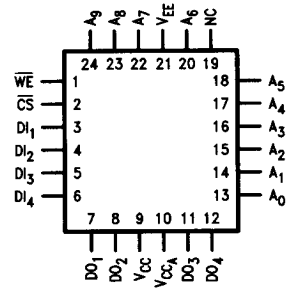
Order Number DM10474AJ, DM10474A-10J or DM10474-8J
See NS Package Number J24E

Flat Pack



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Order Number DM10474AW, DM10474A-10W or DM10474A-8W
See NS Package Number W24B

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