National Semiconductor

DM54S187/DM74S187 1024-Bit (256 × 4) Open-Collector ROM
DM75S97/DM85S97 1024-Bit (256 × 4) TRI-STATE® ROM

general description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

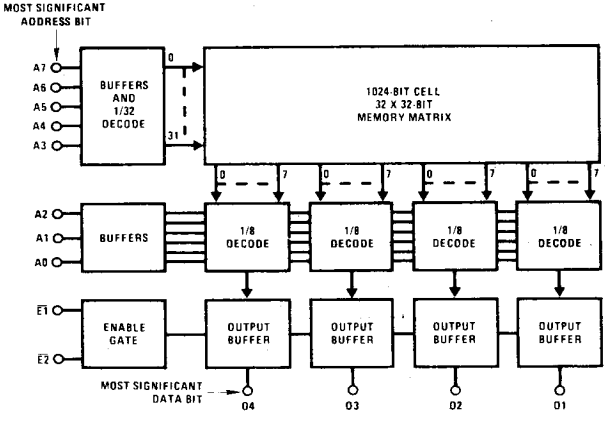
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Schottky-clamped for high speed
  - Address access—50 ns max
  - Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM74S287 and DM74S387

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S187		X	X		N, J
DM85S97		X		X	N, J
DM54S187	X		X		J
DM75S97	X			X	J

block diagram

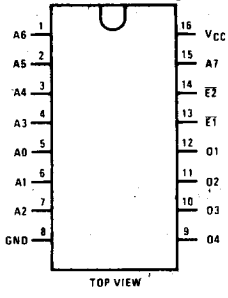


Order Number DM54S187J, DM74S187J, DM75S97J or DM85S97
See NS Package J16A

Order Number DM74S187N or DM85S97N
See NS Package N16A

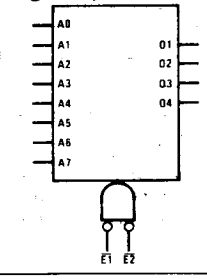
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S187, DM75S97	4.5	5.5	V
DM74S187, DM85S97	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S187, DM75S97	−55	+125	°C
DM74S187, DM85S97	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S187, 75S97			DM74S187, 85S97			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S187, 75S97 5V ±10%; −55°C to +125°C			DM74S187, 85S97 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*	10	35	60	10	35	50	ns
t_{EA}	Enable Access Time	*(Figure 2)*	5	15	30	5	15	25	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*	5	15	30	5	15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

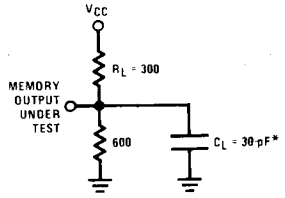
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH} or I_{CEX} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

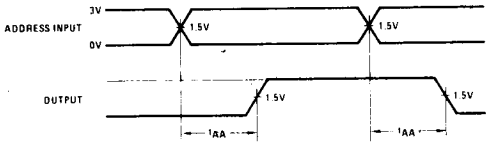


FIGURE 1. Address Access Time

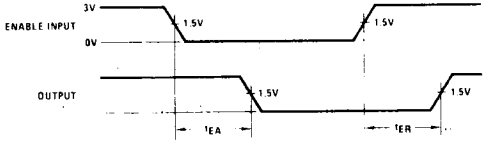
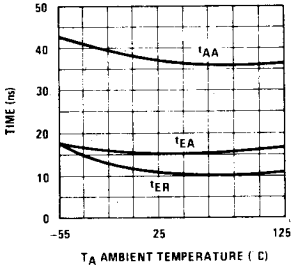


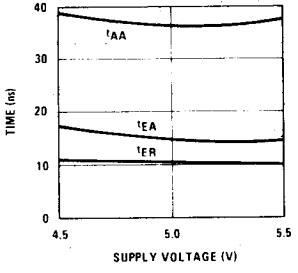
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

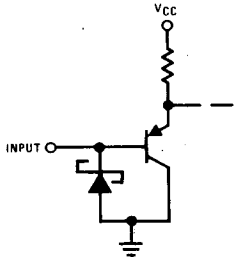


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

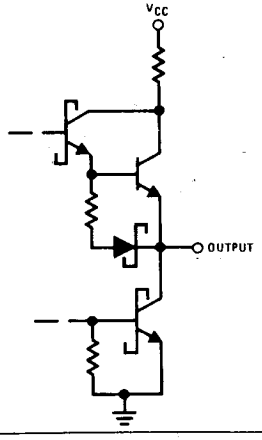


equivalent circuits

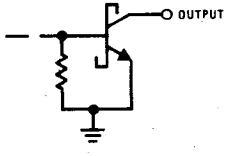
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



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