256K (64K x 4-bit) Static RAM Module — LMM456

FEATURES

- 256K (64K × 4-bit) Static RAM Module
- Advanced CMOS Technology
- High Speed — to 15 ns worst-case
- Low Power Operation
  Active: 900 mW
  Standby: 30 mW typical
- Single 5 V (±10%) Power Supply
- TTL-Compatible Inputs and Outputs
- Plug Compatible with IDT7MP456
- Package Styles Available:
  - 28-pin SIP Module

DESCRIPTION

The LMM456 is a 256K high speed CMOS static RAM module organized as 64K × 4-bits. This module is constructed using four L7C187 64K × 1 static RAMs in plastic surface mount packages assembled on an epoxy laminate SIP substrate.

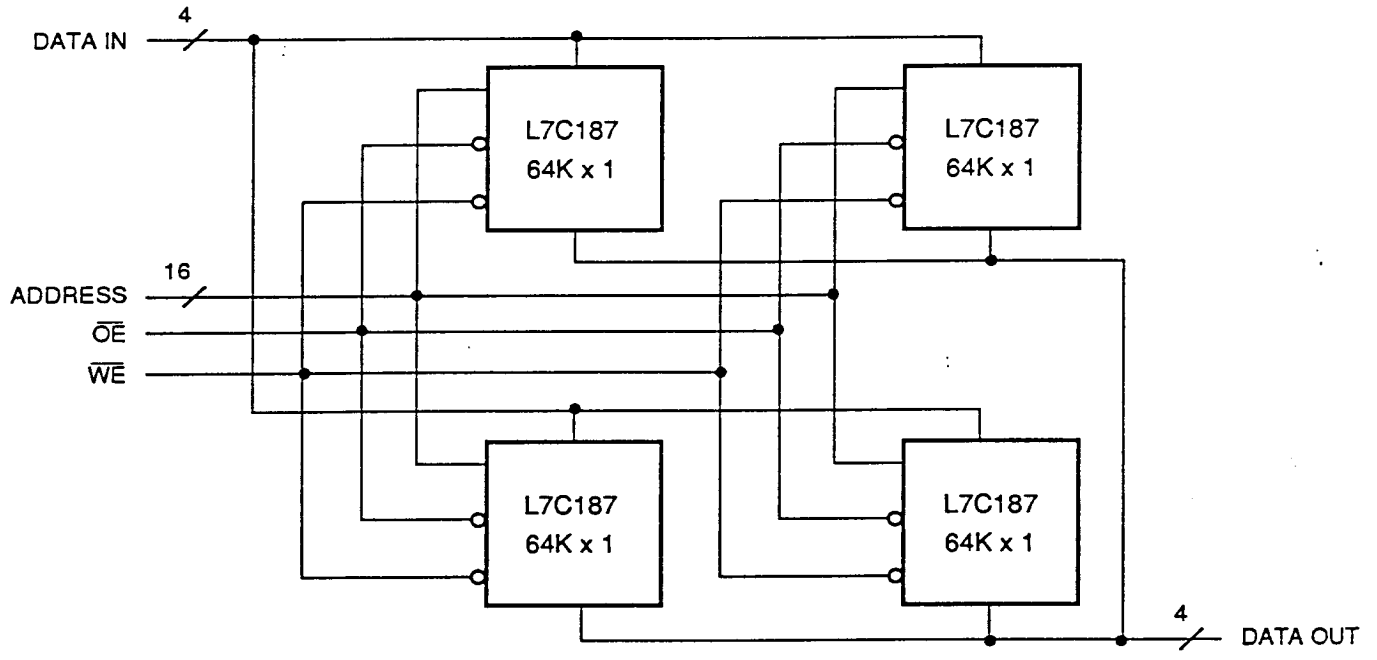
Memory locations are specified on Address pin A0 through A15. Writing to the memory module is accomplished when the active-low Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both low. Either signal may be used to terminate the Write operation.

Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data In/Data Out pins. The input/output pins stay in a high impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

The LMM456 provides asynchronous (unclocked) operation with matching access and cycle times. All inputs and outputs are TTL compatible and operate from a single 5 V power supply.

Latchup and static discharge protection are provided on-chip. The LMM456 can withstand an injection current of up to 200 mA on any pin without damage.

LMM456 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−55°C to +125°C
Operating ambient temperature	0°C to +70°C
Temperature under bias	−10°C to +85°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
DC output current	50 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

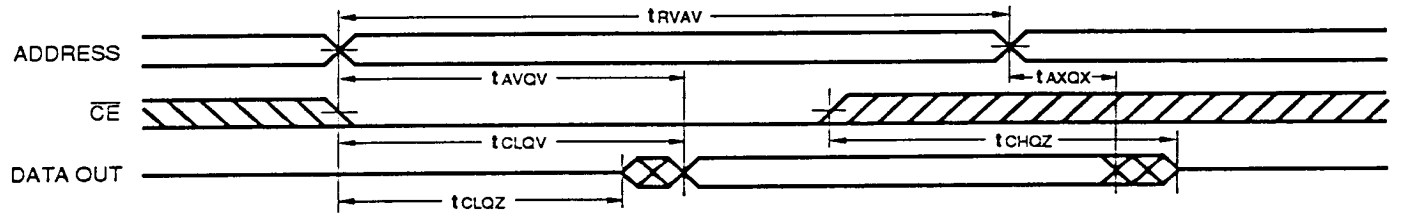
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA, V_{CC} = 4.5 V			0.4	V
V_{IH}	Input High Voltage		2.2		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	−0.5		0.8	V
I_{IX}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = GND to V_{CC}			15	µA
I_{OZ}	Output Leakage Current	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}			15	µA
I_{CC1}	V_{CC} Current, Active	$\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V, Output Open, f = 0		100	165	mA
I_{CC2}	V_{CC} Current, Dynamic	$\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V, Output Open, f = f_{MAX}		240	440	µA
I_{CC3}	V_{CC} Current, Standby	$\overline{CE}$ ≥ V_{IH}, V_{CC} = 5.5 V, Output Open		90	180	µA
I_{CC4}	V_{CC} Current, Full Standby	$\overline{CE}$ ≥ V_{HC}, V_{HC} ≥ V_{IN} or ≤ V_{LC}, V_{CC} = 5.5 V, Out Open		6	60	µA
C_{IN}	Input Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, V_{IN} = 0.0 V			35	pF
C_{OUT}	Output Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, V_{OUT} = 0.0 V			40	pF

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

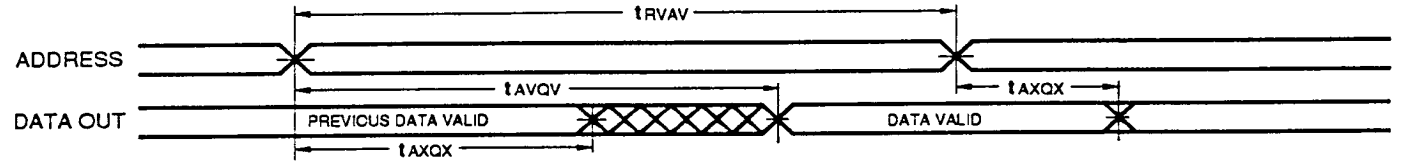
READ CYCLE *(Notes 11, 12, 22, 23, 24)*

Symbol	Parameter	LMM456- 45 Min	45 Max	35 Min	35 Max	30 Min	30 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRVAV	Read Cycle Time	45		35		30		25		20		15	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		30		25		20		15
tAXQX	Address Change to Output Hold	5		5		5		5		5		5	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		30		25		20		15
tCLQZ	Chip Enable Low to Output in Low Z (20, 21)	5		5		5		5		5		5	
tCHQZ	Chip Enable to Output in High Z (20, 21)		35		30		25		20		15		10
tPU	Chip Enable Low to Power Up (10, 19)	0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		30		25		20		20

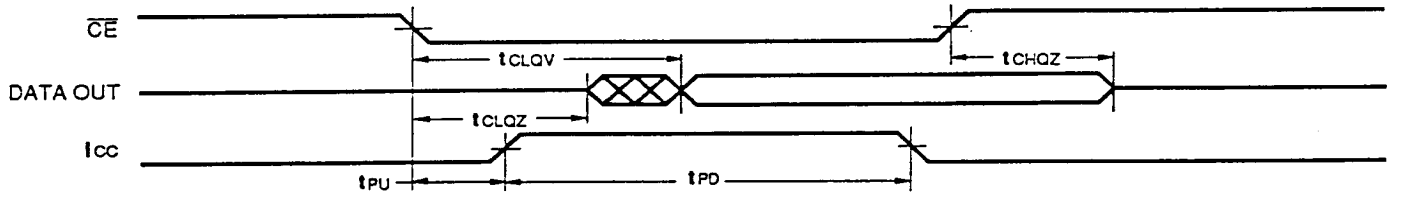
READ CYCLE — ADDRESS CONTROLLED No. 1 *(Notes 13, 14)*



READ CYCLE — ADDRESS CONTROLLED No. 2 *(Notes 13, 15)*



READ CYCLE — CE CONTROLLED *(Notes 13, 15)*

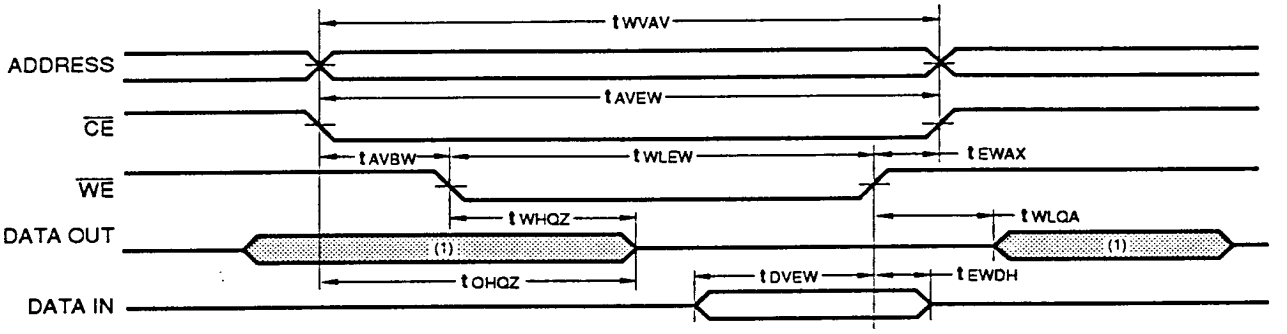


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

Write Cycle (Notes 11, 12, 22, 23, 24)

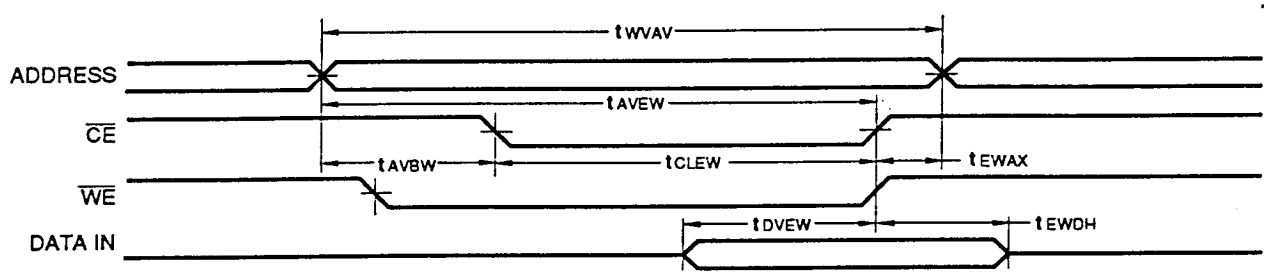
Symbol	Parameter	LMM456- 45 Min	45 Max	35 Min	35 Max	30 Min	30 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tWVAV	Write Cycle Time	45		35		30		25		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	40		30		25		25		25		15	
tAVBW	Address Valid to Beginning of Write Cycle	5		5		5		5		5		5	
tAVEW	Address Valid to End of Write Cycle	40		30		25		25		25		15	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	35		25		20		20		20		15	
tDVEW	Data to End of Write Cycle	25		20		20		15		15		10	
tEWDH	End of Write Cycle to Data Hold	5		5		5		5		5		0	
tWHQZ	Write Enable High to Output in High Z (20, 21)		30		25		20		20		20		15
tWLQA	Write Enable Low to Output Active (20, 21)	0		0		0		0		0		0	

Write Cycle — $\overline{WE}$ Controlled (Notes 16, 17, 18, 19)



(1) During this period, I/O pins are in the output state, and input signals must not be applied.

Write Cycle — $\overline{CE}$ Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE} \le$ VIL, $\overline{WE} \ge$ VIH.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge$ VIH.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.5 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.3 V. For all other inputs VIN ≥ VCC – 0.3 V or VIN ≤ 0.3 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

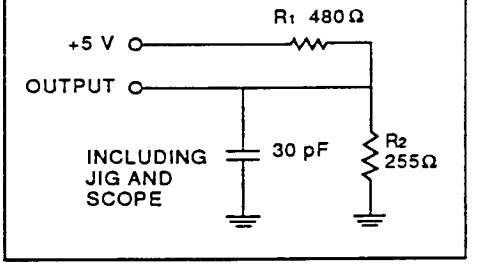


FIGURE 1b.

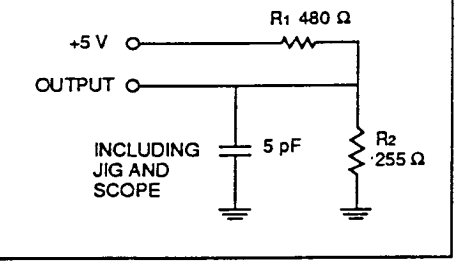
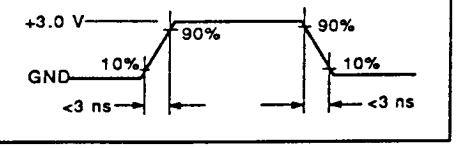
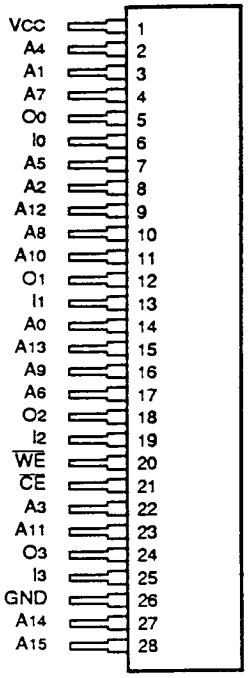


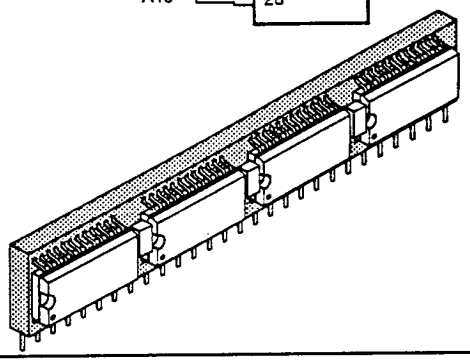
FIGURE 2.



ORDERING INFORMATION

28-pin





Speed	Plastic DIP Surface Mount (S1)
	0°C to +70°C — COMMERCIAL SCREENING
45 ns	LMM456SC45
35 ns	" " 35
30 ns	" " 30
25 ns	" " 25
20 ns	" " 20
15 ns	" " 15