12-bit Cascadable Multiplier-Accumulator LMS12

FEATURES

- 12 × 12-bit Multiplier with Pipelined 26-bit Output Summer
- Summer has 26-bit Input Port Fully Independent from Multiplier Inputs
- Cascadable to Form Video Rate FIR Filter with 3-bit Headroom
- A, B, and C Input Registers Separately Enabled for Maximum Flexibility
- 25 MHz Data Rate for FIR Filtering Applications
- High Speed, Low Power CMOS Technology
- Package Styles Available:
  - 84-pin Plastic LCC J-Lead
  - 84-pin Grid Array

DESCRIPTION

The LMS12 is a high speed 12 × 12-bit combinatorial multiplier integrated with a 26-bit adder in a single 84-pin package. It is an ideal building block for the implementation of very high speed FIR filters for video, RADAR, and other similar applications. The LMS12 implements the general form (A•B) + C. As a result, it is also useful in implementing polynomial approximations to transcendental functions.

Architecture

A block diagram of the LMS12 is shown below. Its major features are discussed individually in the following paragraphs.

Multiplier

The A_{11}–A_0 and B_{11}–B_0 inputs to the LMS12 are captured at the rising edge of the clock in the 12-bit A and B input register, respectively. These registers are independently enabled by the $\overline{ENA}$ and $\overline{ENB}$ inputs. The registered input data are then applied to a 12 × 12-bit multiplier array, which produces a 24-bit result. Both the inputs and outputs of the multiplier are in 2's complement format. The multiplication result forms the input to the 24-bit product register.

Summer

The C_{25}–C_0 inputs to the LMS12 form a 26-bit 2's complement number which is captured in the C register at the rising edge of the clock. The C register is enabled by assertion of the $\overline{ENC}$ input. The summer is a 26-bit adder which operates on the C register data and the (sign extended) contents of the product register to produce a 26-bit sum. This sum is applied to the 26-bit S register.

Output Multiplexer

The FTS input controls a multiplexer which selects the data to be output on the S_{25}–S_0 lines. When FTS is asserted, the summer result is applied directly to the S output port. When FTS is deasserted, the multiplexer selects the S register for output on the S port, effecting a one-cycle delay of the summer result. The S output port can be forced to a high impedance state by driving the $\overline{OE}$ control line high. FTS would be asserted for conventional FIR filter applications, however the insertion of zero-coefficient filter taps may be accomplished by negating FTS. Negating FTS also allows application of the same filter transfer function to two interleaved datastreams with successive input and output sample points occurring on alternate clock cycles.

LMS12 Block Diagram

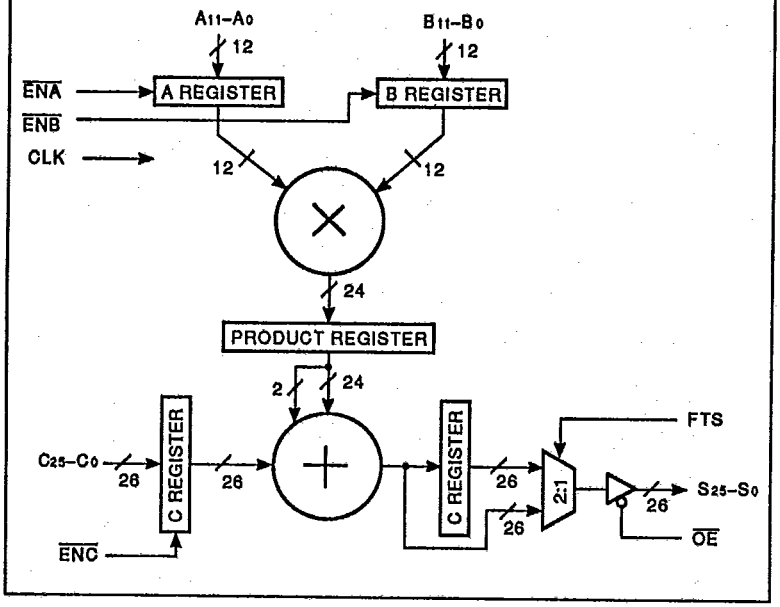

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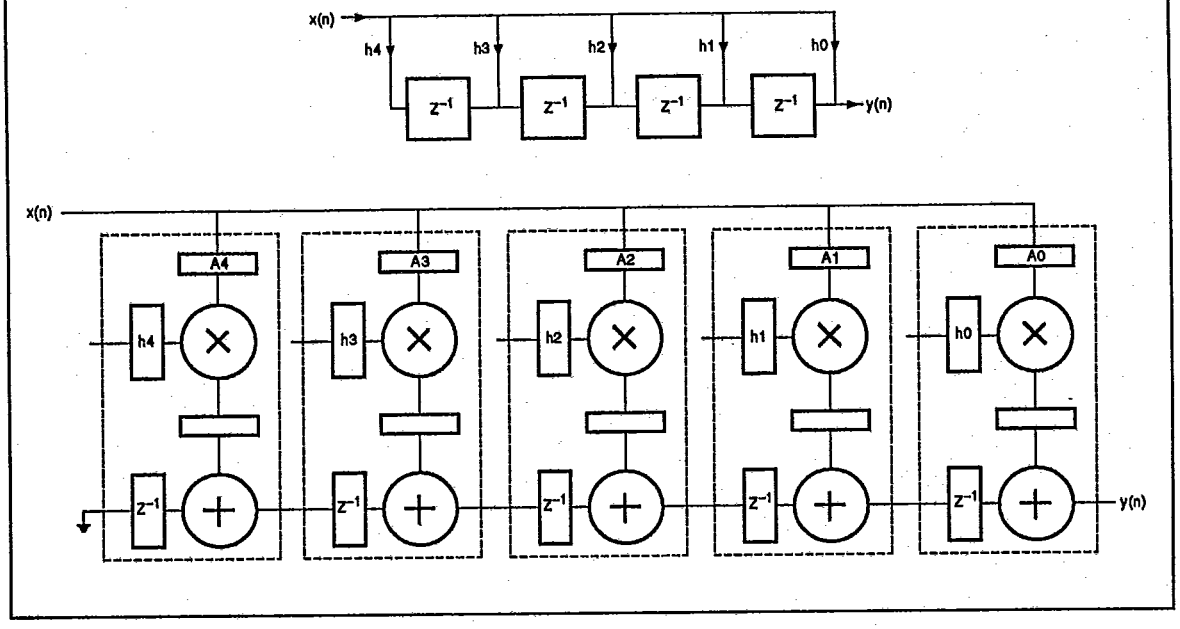
FIGURE 1. FLOW DIAGRAM FOR 5-TAP FIR FILTER.



Applications

The LMS12 is designed specifically for high speed FIR filtering applications requiring a throughput rate of one output sample per clock period. By cascading LMS12 units, the transpose form of the FIR transfer function is implemented directly, with each of the LMS12 units supplying one of the filter weights, and the cascaded summers accumulating the results. The signal flow graph for a 5-tap FIR filter and the equivalent implementation using LMS12's is shown in Fig. 1.

The operation of the 5-tap FIR filter implementation of Fig. 1 is depicted in Table 1. The filter weights h4–h0 are assumed to be latched in the B input registers of the LMS12 units. The x(n) data is applied in parallel to the A input registers of all devices. For descriptive purposes in the table, the A-register contents and Sum output data of each device is labelled according to the index of the weight applied by that device; i.e., S0 is produced by the rightmost device, which has h0 as its filter weight and A0 as its input register contents. Each column represents one clock cycle, with the data passing a particular point in the system illustrated across each row.

TABLE 1. TIMING EXAMPLE FOR 5-TAP NONDECIMATING FIR FILTER.

CLK Cycle	1	2	3	4	5	6	7	8	9
X(n)	X_n	X_{n+1}	X_{n+2}	X_{n+3}	X_{n+4}	X_{n+5}	X_{n+6}	X_{n+7}	X_{n+8}
A_4 Register Sum 4		X_n	X_{n+1} h_4X_n	X_{n+2} h_4X_{n+1}	X_{n+3} h_4X_{n+2}	X_{n+4} h_4X_{n+3}	X_{n+5} h_4X_{n+4}	X_{n+6} h_4X_{n+5}	X_{n+7} h_4X_{n+6}
A_3 Register Sum 3		X_n	X_{n+1} h_3X_n + h_4X_{n-1}	X_{n+2} h_3X_{n+1} + h_4X_n	X_{n+3} h_3X_{n+2} + h_4X_{n+1}	X_{n+4} h_3X_{n+3} + h_4X_{n+2}	X_{n+5} h_3X_{n+4} + h_4X_{n+3}	X_{n+6} h_3X_{n+5} + h_4X_{n+4}	X_{n+7} h_3X_{n+6} + h_4X_{n+5}
A_2 Register Sum 2		X_n	X_{n+1} h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+2} h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+3} h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+4} h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+5} h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}	X_{n+6} h_2X_{n+5} + h_3X_{n+4} + h_4X_{n+3}	X_{n+7} h_2X_{n+6} + h_3X_{n+5} + h_4X_{n+4}
A_1 Register Sum 1		X_n	X_{n+1} h_1X_n + h_2X_{n-1} + h_3X_{n-2} + h_4X_{n-3}	X_{n+2} h_1X_{n+1} + h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+3} h_1X_{n+2} + h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+4} h_1X_{n+3} + h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+5} h_1X_{n+4} + h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+6} h_1X_{n+5} + h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}	X_{n+7} h_1X_{n+6} + h_2X_{n+5} + h_3X_{n+4} + h_4X_{n+3}
A_0 Register Sum 0		X_n	X_{n+1} h_0X_n + h_1X_{n-1} + h_2X_{n-2} + h_3X_{n-3} + h_4X_{n-4}	X_{n+2} h_0X_{n+1} + h_1X_n + h_2X_{n-1} + h_3X_{n-2} + h_4X_{n-3}	X_{n+3} h_0X_{n+2} + h_1X_{n+1} + h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+4} h_0X_{n+3} + h_1X_{n+2} + h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+5} h_0X_{n+4} + h_1X_{n+3} + h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+6} h_0X_{n+5} + h_1X_{n+4} + h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+7} h_0X_{n+6} + h_1X_{n+5} + h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}

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MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, Vcc = Max (Notes 4, 8)			–250	mA
I_{CC1}	Vcc Current, Dynamic	(Notes 5, 6)		15	25	mA
I_{CC2}	Vcc Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

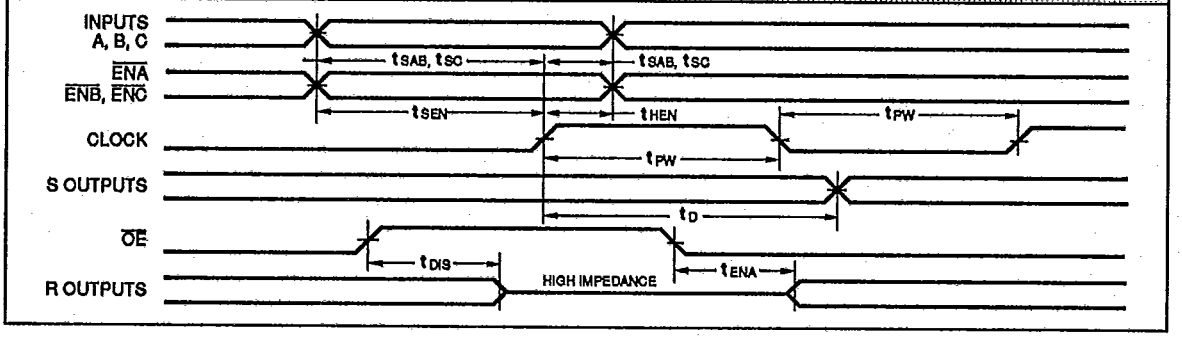
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMS12-65 Min	LMS12-65 Max	LMS12-50 Min	LMS12-50 Max	LMS12-40 Min	LMS12-40 Max
tCP	Clock Period	40		35		30	
tD	Clock to S–FT = 1		50		40		35
	Clock to S–FT = 0		25		25		25
tSC	C Data Setup Time	15		10		7	
tSAB	A, B Data Setup Time	15		12		12	
tSEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12		12	
tHC	C Data Hold Time	5		5		5	
tHAB	A, B Data Hold Time	5		5		5	
tHEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5	
tPW	Clock Pulse Width	15		15		12	
tENA	Output Enable Time (Note 11)		25		25		25
tDIS	Output Disable Time (Note 11)		22		22		22

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMS12-65 Min	LMS12-65 Max	LMS12-50 Min	LMS12-50 Max	Min	Max
tCP	Clock Period	40		35			
tD	Clock to S–FT = 1		50		40		
	Clock to S–FT = 0		25		25		
tSC	C Data Setup Time	15		12			
tSAB	A, B Data Setup Time	15		12			
tSEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12			
tHC	C Data Hold Time	5		5			
tHAB	A, B Data Hold Time	5		5			
tHEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5			
tPW	Clock Pulse Width	15		15			
tENA	Output Enable Time (Note 11)		25		25		
tDIS	Output Disable Time (Note 11)		22		22		

SWITCHING WAVEFORMS



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

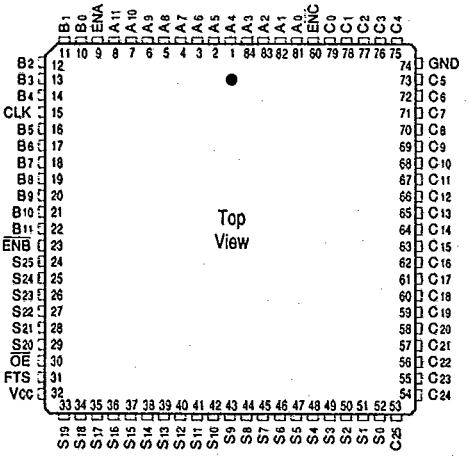
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

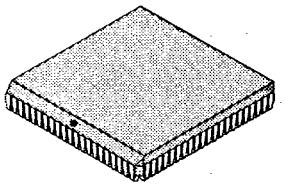
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

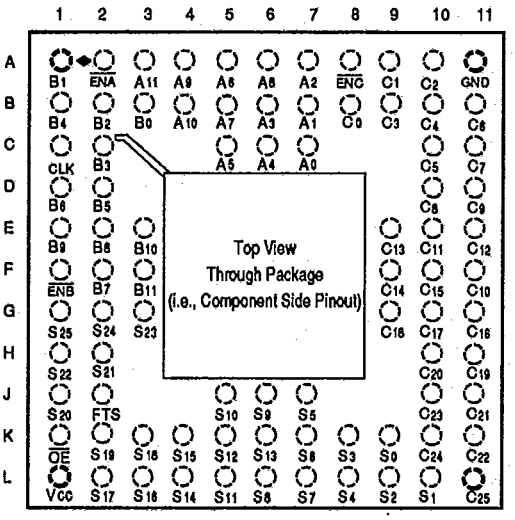
ORDERING INFORMATION

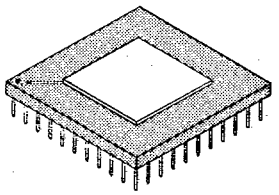
84-pin





84-pin





Speed	Plastic J-Lead Chip Carrier (J3)	Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening	
65 ns	LMS12JC65	LMS12GC65
50 ns	" " 50	" " 50
40 ns	" " 40	" " 40
	–55°C to +125°C — Commercial Screening	
65 ns		LMS12GM65
50 ns		" " 50
	–55°C to +125°C — Extended Screening	
65 ns		LMS12GME65
50 ns		" " 50
	–55°C to +125°C — MIL-STD-883 Compliant	
65 ns		LMS12GMB65
50 ns		" " 50

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