LOGIC DEVICES INCORPORATED

LMU08/8U
8 x 8-bit Parallel Multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- LMU08 Replaces TRW TMC208K
- LMU8U Replaces TRW TMC28KU
- Two's Complement (LMU08), or Unsigned Operands (LMU8U)
- Three-State Outputs
- DECC SMD No. 5962-88739
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

DESCRIPTION

The **LMU08** and **LMU8U** are high-speed, low power 8-bit parallel multipliers. They are pin-for-pin equivalents with TRW TMC208K and TMC28KU type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU08 and the LMU8U produce the 16-bit product of two 8-bit numbers. The LMU08 accepts operands in two's complement format, and produces a two's complement result. The product is provided in two halves with the sign bit replicated as the most significant bit of both halves. This facilitates use of the LMU08 product as a double precision operand in 8-bit systems. The LMU8U operates on unsigned data, producing an unsigned magnitude result.

Both the LMU08 and the LMU8U feature independently controlled registers for both inputs and the product, which along with three-state outputs allows easy interfacing with microprocessor busses. Provision is made in the LMU08 and LMU8U for proper rounding of the product to 8-bit precision. The round input is loaded at the rising edge of the logical OR of CLK A and CLK B for the LMU08. The LMU8U latches RND on the rising edge of CLK A only. In either case, a '1' is added in the most significant position of the lower product byte when RND is asserted. Subsequent truncation of the least significant product byte results in a correctly rounded 8-bit result.

LMU08/8U Block Diagram

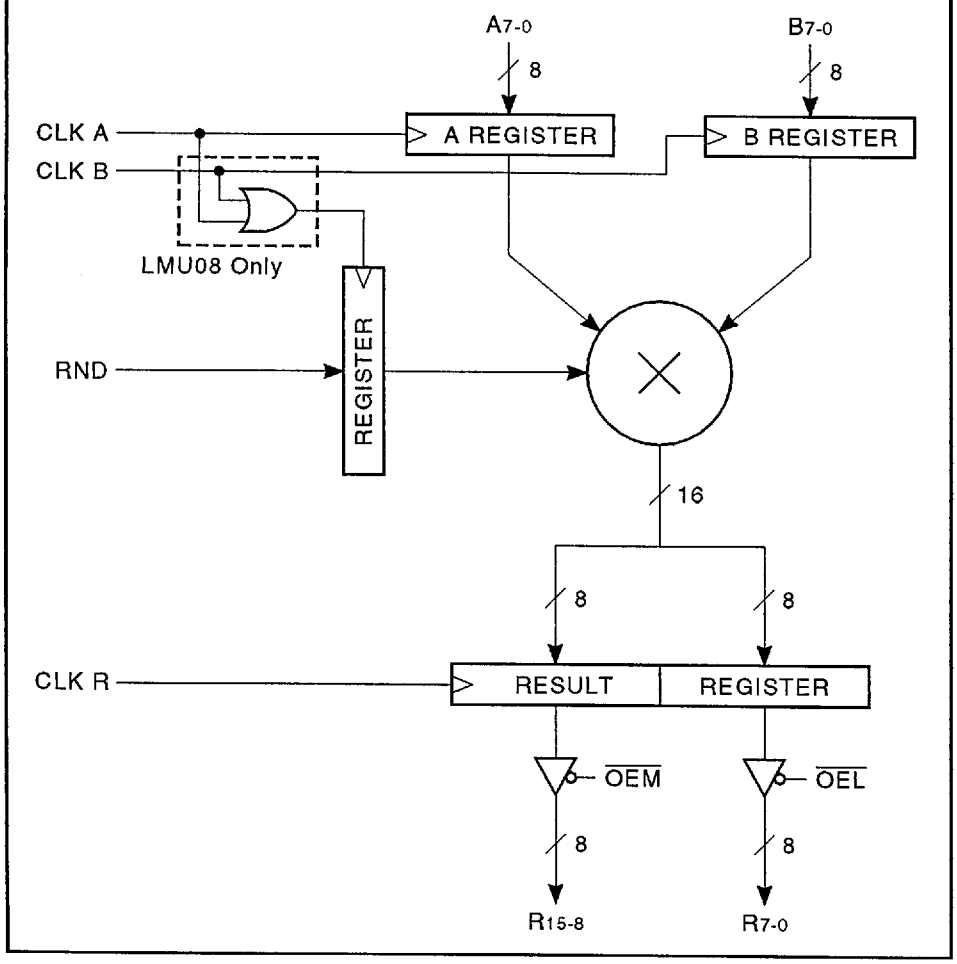


FIGURE 1A. INPUT FORMATS

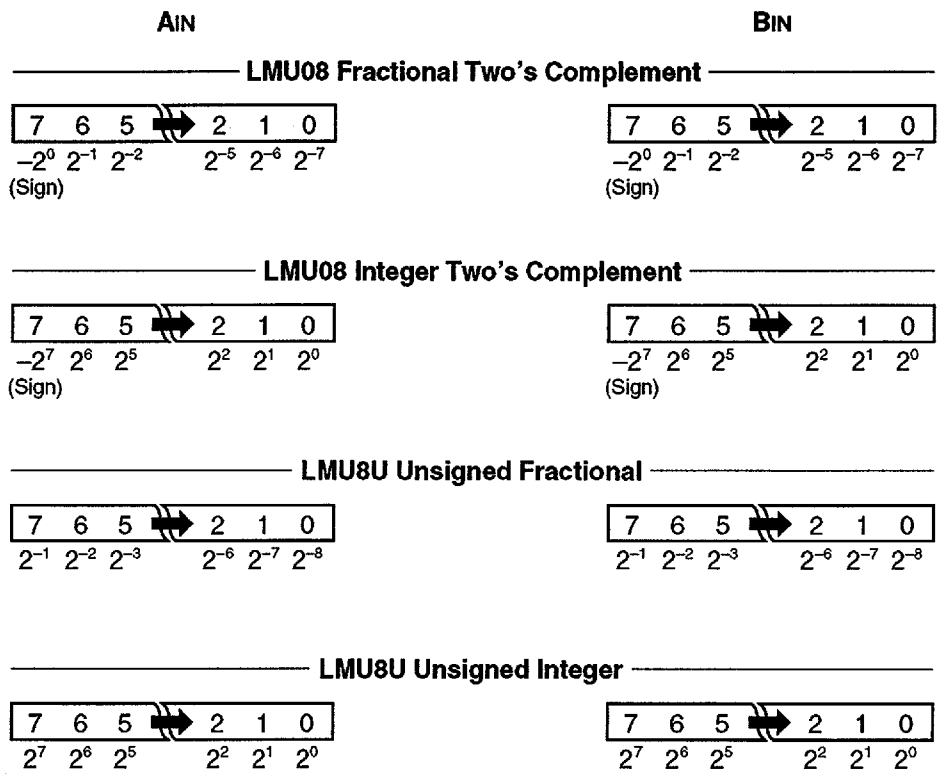
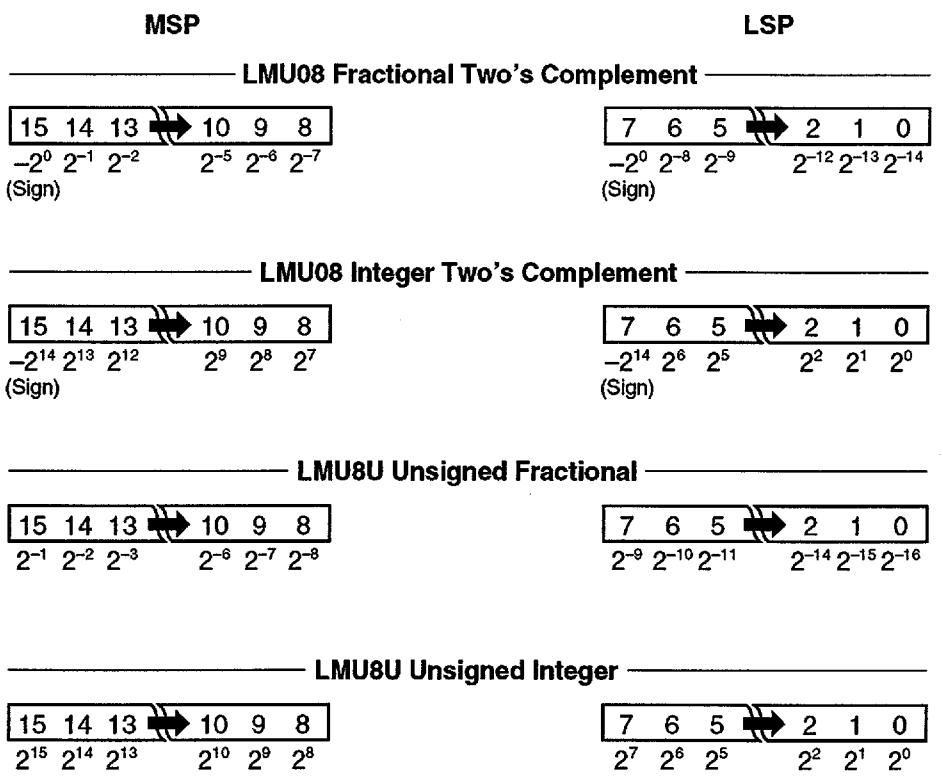


FIGURE 1B. OUTPUT FORMATS



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		8	24	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

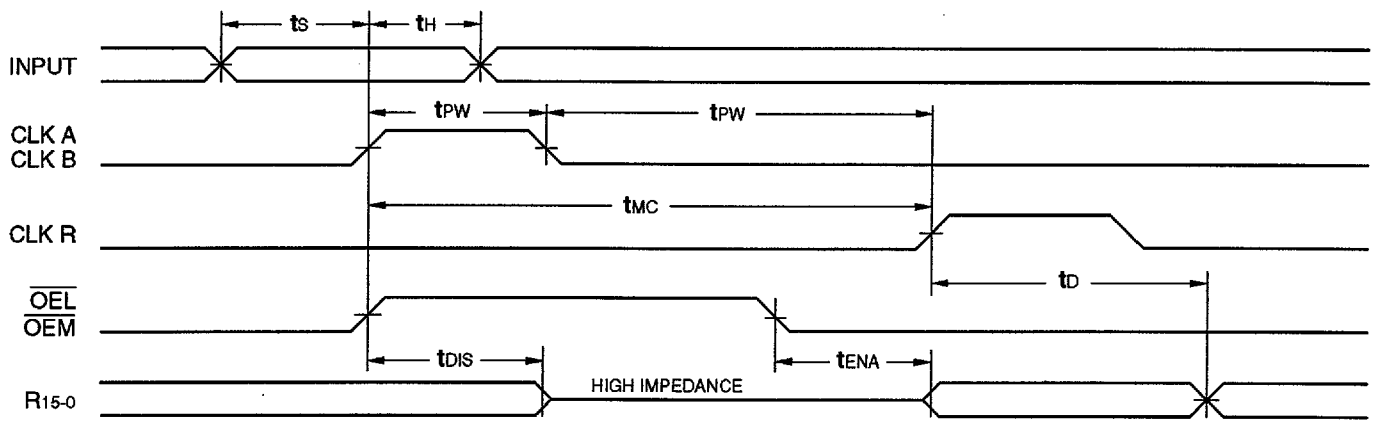
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU08/8U–							
		70		50		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		70		50		35		20
t_{PW}	Clock Pulse Width	20		20		10		8	
t_S	Input Register Setup Time	14		14		14		10	
t_H	Input Register Hold Time	4		0		0		0	
t_D	Output Delay		25		20		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		24		22		22		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		20		20		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU08/8U–							
		90		60		45		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		90		60		45		25
t_{PW}	Clock Pulse Width	25		20		15		10	
t_S	Input Register Setup Time	20		15		15		15	
t_H	Input Register Hold Time	5		2		2		2	
t_D	Output Delay		35		22		22		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		24		24		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		35		22		22		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at -0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

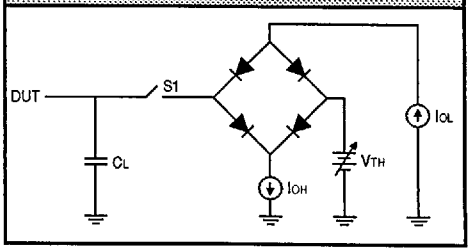
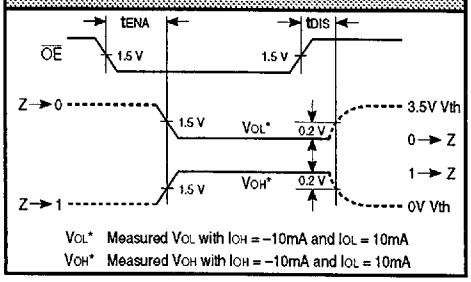
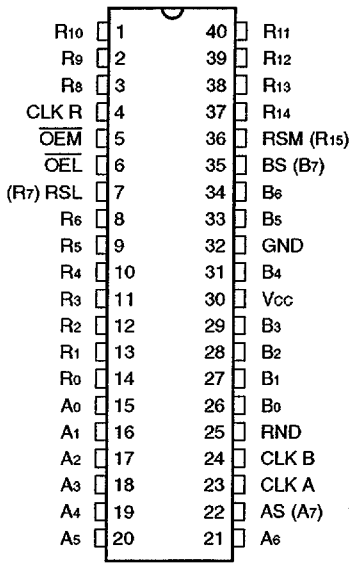


FIGURE B. THRESHOLD LEVELS

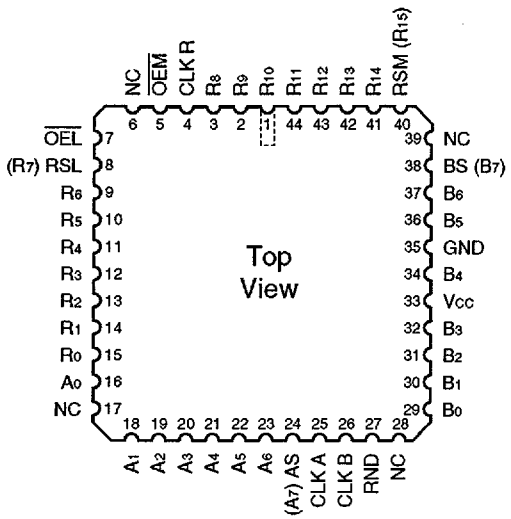


LMU08 — ORDERING INFORMATION

40-pin — 0.6" wide



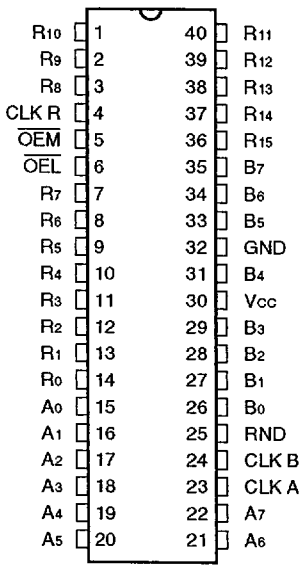
44-pin



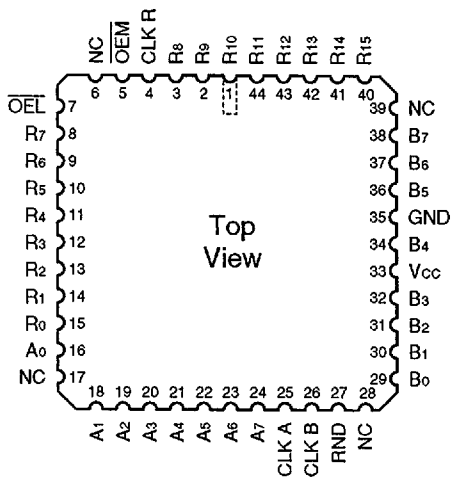
Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
70 ns	LMU08PC70		LMU08JC70	
50 ns	LMU08PC50		LMU08JC50	
35 ns	LMU08PC35		LMU08JC35	
20 ns	LMU08PC20		LMU08JC20	
	–55°C to +125°C — Commercial Screening			
	–55°C to +125°C — MIL-STD-883 Compliant			
90 ns		LMU08CMB90		LMU08KMB90
60 ns		LMU08CMB60		LMU08KMB60
45 ns		LMU08CMB45		LMU08KMB45
25 ns		LMU08CMB25		LMU08KMB25

LMU8U — ORDERING INFORMATION

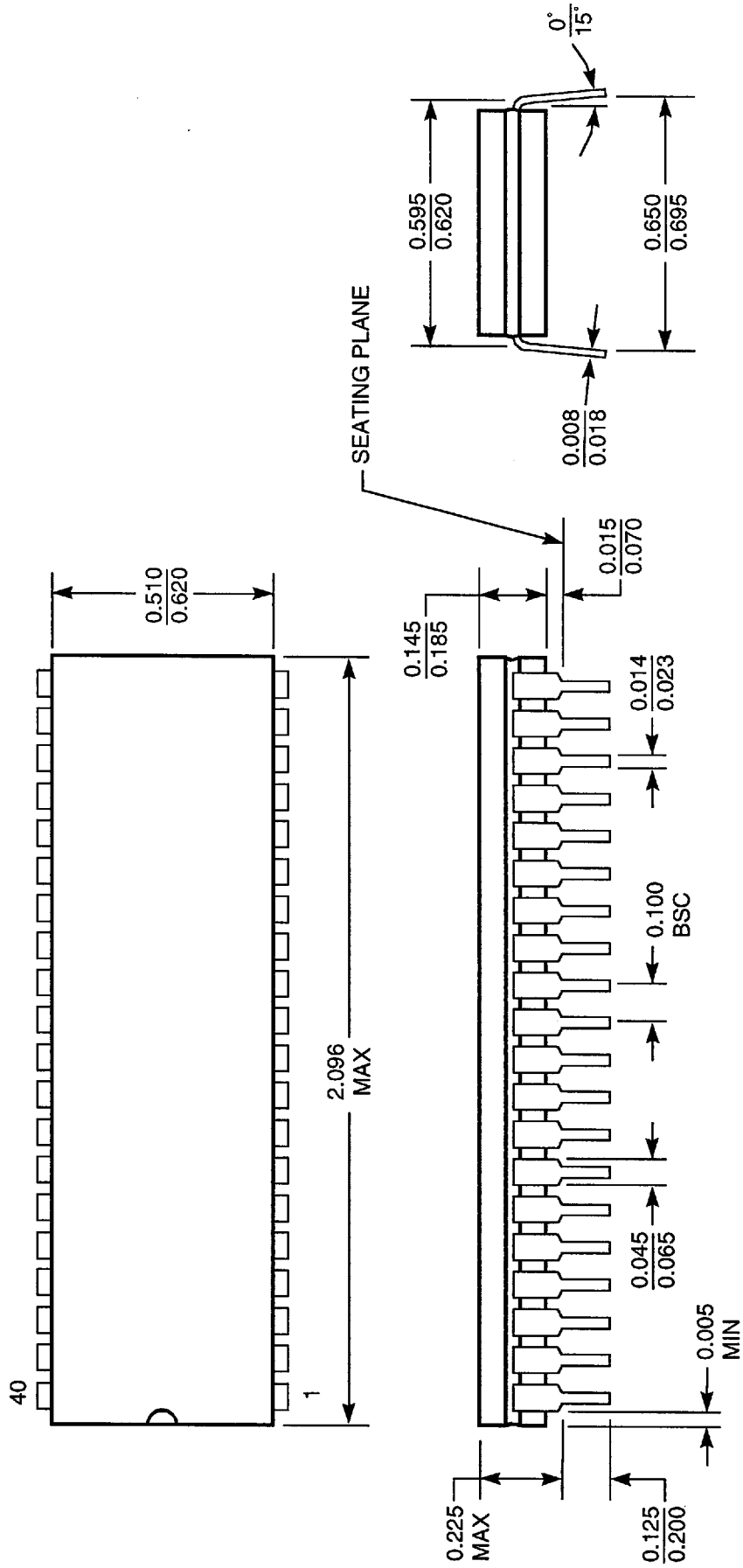
40-pin — 0.6" wide



44-pin



Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
70 ns	LMU8UPC70		LMU8UJC70	
50 ns	LMU8UPC50		LMU8UJC50	
35 ns	LMU8UPC35		LMU8UJC35	
20 ns	LMU8UPC20		LMU8UJC20	
	–55°C to +125°C — Commercial Screening			
	–55°C to +125°C — MIL-STD-883 Compliant			
90 ns		LMU8UCMB90		LMU8UKMB90
60 ns		LMU8UCMB60		LMU8UKMB60
45 ns		LMU8UCMB45		LMU8UKMB45
25 ns		LMU8UCMB25		LMU8UKMB25



LOGIC DEVICES INCORPORATED
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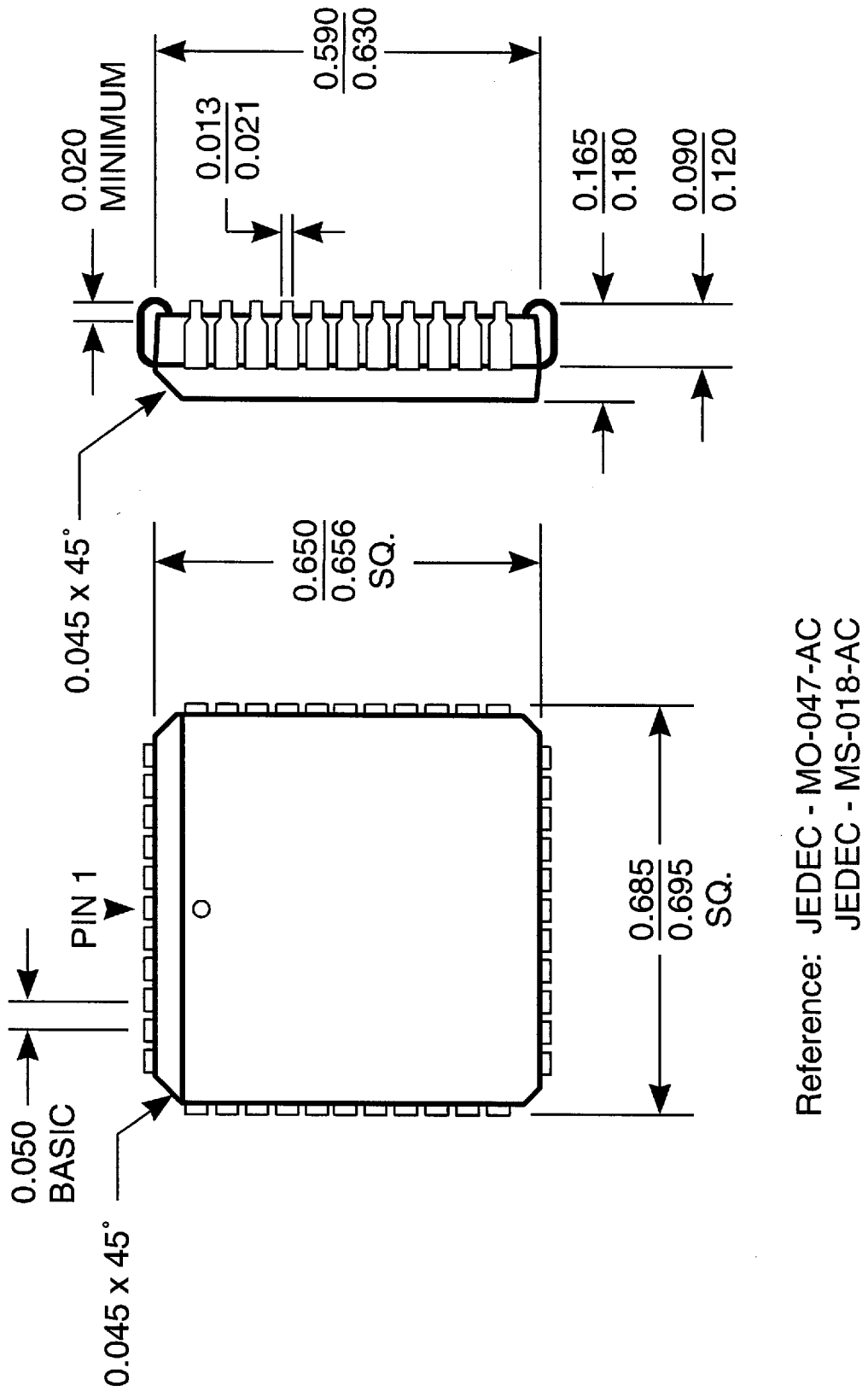
Sunnyvale, CA 94089
(408) 542-5400

TITLE CERAMIC DIP
40-PIN
600 MIL

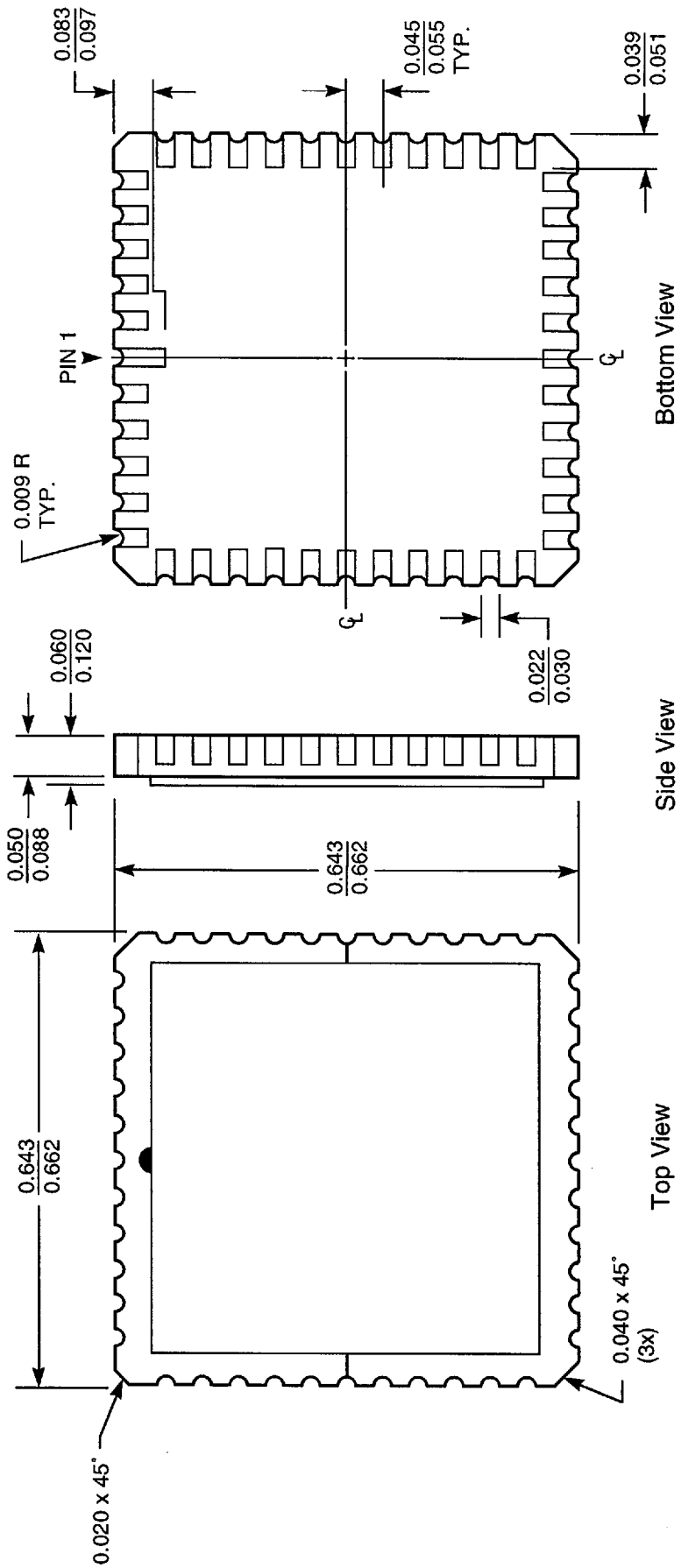
DOCUMENT NUMBER MD-C11 | REV A
DATE 05/06/96 | SHEET 1 OF 1

5565905 0004597 633



LOGIC DEVICES INCORPORATED 1320 Orleans Drive Sunnyvale, CA 94089 (408) 542-5400	TITLE PLASTIC J-LEAD CHIP CARRIER 44-PIN 0.690" x 0.690"	DOCUMENT NUMBER **MD-J1**	REV C
		DATE 01/10/97	SHEET 1 OF 1

5565905 0004632 568



LOGIC DEVICES INCORPORATED 1320 Orleans Drive Sunnyvale, CA 94089 (408) 542-5400	TITLE CERAMIC LEADLESS CHIP CARRIER, 44-PIN 0.650" x 0.650"	DOCUMENT NUMBER MD-K2	REV A
		DATE 05/06/96	SHEET 1 OF 1

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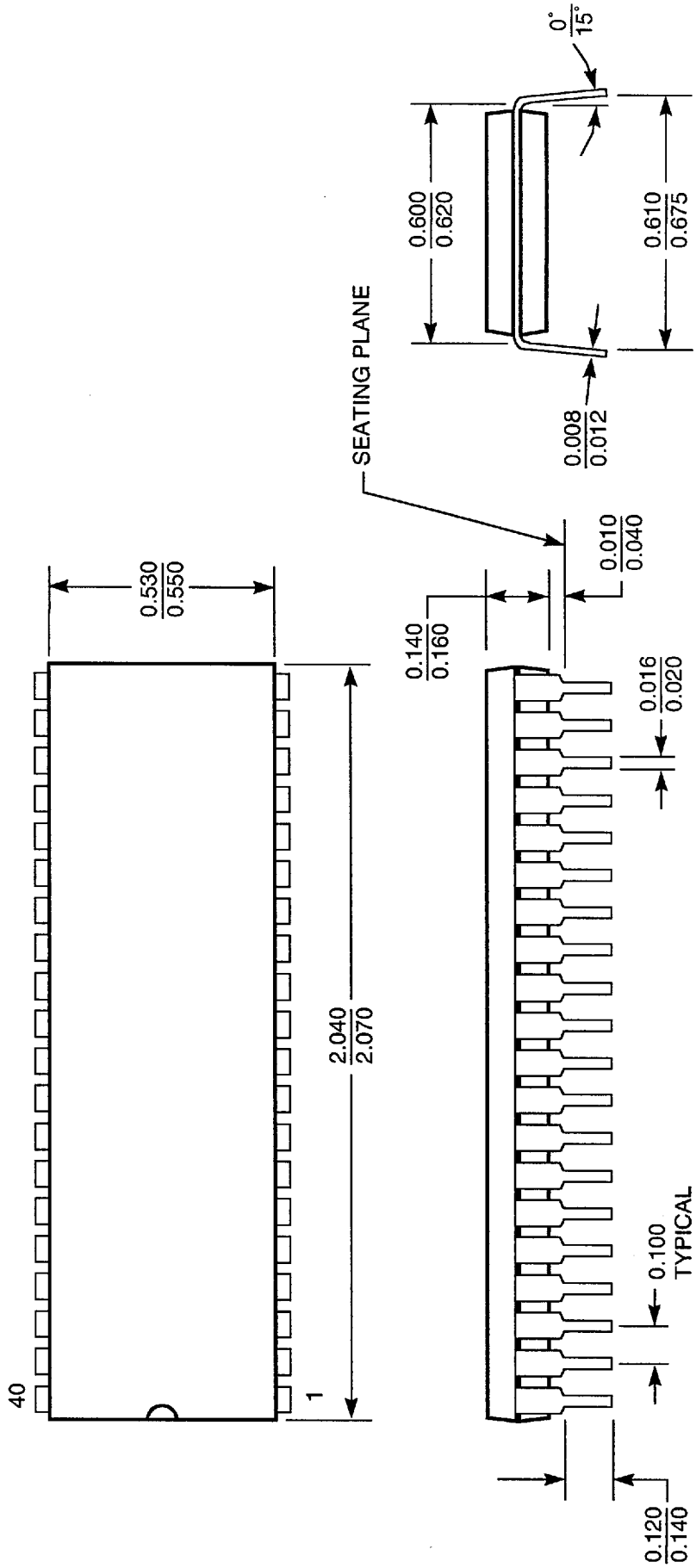

LOGIC DEVICES INCORPORATED 1320 Orleans Drive Sunnyvale, CA 94089 (408) 542-5400	TITLE PLASTIC DIP 40-PIN 600 MIL	DOCUMENT NUMBER MD-P3	REV A
		DATE 05/06/96	SHEET 1 OF 1