LOGIC DEVICES INCORPORATED

LMU12
12 x 12-bit Parallel Multiplier

FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY012H
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA

DESCRIPTION

The LMU12 is a high-speed, low power 12-bit parallel multiplier. It is pin and functionally compatible with TRW MPY012H devices. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU12 produces the 24-bit product of two 12-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B.

The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 23-bit product with a copy of the sign bit inserted in the MSB position of the least significant half. RS HIGH gives a full 24-bit product. Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

LMU12 Block Diagram

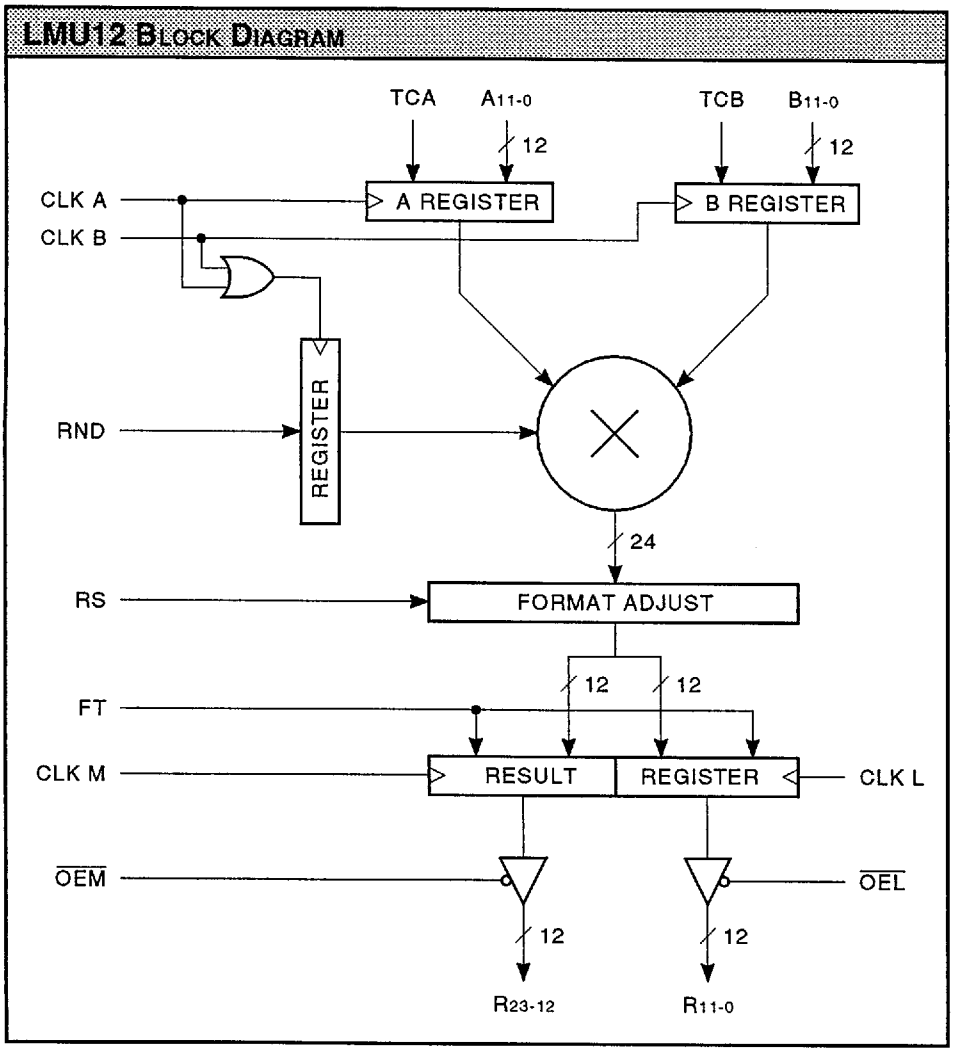


FIGURE 1A. INPUT FORMATS

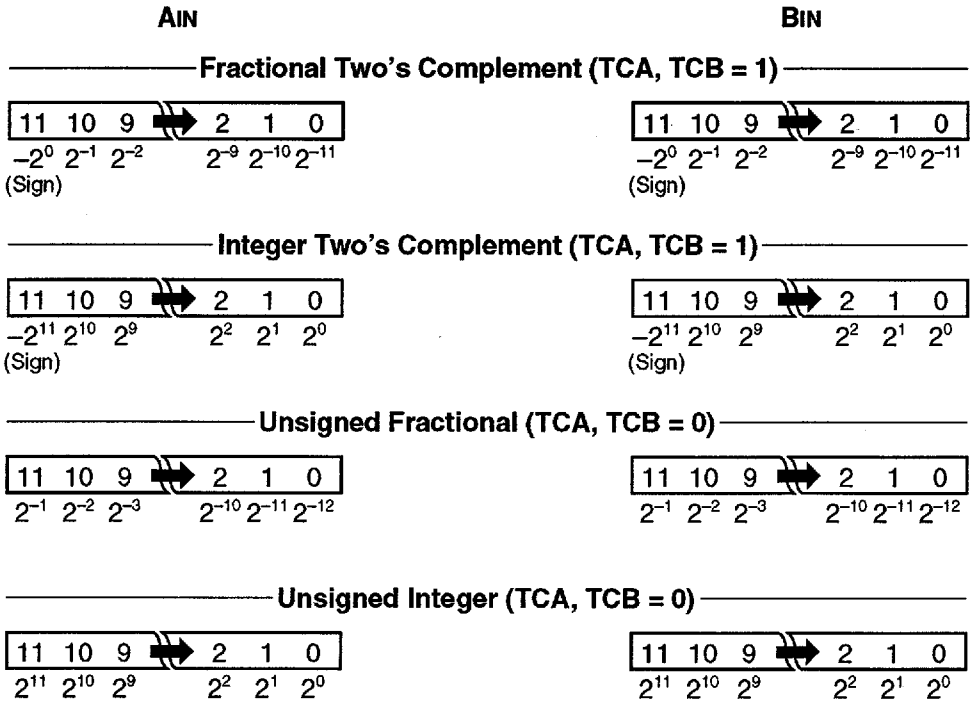
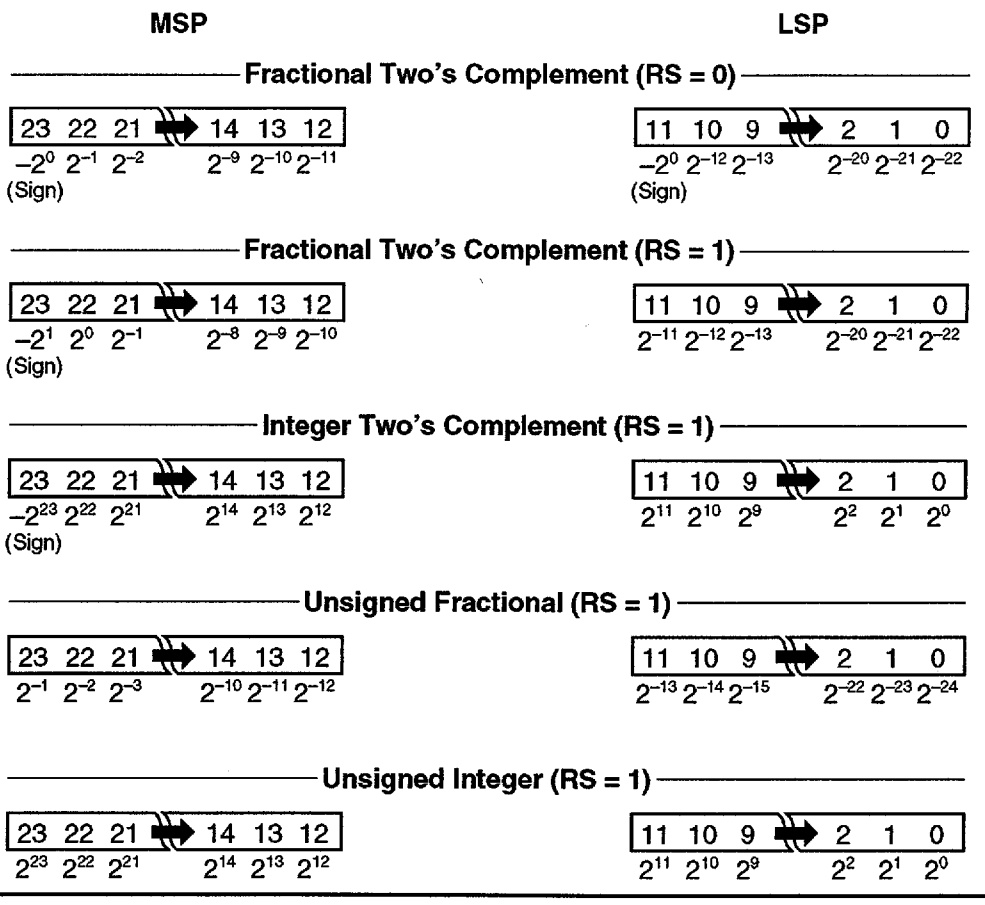


FIGURE 1B. OUTPUT FORMATS



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		17	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

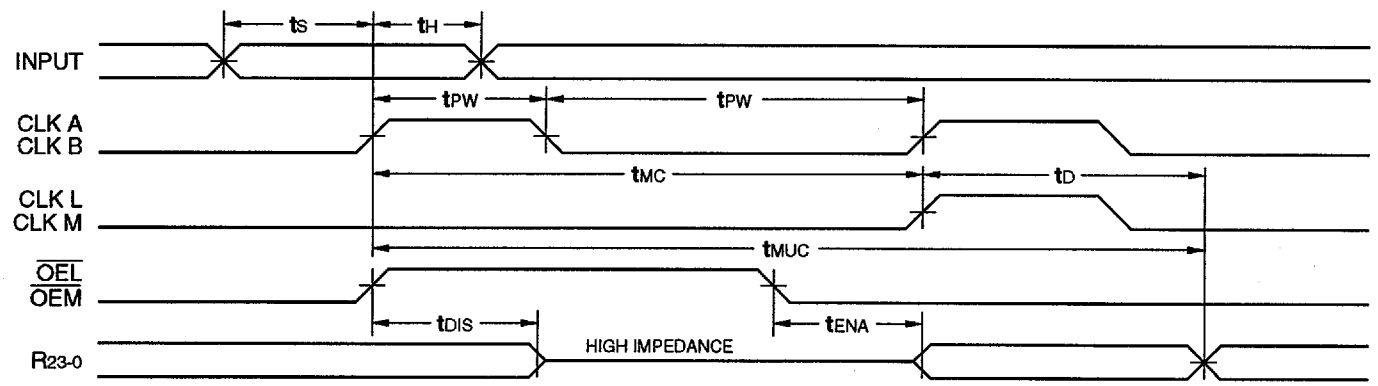
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU12–							
		65		45		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		45		35		20
t_{MUC}	Unclocked Multiply Time		95		65		55		40
t_{PW}	Clock Pulse Width	25		15		15		8	
t_S	Input Register Setup Time	18		15		12		10	
t_H	Input Register Hold Time	2		2		2		0	
t_D	Output Delay		26		25		25		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		22		20		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20		18		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU12–							
		75		55		45		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45		25
t_{MUC}	Unclocked Multiply Time		110		75		65		45
t_{PW}	Clock Pulse Width	25		20		15		10	
t_S	Input Register Setup Time	18		15		15		12	
t_H	Input Register Hold Time	2		2		2		2	
t_D	Output Delay		30		30		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		26		26		24		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		24		22		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

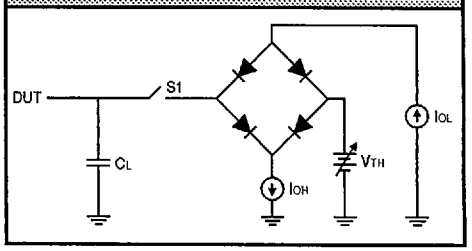
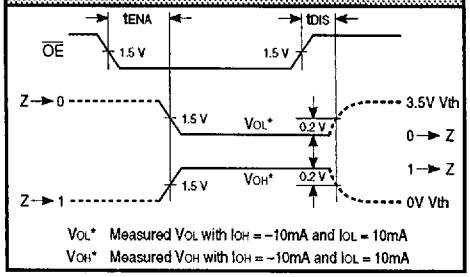
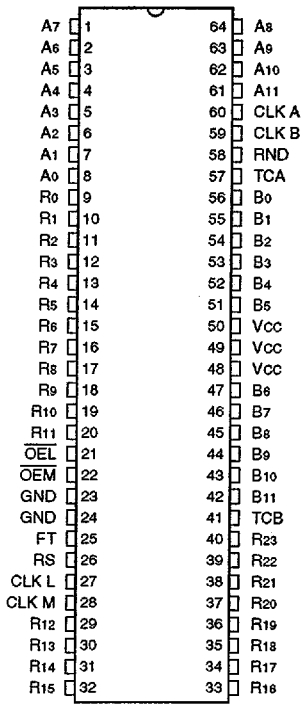


FIGURE B. THRESHOLD LEVELS



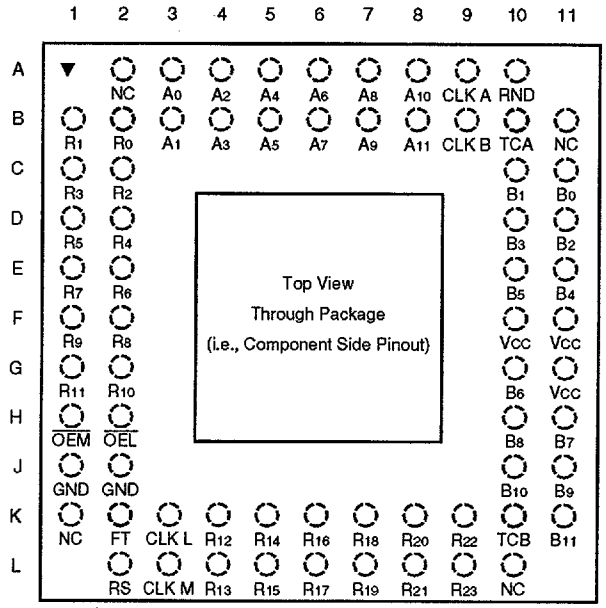
ORDERING INFORMATION

64-pin



*** 64-pin DIP not recommended for new designs**

68-pin



Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening	
65 ns	LMU12DC65	LMU12GC65
45 ns	LMU12DC45	LMU12GC45
35 ns	LMU12DC35	LMU12GC35
20 ns		LMU12GC20
	–55°C to +125°C — Commercial Screening	
75 ns	LMU12DM75	LMU12GM75
55 ns	LMU12DM55	LMU12GM55
45 ns	LMU12DM35	LMU12GM45
25 ns		LMU12GM25
	–55°C to +125°C — MIL-STD-883 Compliant	
75 ns	LMU12DMB75	LMU12GMB75
55 ns	LMU12DMB55	LMU12GMB55
45 ns	LMU12DMB35	LMU12GMB45
25 ns		LMU12GMB25

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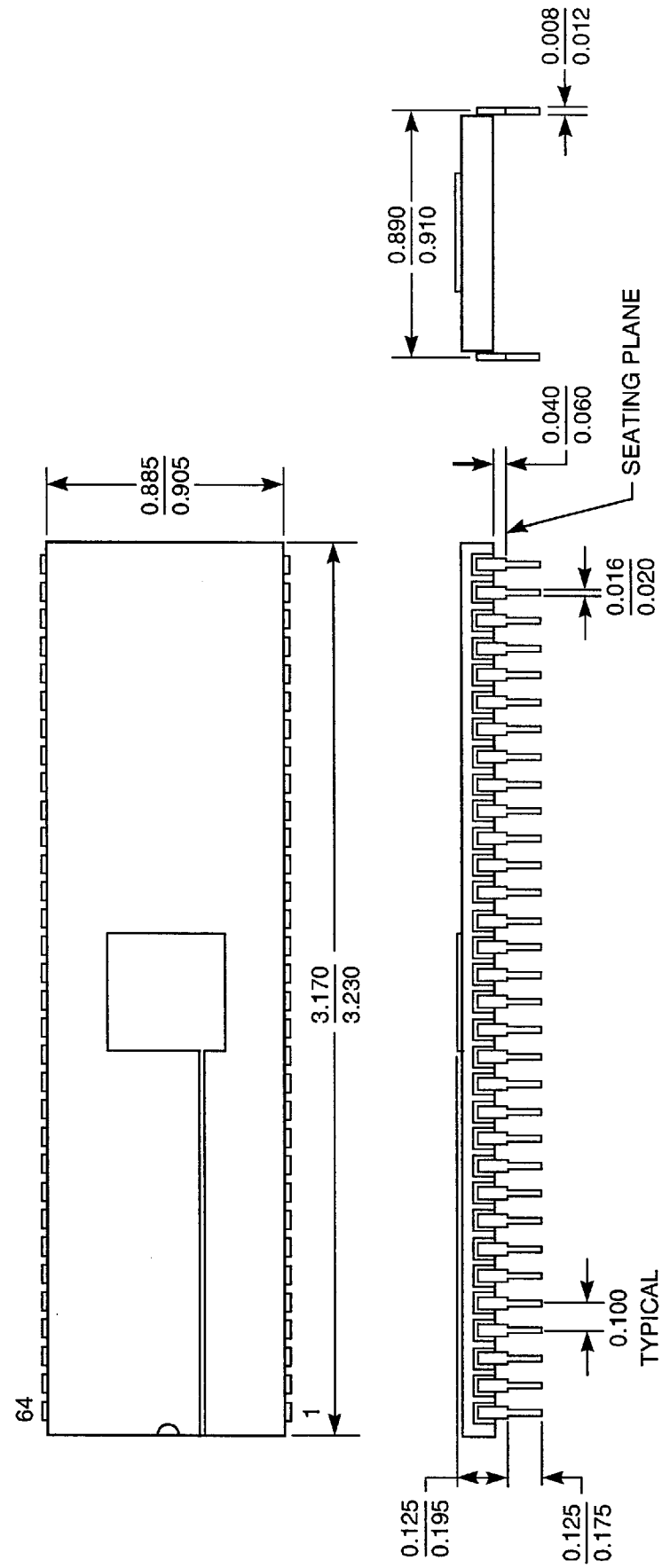
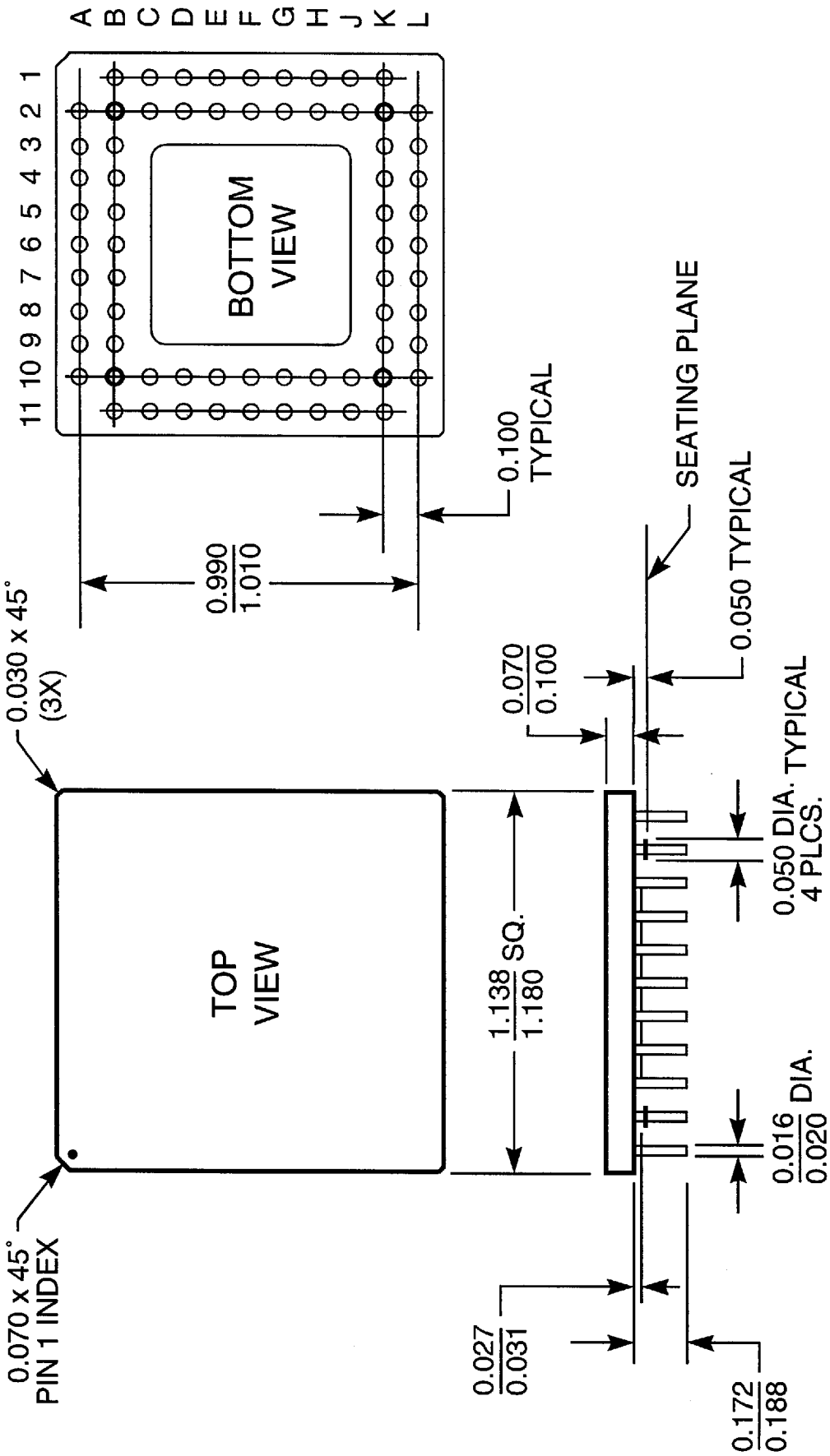


LOGIC DEVICES INCORPORATED 1320 Orleans Drive Sunnyvale, CA 94089 (408)542-5400	TITLE SIDEBRAZE, HERMETIC DIP 64-PIN 900 MIL, CAVITY UP	DOCUMENT NUMBER **MD-D4**	REV A
		DATE 05/06/96	SHEET 1 OF 1

5565905 0004612 77T



LOGIC DEVICES INCORPORATED 1320 Orleans Drive Sunnyvale, CA 94089 (408) 542-5400	TITLE CERAMIC PGA 68-PIN 600 MIL, CAVITY DOWN	DOCUMENT NUMBER MD-G2	REV B
		DATE 05/06/96	SHEET 1 OF 1

5565905 0004627 1T0