16 x 16-bit Parallel Multiplier LMU17/217

FEATURES

- 45 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces AMD Am29517
- Single Clock Architecture with Register Enables
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The LMU17 and LMU217 are 16-bit parallel multipliers with high speed and low power consumption. They are pin and functionally compatible with AMD Am29517 devices. The LMU17 and LMU217 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

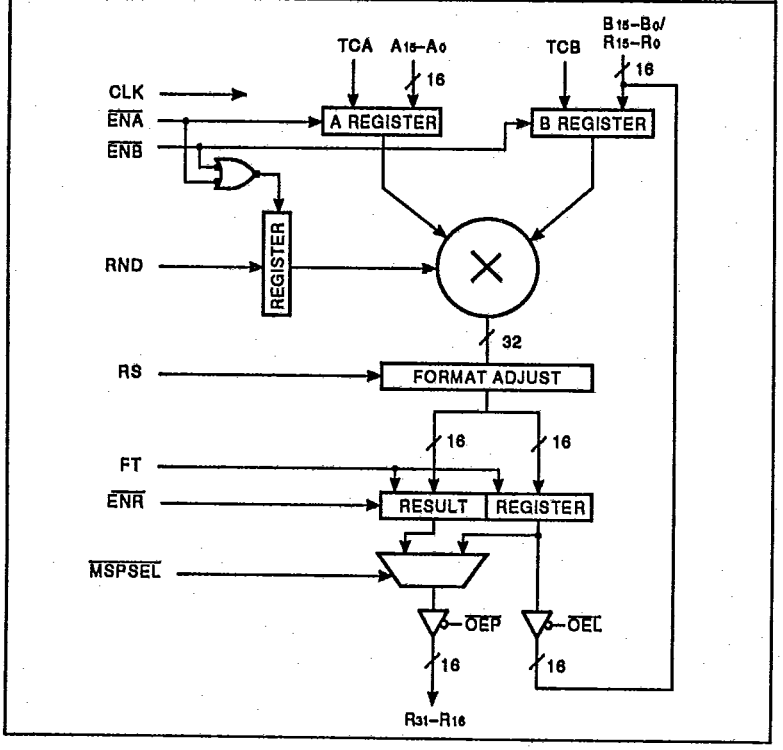
The LMU17 and LMU217 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When high, these prevent application of the clock to the respective register. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are low. RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is high, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ high routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B input port through a separate three-state buffer.

LMU17/217 Block Diagram



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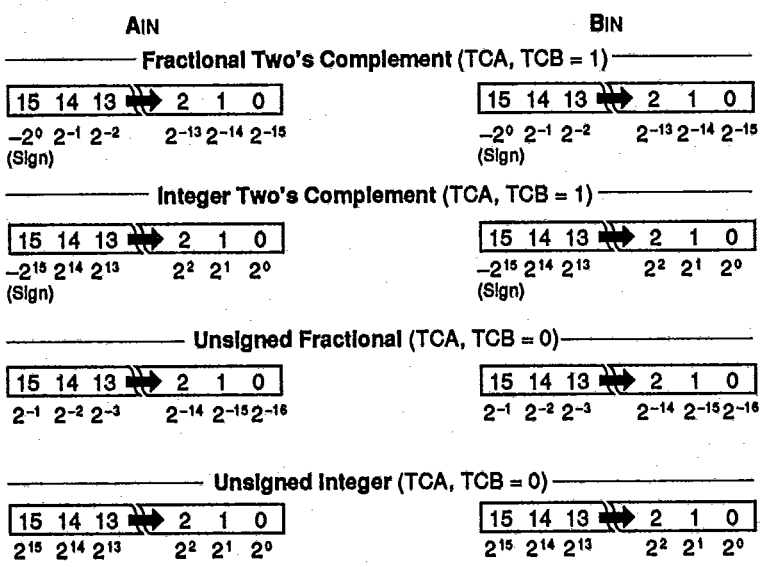
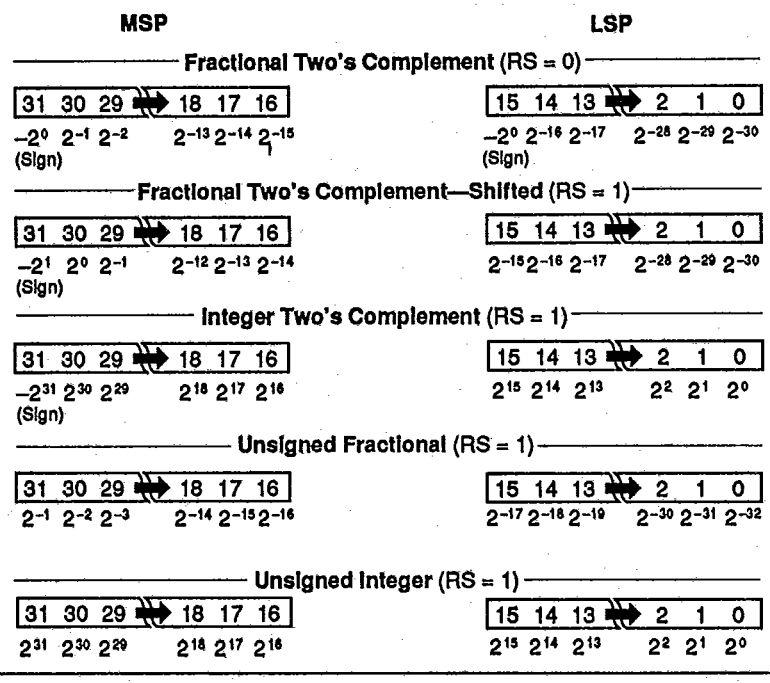
Input Formats



Output Formats



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
Vcc supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, Vcc = Max (Notes 4, 8)			–250	mA
I_{CC1}	Vcc Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	Vcc Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

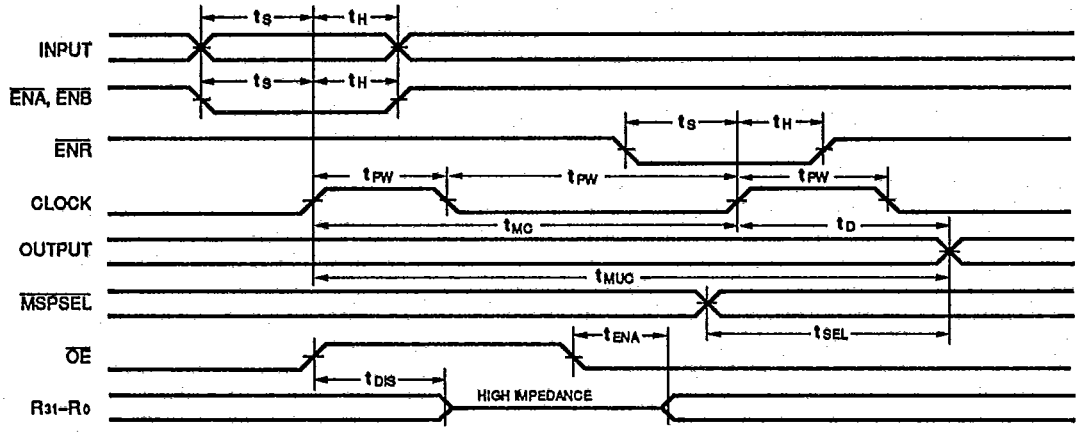
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU17/217- 65 Min	65 Max	55 Min	55 Max	45 Min	45 Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	3		3		3	
t_S	Input Register Setup Time	15		15		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU17/217- 75 Min	75 Max	65 Min	65 Max	55 Min	55 Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	3		3		3	
t_S	Input Register Setup Time	15		15		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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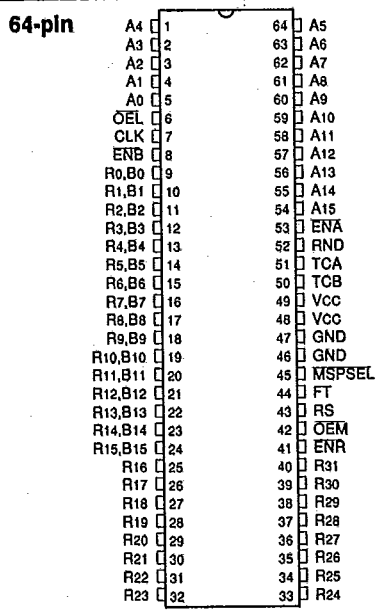
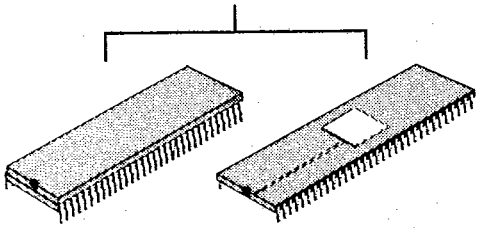
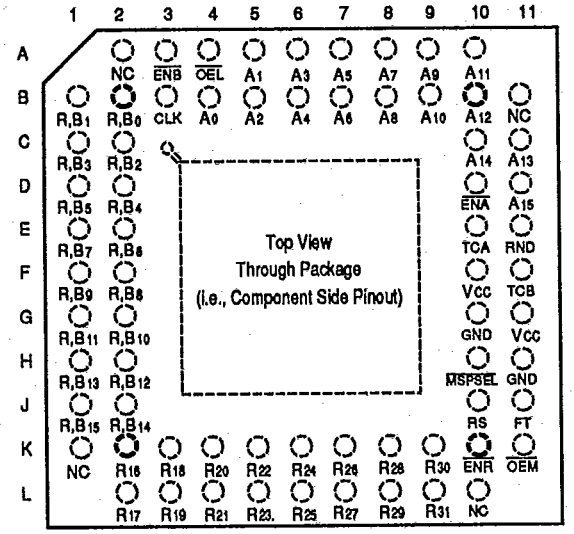
LMU17 — ORDERING INFORMATION

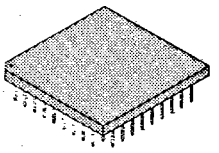
64-pin





68-pin

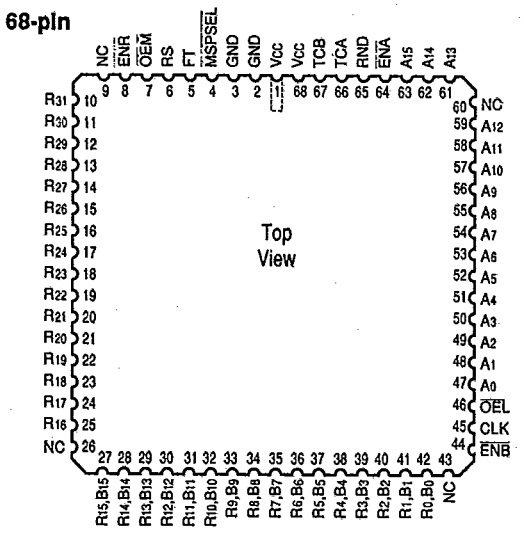


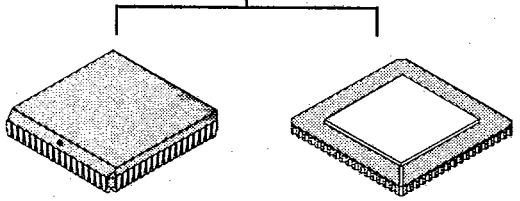


Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening		
65 ns	LMU17PC65	LMU17DC65	LMU17GC65
55 ns	" " 55	" " 55	" " 55
45 ns	" " 45	" " 45	" " 45
	–55°C to +125°C — Commercial Screening		
75 ns		LMU17DM75	LMU17GM75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — Extended Screening		
75 ns		LMU17DME75	LMU17GME75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — MIL-STD-883 Compliant		
75 ns		LMU17DMB75	LMU17GMB75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55

LMU217 — ORDERING INFORMATION

68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — Commercial Screening			
65 ns 55 ns 45 ns	LMU217JC65 ▪ ▪ 55 ▪ ▪ 45	LMU217KC65 ▪ ▪ 55 ▪ ▪ 45		
	–55°C to +125°C — Commercial Screening			
75 ns 65 ns 55 ns		LMU217KM75 ▪ ▪ 65 ▪ ▪ 55		
	–55°C to +125°C — Extended Screening			
75 ns 65 ns 55 ns		LMU217KME75 ▪ ▪ 65 ▪ ▪ 55		
	–55°C to +125°C — MIL-STD-883 Compliant			
75 ns 65 ns 55 ns		LMU217KMB75 ▪ ▪ 65 ▪ ▪ 55		

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