National Semiconductor

DM74ALS169B
Synchronous Four-Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The ALS169B is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

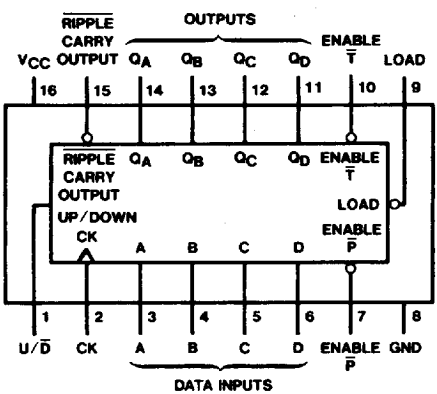
The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- ESD inputs

Connection Diagram

Dual-In-Line Package



TL/F/6207–1

Order Number DM74ALS169BM or 169BN
See NS Package Number M16A or N16A

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	78.1°C/W
M Package	106.8°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74ALS169B			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency		0		40	MHz
t_{SU}	Setup Time	Data; A, B, C, D	15 ↑	6		ns
		$\overline{En}$ P, $\overline{En}$ T	15 ↑	8		ns
		$\overline{Load}$	15 ↑	8		ns
		U/$\overline{D}$	15 ↑	10		ns
t_H	Hold Time	Data; A, B, C, D	0 ↑	−3		ns
		$\overline{En}$ P, $\overline{En}$ T	0 ↑	−3		ns
		$\overline{Load}$	0 ↑	−4		ns
		U/$\overline{D}$	0 ↑	−4		ns
t_W	Width of Clock Pulse		13			ns

Note 1: The symbol (↑) indicates that the rising edge of the clock is used as reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			15	25	mA

6501122 0082881 019

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM74ALS169B		Units
					Min	Max	
f_{MAX}	Max. Clock Freq.				40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Clock	$\overline{\text{Ripple}}$ Carry	3	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	$\overline{\text{Ripple}}$ Carry	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	2	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	$\overline{\text{Ripple}}$ Carry	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	$\overline{\text{Ripple}}$ Carry	3	16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry	5	19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry	5	19	ns

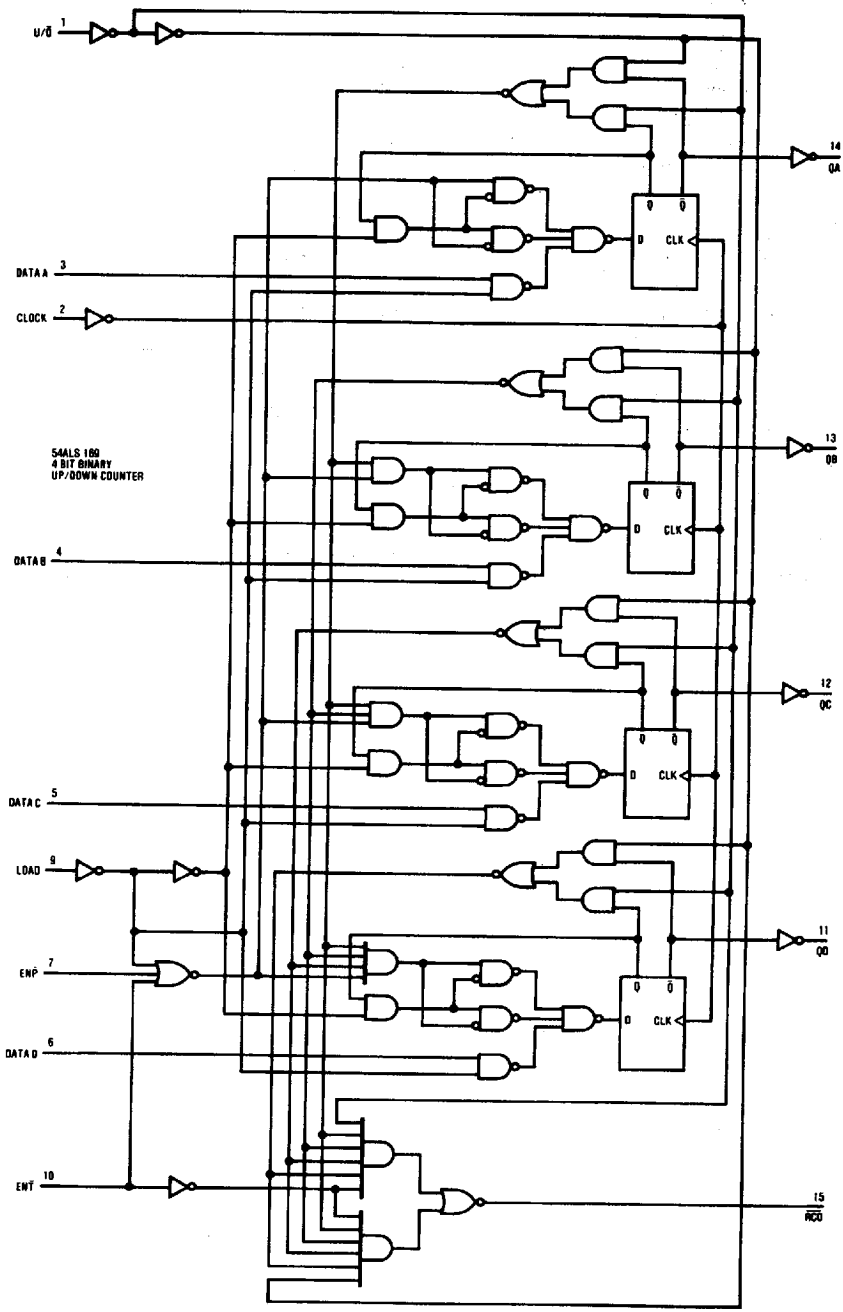
Note 1: See Section 5 for test waveforms and output load.

Note 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for ALS168B or 15 for ALS169B), the ripple carry output will be out of phase.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Logic Diagram

DM74ALS169B



TL/F/6207–3

Powered by ICminer.com Electronic-Library Service CopyRight 2003