intel.

PRELIMINARY

T-49-19-63
T-49-19-61

80C52/80C32
CHMOS SINGLE-CHIP 8-BIT MICROCOMPUTER

80C52—8K Bytes of Factory Mask Programmable ROM
80C32—CPU with RAM and I/O
80C52/80C32—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
80C52-1/80C32-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%

- **Three 16-Bit Timer/Counters**
  - **Timer 2 is an Up/Down Timer/Counter and Capture**
- **Power Off Flag**
- **256 Bytes of On-Chip Data RAM**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **6 Interrupt Sources**
- **Programmable Serial Channel with:**
  - **Framing Error Detection**
  - **Automatic Address Recognition**
- **TTL and CMOS Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS®-51 Fully Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE™ (On-Circuit Emulation) Mode**

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8K bytes of the program memory can reside in the on-chip ROM (80C52 only). In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64K bytes of external data memory.

The Intel 80C52 is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III technology. Being a member of the 8051 family, the 80C52 uses the same powerful instruction set, has the same architecture, and is pin for pin compatible with the existing MCS-51 products. The 80C52 is an enhanced version of the 80C51BH. It's added features make it an even more powerful microcontroller for applications that require up/down counting capabilities such as motor control or a more versatile serial channel to facilitate multi-processor communications.

For the remainder of this document, the 80C52 and 80C32 will be referred to as the 80C52.

July 1989
Order Number: 270757-002

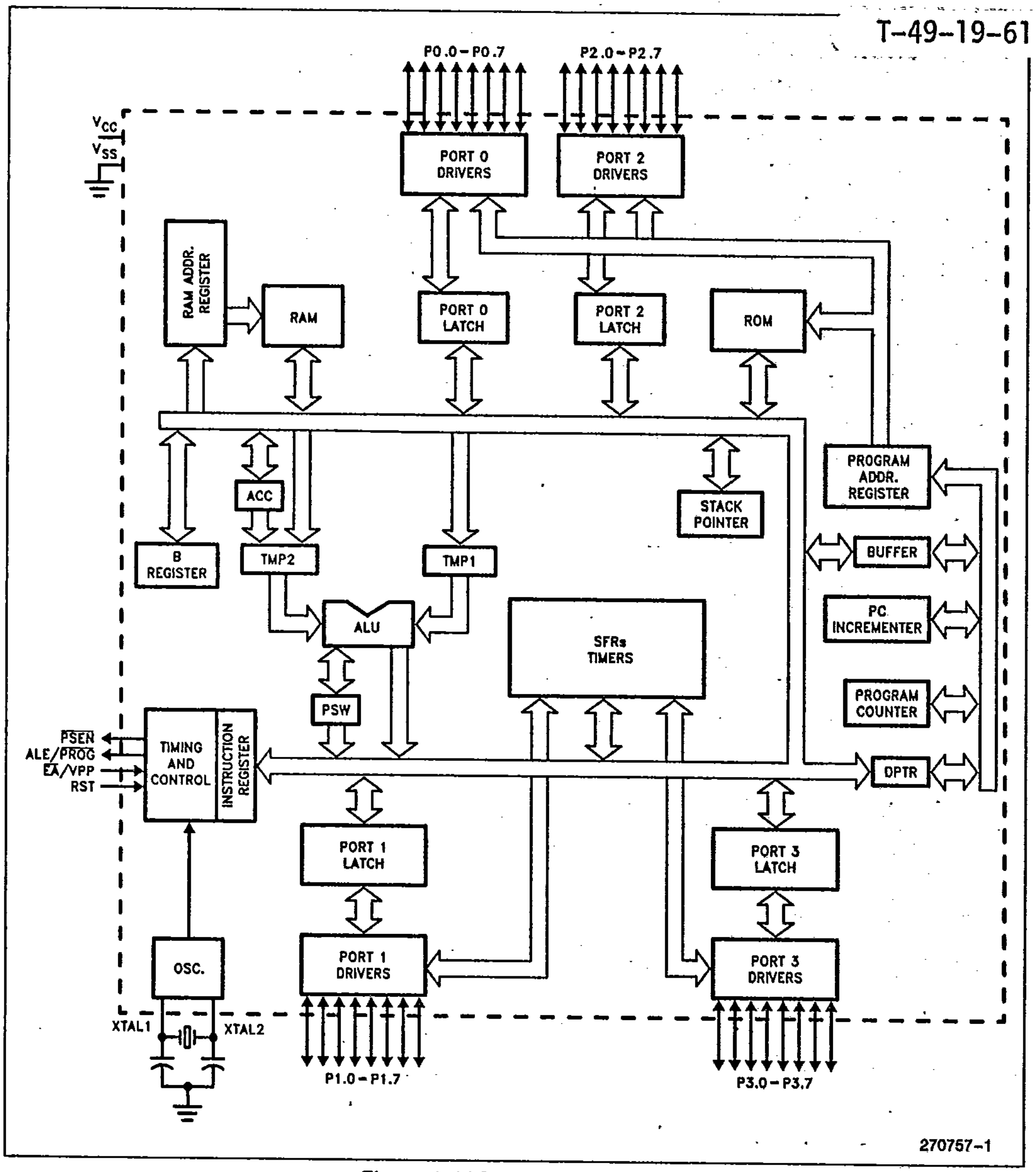

Figure 1. 80C52 Block Diagram

PACKAGES

Part	Prefix	Package Type
80C52	P	40-Pin Plastic DIP
80C32	D	40-Pin CERDIP
	N	44-Pin PLCC

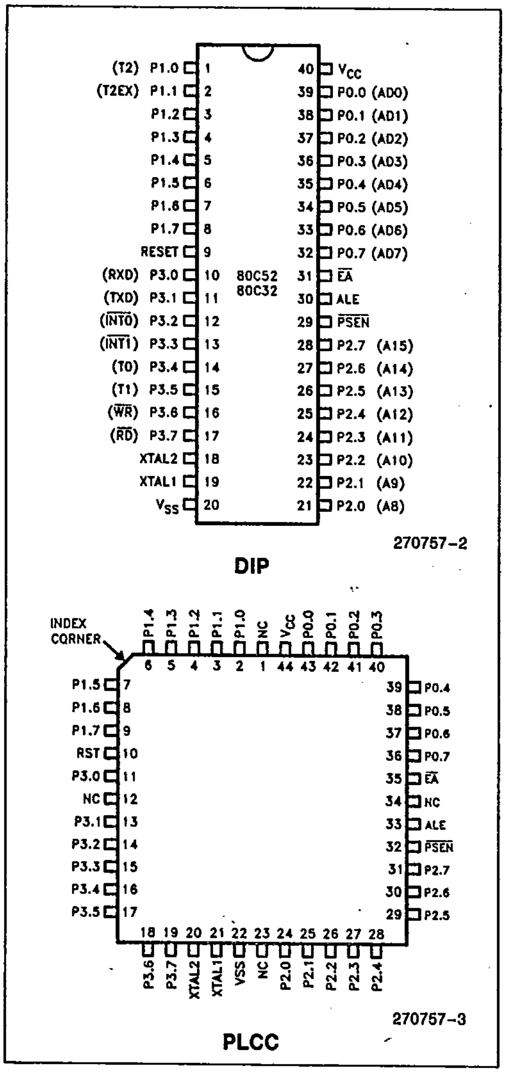

Figure 2. Pin Connections

PIN DESCRIPTIONS

T-49-19-61

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 outputs the code bytes during program verification on the 80C52. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 80C52:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/Counter 2)
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during ROM verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

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Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of ⅙ the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{\text{PSEN}}$: Program Store Enable is the read strobe to external Program Memory.

When the 80C52 is executing code from external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external Data Memory.

$\overline{\text{EA}}/V_{PP}$: External Access enable. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

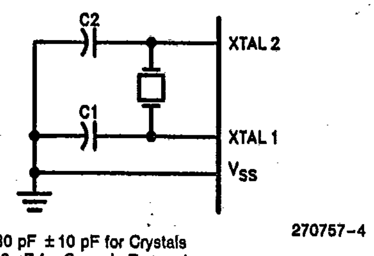
XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.



C1, C2 = 30 pF ±10 pF for Crystals
= 10 pF for Ceramic Resonators

Figure 3. Oscillator Connections

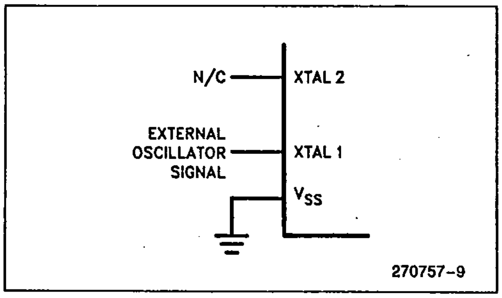


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 80C52 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- Writing to unspecified SFR's (see Table 3) may cause unpredictable operation.

ONCE™ MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 80C52 without the 80C52 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;

2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 80C52 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

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Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Controller Handbook, and Application Note AP-252, "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature ....−65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ....0V to +6.5V
Voltage on Any Other Pin to V_{SS} ..−0.5V to +6.5V
Maximum I_{OL} per I/O Pin ....15 mA
Power Dissipation..........................1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

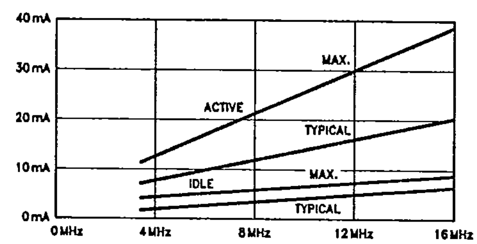
**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS: T_A = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V

Symbol	Parameter	Min	Typical (4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage (5) (Ports 1, 2 and 3, ALE/$\overline{PROG}$, $\overline{PSEN}$)			0.3 0.45 1.0	V V V	I_{OL} = 100 μA I_{OL} = 1.6 mA (1) I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage (5) (Port 0)			0.3 0.45 1.0	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA (1) I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Ports 1, 2 and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	V_{CC}−0.3 V_{CC}−0.7 V_{CC}−1.5			V V V	I_{OH} = −10 μA I_{OH} = −30 μA (2) I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3 V_{CC}−0.7 V_{CC}−1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA (2) I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)		−10	−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)		0.02	±10	μA	0 < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)		−265	−650	μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	40	100	225	KΩ	
CIO	Pin Capacitance		10		pF	(Note 6)
I_{CC}	Power Supply Current: Running at 12 MHz (Figure 5) Idle Mode at 12 MHz (Figure 5) Power Down Mode		 15 5 5	 30 7.5 75	 mA mA μA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pFs, the noise pulse on the ALE signal may exceed 0.8V. In these cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an Address Latch with a Schmitt Trigger Strobe input.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Typicals are based on limited number of samples, and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
6. CIO is the adjacent pin capacitance inherent to the package.



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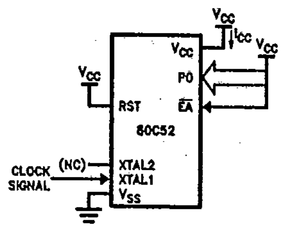
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} MAX = 2.2 × FREQ + 3.1
Idle Mode
I_{CC} MAX = 0.49 × FREQ + 1.6
Where FREQ is in MHz, I_{CC}MAX is given in mA.

Figure 5. I_{CC} vs Frequency



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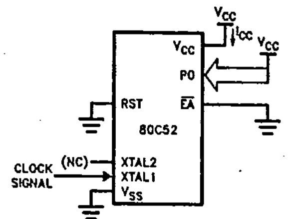
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



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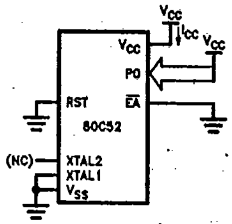
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



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All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode. V_{CC} = 2.0V to 6.0V.

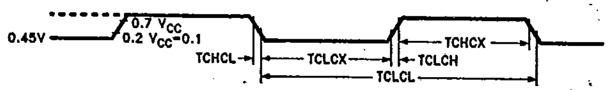

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Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

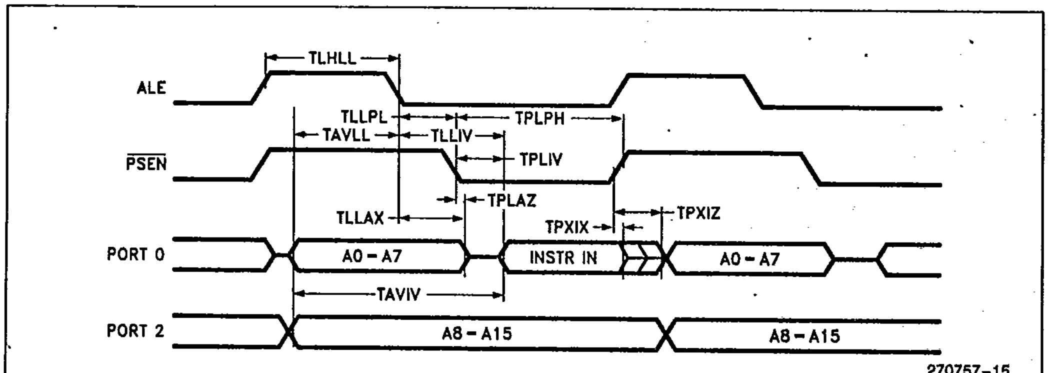
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±20%, V_{SS} = 0V, Load Capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 80C52 80C52-1			 3.5 3.5	 12 16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



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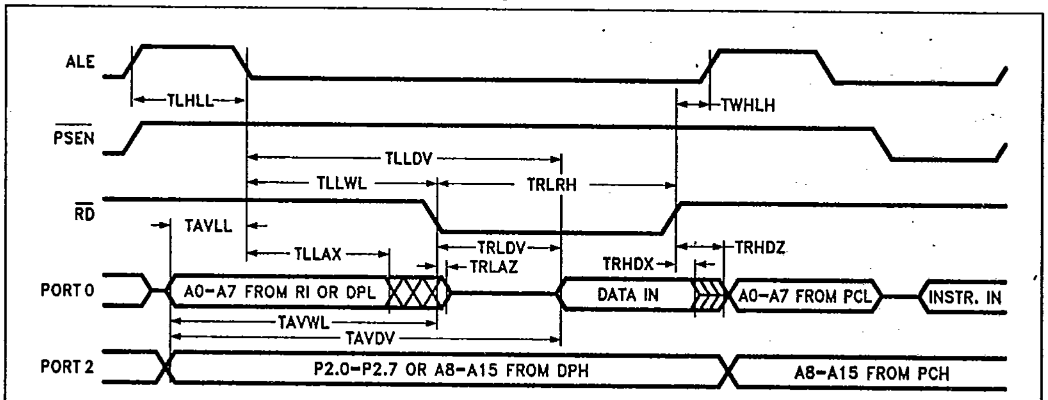
EXTERNAL DATA MEMORY READ CYCLE



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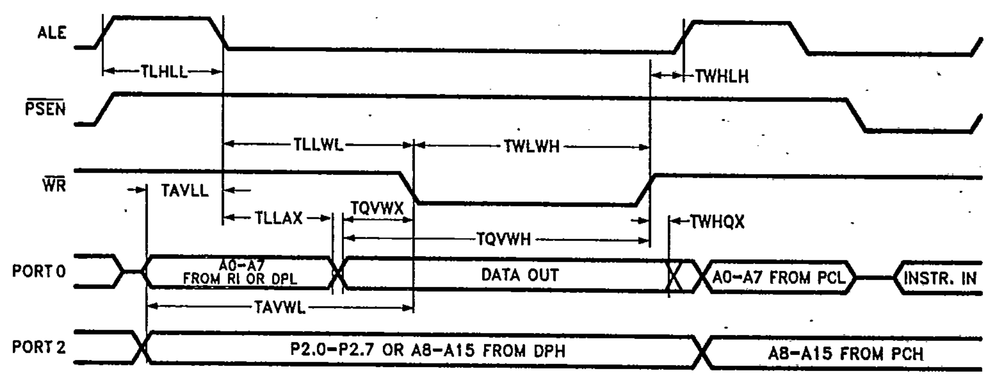
EXTERNAL DATA MEMORY WRITE CYCLE



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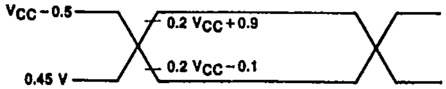
A.C. TESTING INPUT

Input, Output Waveforms



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AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

Float Waveforms

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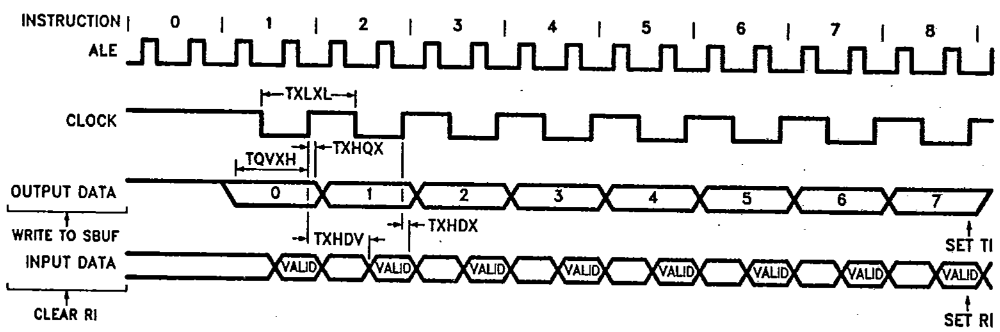
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



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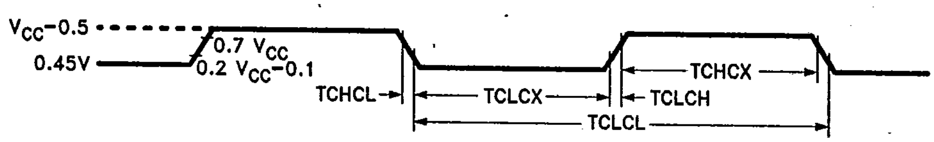
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 80C52/80C32 80C52-1/80C32-1	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



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ROM CHARACTERISTICS

Table 2 shows the logic levels for verifying the code data and reading the signature bytes on the 80C52.

Table 2. ROM Modes

Mode	RST	$\overline{PSEN}$	ALE	$\overline{EA}$	P2.7	P2.6	P3.6	P3.7
Verify Code Data	1	0	1	1	0	0	1	1
Read Signature	1	0	1	1	0	0	0	0

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin

Program Verification

The address of the Program Memory location to be read is applied to Port 1 and pins P2.0–P2.4. The other pins should be held at the "Verify" levels indicated in Table 2. The contents of the addressed locations will come out on Port 0. External pullups are required on Port 0 for this operation.

Figure 10 shows the setup for verifying the program memory.

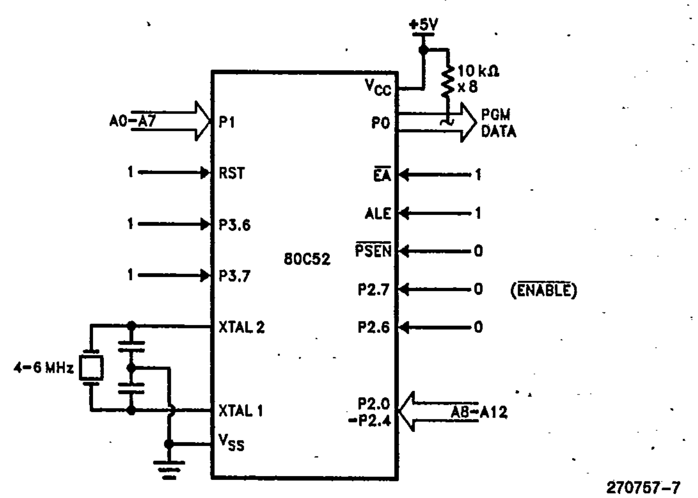

Figure 10. Verifying the ROM

ROM VERIFICATION CHARACTERISTICS

T_A = 21°C to 27°C; V_{CC} = 5V ± 0.25V; V_{SS} = 0V

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	

ROM VERIFICATION WAVEFORMS

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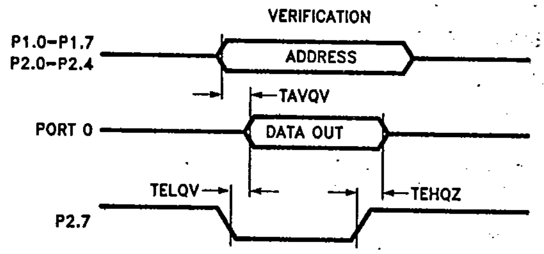

270757-8

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

(030H) = 89H indicates manufacture by Intel
(031H) = 53H indicates 80C52

Table 3. 80C52 Special Function Registers

Address	Name	Reset Value
80H	P0*	11111111B
81H	SP	00000111B
82H	DPL	00000000B
83H	DPH	00000000B
87H	PCON	00XX0000B
88H	TCON*	00000000B
89H	TMOD	00000000B
8AH	TL0	00000000B
8BH	TL1	00000000B
8CH	TH0	00000000B
8DH	TH1	00000000B
90H	P1*	11111111B
98H	SCON*	00000000B
99H	SBUF	XXXXXXXXB
0A0H	P2*	11111111B
0A8H	IE*	00000000B
0A9H	SADDR	00000000B
0B0H	P3*	11111111B
0B8H	IP*	X0000000B
0B9H	SADEN	00000000B
0C8H	T2CON*	00000000B
0C9H	T2MOD	XXXXXXX0B
0CAH	RCAP2L	00000000B
0CBH	RCAP2H	00000000B
0CCH	TL2	00000000B
0CDH	TH2	00000000B
0D0H	PSW*	00000000B
0E0H	ACC*	00000000B
0F0H	B*	00000000B

* = Bit Addressable

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ADVANCE INFORMATION

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80C52/80C32
EXPRESS

80C52/80C32—3.5 MHz to 12 MHz, V_{CC} = 5V ±10%
80C52-1/80C32-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±10%

- **Extended Temperature Range**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

March 1990
Order Number: 270868-001

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)		−75	μA	$V_{In} = 0.45V$
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC} - 1.5$		V	$I_{OH} = -6.0$ mA

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
S	Quad Flat Package	Commercial	No
TS	Quad Flat Package	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-In is dynamic for a minimum time of 168 hours at 125°C, $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

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Examples:

P80C52 indicates 80C52 in a plastic package and specified for commercial temperature range, without burn-in.
LD80C32 indicates 80C32 in a cerdip package and specified for extended temperature range with burn-in.