National Semiconductor

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DM74AS646/DM74AS648
Octal Bus Transceiver and Register

General Description

This device incorporates an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this device with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. It is particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS646, 648 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data, and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable $\overline{G}$ and direction control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal store data transfer to bus A or B.

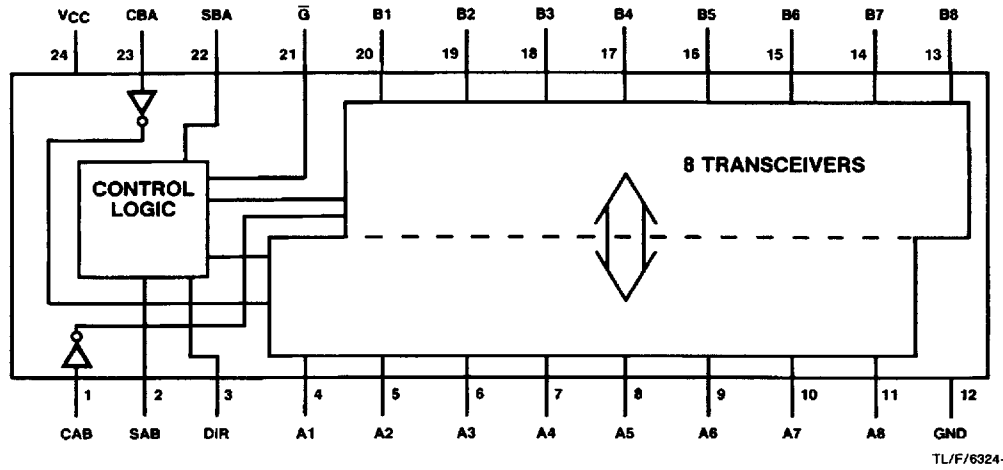
When the enable $\overline{G}$ pin is low, the direction pin selects which bus receives data. When the enable $\overline{G}$ pin is high, both buses become disabled yet their input function is still enabled.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS TTL counterpart
- TRI-STATE® buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



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Order Number DM74AS646NT, DM74AS646WM, DM74AS648NT or DM74AS648WM
See NS Package Number M24B or N24C

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 TL/F/6324 RRD-B30M36/Printed in U. S. A.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	41.1°C/W
M Package	81.5°C/W

Note: This product meets application requirements of 500 temperature cycles from −65°C to +150°C.

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74AS646, 648			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		90	MHz
t_W	Width of Clock Pulse	High	5			ns
		Low	6			ns
t_{SU}	Data Setup Time		6↑			ns
t_H	Data Hold Time		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA					−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, V_{IH} = Min		I_{OH} = Max	2			V
				I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA			V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Min, V_{IH} = 2V, I_{OL} = Max				0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V	V_I = 7V	Control Inputs			0.1	mA
			V_I = 5.5V	A or B Ports			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V (Note 1)		Control Inputs			20	µA
				A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V (Note 1)		Control Inputs			−0.5	mA
				A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V			−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	'AS646	Outputs High		120	195	mA
				Outputs Low		130	211	
				Outputs Disabled		130	211	
			'AS648	Outputs High		110	185	
				Outputs Low		120	195	
				Outputs Disabled		120	195	

Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current, I_{OZH} and I_{OZL}.

'AS646 Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74AS646		Units
					Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 2)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}$	A or B	2	9	ns
t_{PZL}	Output Enable Time to Low Level Output				3	14	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		DIR	A or B	3	16	ns
t_{PZL}	Output Enable Time to Low Level Output				3	18	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	10	ns

Note 1: See Section 5 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

'AS648 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74AS648 Min	DM74AS648 Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CAB or CBA	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 2)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}$	A or B	2	9	ns
t_{PZL}	Output Enable Time to Low Level Output				3	15	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		DIR	A or B	3	16	ns
t_{PZL}	Output Enable Time to Low Level Output				3	18	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	10	ns

Note 1: See Section 5 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Function Table

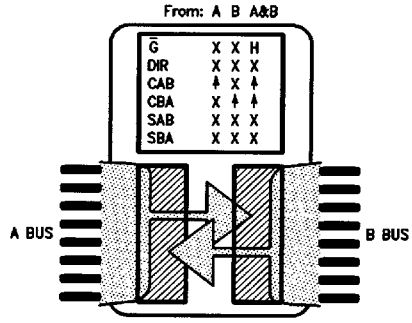
Inputs						Data I/O*		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'AS646	'AS648
H	X	H or L	H or L	X	X	Input	Input	Isolation, Hold Storage	Isolation, Hold Storage
	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus
X	X	↑	X	X	X	Input	Unspecified*	Store A, B Unspecified*	Store A, B Unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A Unspecified*	Store B, A Unspecified*

H—high level; L—low level; X—irrelevant; ↑—low-to-high level transition

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Different Modes of Control for AS646, AS648

Storage From A, B or A and B



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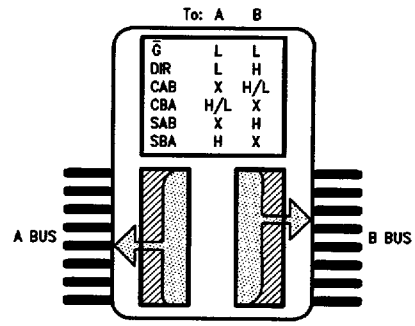
***Transfer Stored Data to A or B**



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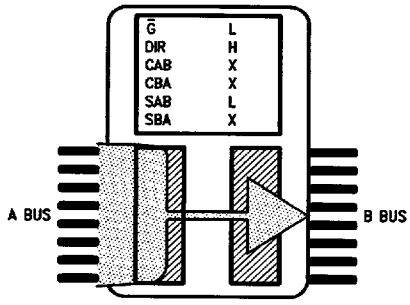
***Real-Time Transfer Bus A to Bus B**



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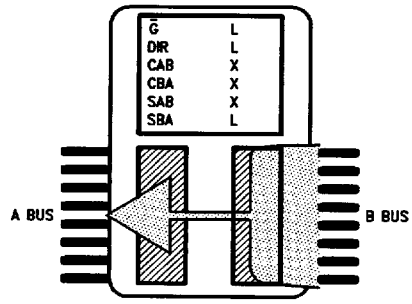
***Real-Time Transfer Bus B to Bus A**



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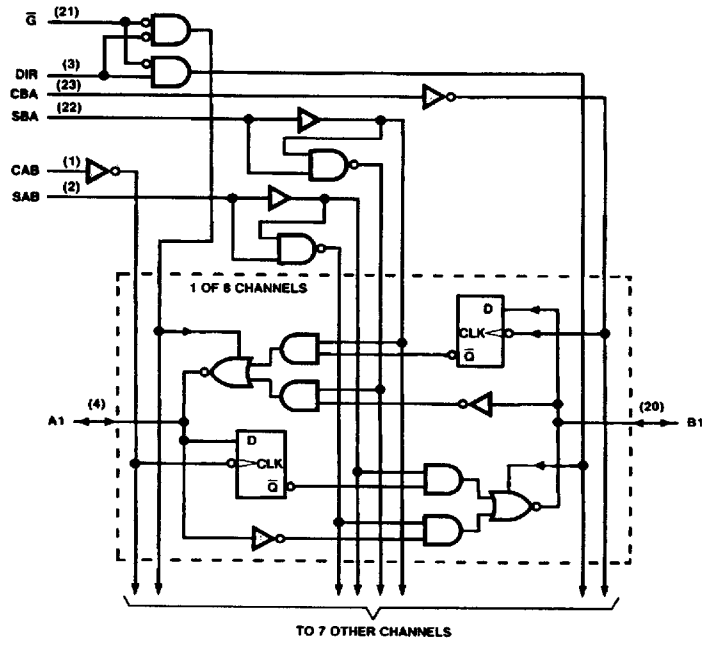
*The complement of A and B data are stored and transferred for AS648

Block Diagram (positive logic)

AS646



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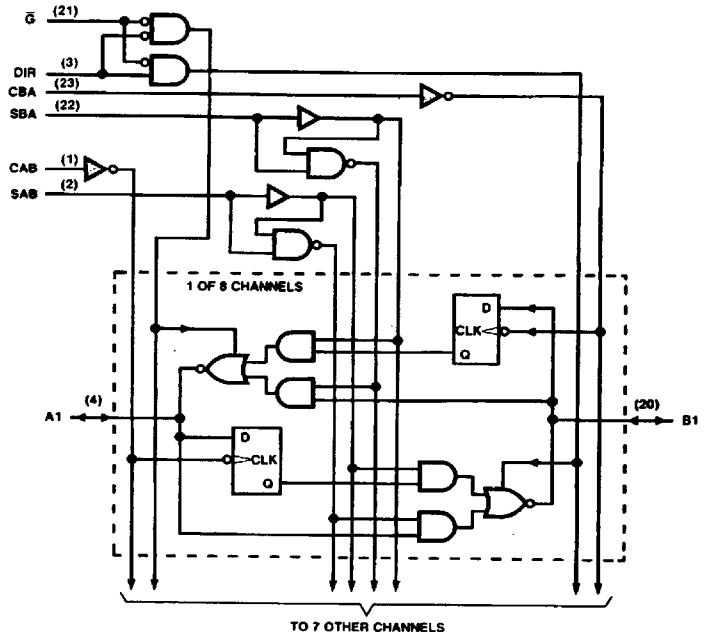
AS648



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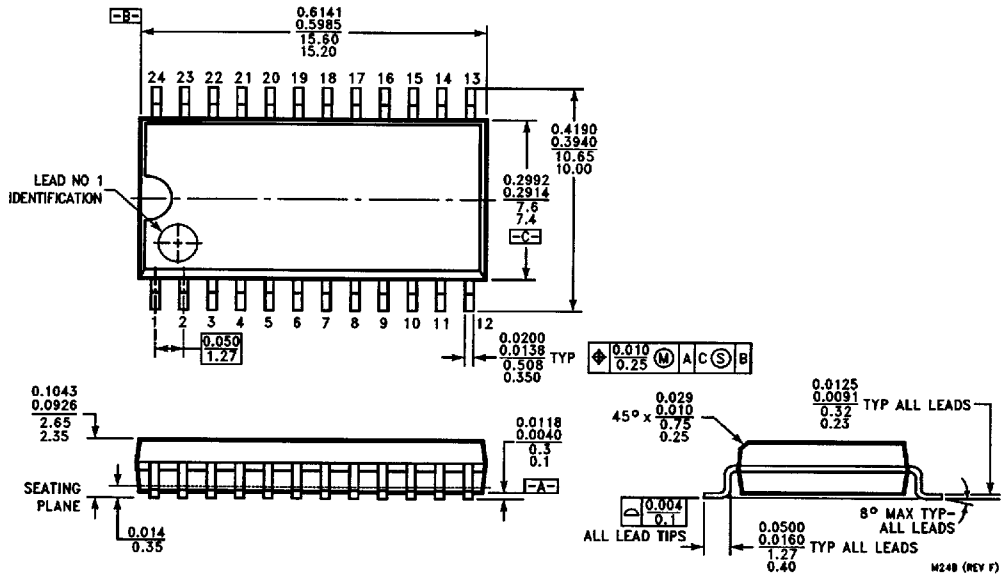
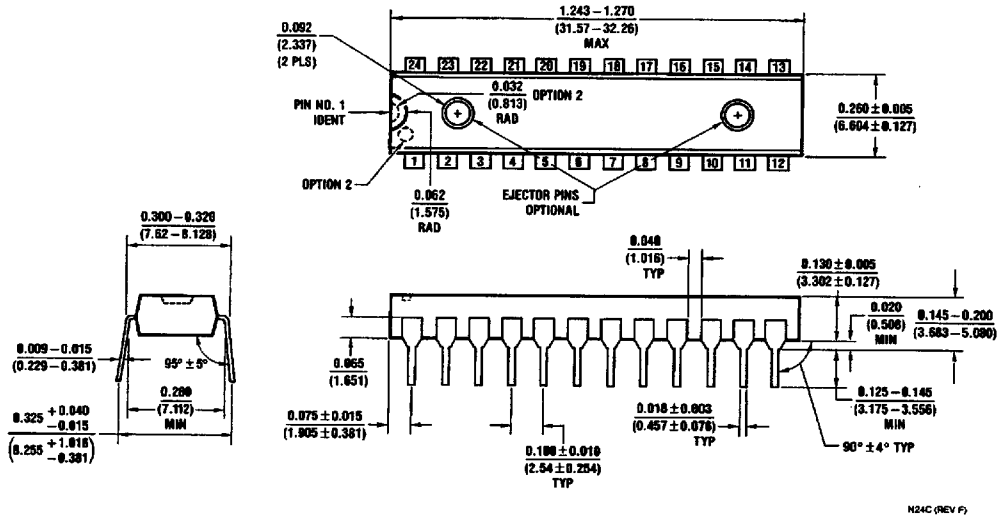
Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (M)
Order Number DM74AS646WM or DM74AS648WM
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number DM74ALS648NT
NS Package Number N24C

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