National Semiconductor

DM74AS74 Dual D Positive-Edge-Triggered Flip-Flop with Preset and Clear

General Description

The AS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

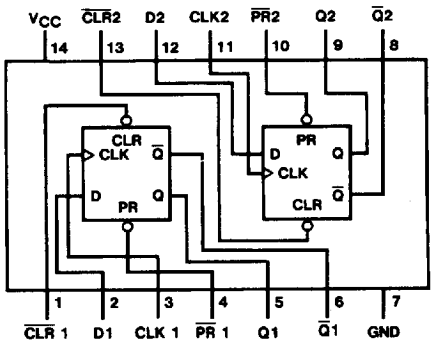
Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over S74 at approximately half the power

Connection Diagram

Dual-In-Line Package



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Order Number DM74AS74M, N
See NS Package Number M14A or N14A

Function Table

Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Q_0 = Previous Condition of Q

* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	76.0°C/W
M Package	107.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLK}	Clock Frequency		0		105	MHz
$t_{W(CLK)}$	Width of Clock Pulse	High	4			ns
		Low	5.5			ns
t_W	Pulse Width Preset & Clear Low		4			ns
t_{SU}	Data Setup Time		4.5 ↑			ns
t_{SU}	PRE or CLR Setup-Time		2 ↑			ns
t_H	Data Hold Time		0 ↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

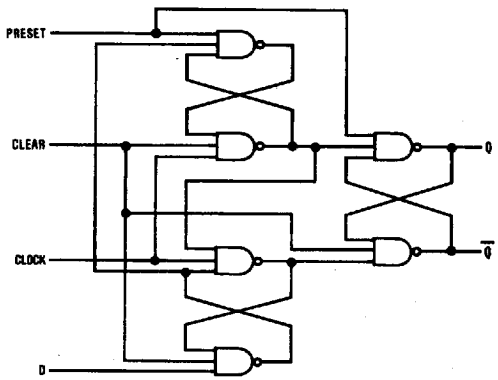
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = Max, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, D			20	μA
			Preset, Clear			40	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, D			−0.5	mA
			Preset, Clear			−1.8	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			10.5	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			105		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Preset or Clear	Q or $\overline{Q}$	3	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset or Clear	Q or $\overline{Q}$	3.5	10.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Q or $\overline{Q}$	3.5	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Q or $\overline{Q}$	4.5	9	ns

Note 1: See Section 5 for test waveforms and output load.

Logic Diagram



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