



DM54S940/DM74S940, DM54S941/DM74S941 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

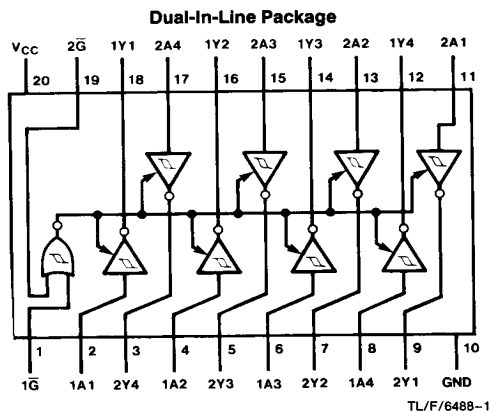
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133Ω.

Features

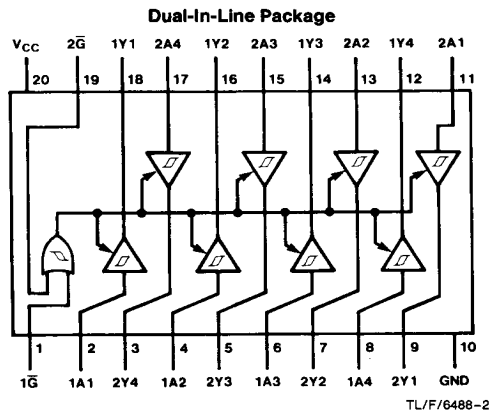
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins

- Typical I_{OL} (sink current)
 - 54S 48 mA
 - 74S 64 mA
- Typical I_{OH} (source current)
 - 54S -12 mA
 - 74S -15 mA
- Typical propagation delay times
 - Inverting 4.5 ns
 - Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
 - Inverting 450 mW
 - Noninverting 538 mW

Connection Diagrams



Order Number DM54S940J or 74S940N
See NS Package Number J20A or N20A



Order Number DM54S941J or 74S941N
See NS Package Number J20A or N20A

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I _{CC}	Supply Current	Outputs High	DM54S940		80	123	mA
			DM74S940		80	135	
			DM54S941		95	147	
			DM74S941		95	160	
		Outputs Low	DM54S940		100	145	
			DM74S940		100	150	
			DM54S941		120	170	
			DM74S941		120	180	
		Outputs Disabled	DM54S940		100	145	
			DM74S940		100	150	
			DM54S941		120	170	
			DM74S941		120	180	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.**Note 2:** Not more than one output should be shorted at a time and duration should not exceed one second.**Switching Characteristics** V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Max	Units
t _{PLH}	Propagation Delay Time Low to High Level Output	C _L = 45 pF R _L = 90Ω	DM54/74S940	2	7	ns
			DM54/74S941	2	9	
t _{PHL}	Propagation Delay Time High to Low Level Output	C _L = 45 pF R _L = 90Ω	DM54/74S940	2	7	ns
			DM54/74S941	2	9	
t _{PZL}	Output Enable Time to Low Level	C _L = 45 pF R _L = 90Ω	DM54/74S940	3	15	ns
			DM54/74S941	3	15	
t _{PZH}	Output Enable Time to High Level	C _L = 45 pF R _L = 90Ω	DM54/74S940	2	10	ns
			DM54/74S941	3	12	
t _{PLZ}	Output Disable Time from Low Level	C _L = 5 pF R _L = 90Ω	DM54/74S940	4	15	ns
			DM54/74S941	2	15	
t _{PHZ}	Output Disable Time from High Level	C _L = 5 pF R _L = 90Ω	DM54/74S940	2	9	ns
			DM54/74S941	2	9	
t _{PLH}	Propagation Delay Time Low to High Level Output	C _L = 150 pF R _L = 90Ω	DM54/74S940	3	10	ns
			DM54/74S941	4	12	
t _{PHL}	Propagation Delay Time High to Low Level Output	C _L = 150 pF R _L = 90Ω	DM54/74S940	3	10	ns
			DM54/74S941	4	12	
t _{PZL}	Output Enable Time to Low Level	C _L = 150 pF R _L = 90Ω	DM54/74S940	6	21	ns
			DM54/74S941	6	21	
t _{PZH}	Output Enable Time to High Level	C _L = 150 pF R _L = 90Ω	DM54/74S940	4	12	ns
			DM54/74S941	4	15	