# TRI-STATE® Quad Buffers

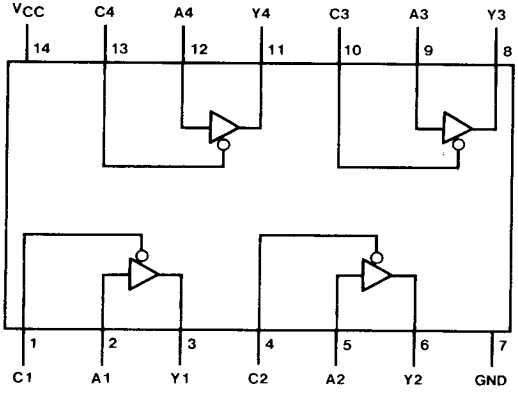
## General Description

The DM7093/DM8093 and DM7094/DM8094 are quad two-input buffers which accept normal TTL or DTL input levels; and have outputs which provide either normal low-impedance TTL characteristics, or a high-impedance third logic state. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state. The other input simple passes the non-inverted data through the buffer. The DM7093/DM8093 provides the high-impedance state when a high logic level is applied to the control input, the DM7094/DM8094 when a low logic level is applied to the control input. The low output inpedance of these devices provides good capacitive-drive capability and rapid transition from the low to the high logic levels, thus assuring both speed and waveform integrity. It is possible to connect as many as 128 devices to a common bus line, and still have adequate drive capability.

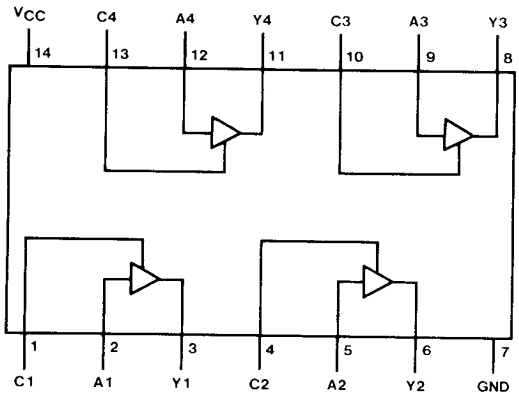
## Features

- Pin equivalent to DM54125/74125 (7093/8093) and DM54126/74126 (7094/8094)
- Up to 128 devices can be connected to a common bus line
- High capacitive-drive capability
- Independent control of each buffer
- Typical propagation delay—12 ns

## Connection Diagrams




7093 (J,W); 8093 (N)




7094 (J,W); 8094 (N)

## Truth Tables

DM7093/DM8093

| Data | Controls | Outputs |
|---|---|---|
| H | L | H |
| L | L | L |
| X | H | Hi-Z |

DM7094/DM8094

| Data | Controls | Outputs |
|---|---|---|
| H | H | H |
| L | H | L |
| X | L | Hi-Z |

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | DM70 93, 94 | | | DM80 93, 94 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ (1) | Max | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ Min, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | −2.0 | | | −5.2 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = Max | 2.4 | 3.4 | | 2.4 | 3.1 | | V |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | V |
| $I_{O(OFF)}$ | Off-State (High Impedance State) Output Current | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_O$ = 0.4 V | | | −40 | | | −40 | μA |
| | | $V_{CC}$ = Max, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_O$ = 2.4 V | | | 40 | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | −30 | | −70 | −28 | | −70 | mA |
| $I_{CCH}$ | Supply Current (Total, Outputs High) | $V_{CC}$ = Max | | 32 | 54 | | 32 | 54 | mA |
| $I_{CCL}$ | Supply Current (Total, Outputs Low) | $V_{CC}$ = Max | | 36 | 62 | | 36 | 62 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | Conditions | DM70/80 93 | | | DM70/80 94 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 50 pF, $R_L$ = 400 Ω | | 10 | 15 | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | | 12 | 18 | | 12 | 18 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 12 | 18 | | 13 | 19 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 16 | 25 | | 16 | 25 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | $C_L$ = 5 pF, $R_L$ = 400 Ω | | 5 | 8 | | 10 | 16 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | | 9 | 14 | | 14 | 20 | ns |

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