TRI-STATE Quad 2-Input NAND Buffers

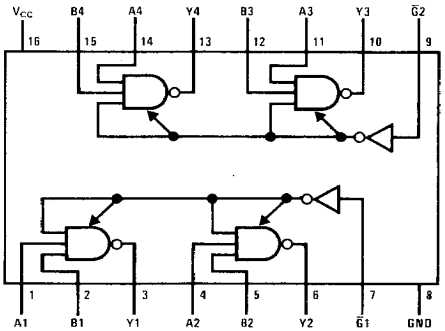
General Description

These devices provide four, two-input NAND buffers in each package. They accept normal TTL or DTL input levels, and have outputs which provide either normal low-impedance TTL characteristics, or a high-impedance third logic state. There are two independent disable lines, each of which controls two gates. When the disable input is taken to a high logic level, the outputs go into the high-impedance state. The low output impedance of these devices provides good capacitive-drive capability and rapid transition from the low to the high logic levels, thus assuring both speed and waveform integrity.

Features

- Combines logic gating with TRI-STATE outputs
- Typical propagation delay 9 ns
- High capacitive-drive capability
- Up to 128 devices can be connected to a common bus line

Connection Diagram



7099/8099(J), (N), (W)

Truth Table

DISABLE	INPUTS		OUTPUT
$\overline{G}$	A	B	Y
L	L	H	H
L	H	L	H
L	L	L	H
L	H	H	L
H	X	X	Hi-Z

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Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS		DM70 99 MIN	DM70 99 TYP(1)	DM70 99 MAX	DM80 99 MIN	DM80 99 TYP(1)	DM80 99 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current						−2.0			−5.2	mA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current						16			16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current		V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
				V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	Either Data Input	V_{CC} = Max	$\overline{G}$ Input at 2V, V_I = 0.4V			−40			−40	μA
		$\overline{G}$ Input		$\overline{G}$ Input at 0.4V, V_I = 0.4V			−1.6			−1.6	mA
				V_I = 0.4V			−1.6			−1.6	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		−25	−70		−25	−70		mA
I_{CC}	Supply Current		V_{CC} = Max				35			35	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM70/80 99 MIN	DM70/80 99 TYP	DM70/80 99 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 400Ω		10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			8	15	ns
t_{ZH}	Output Enable Time to High Level			13	20	ns
t_{ZL}	Output Enable Time to Low Level			13	20	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 400Ω		4	7	ns
t_{LZ}	Output Disable Time from Low Level			11	17	ns

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