TRI-STATE® Data Selectors/Multiplexers

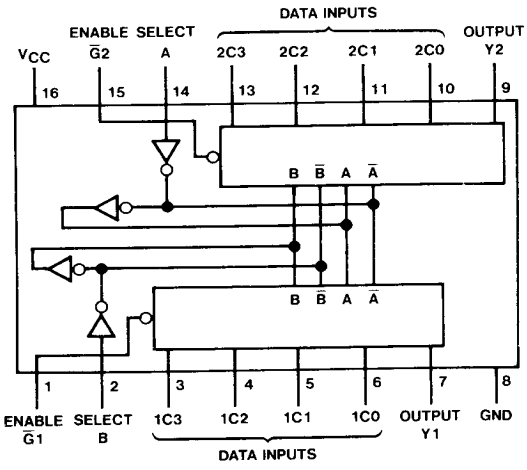
General Description

These devices are the TRI-STATE versions of the very popular DM54153 (DM7214) and DM54150 (DM7219) data selectors/multiplexers. They contain full on-chip decoding to select the desired data input. The DM7214/8214 is a dual, four-line multiplexer, while the DM7219/ 8219 selects one of sixteen input data lines, depending upon the binary number applied to the select inputs. The DM7214/8214 has common select lines, which therefore select the same input line of both multiplexers. However, the two outputs can be individually controlled by means of the separate enable lines; which, when taken to a high logic level, places the output in the high-impedance TRI-STATE condition. The data at the output of the DM7214/8214 is true, whereas the DM7219/8219 is inverted.

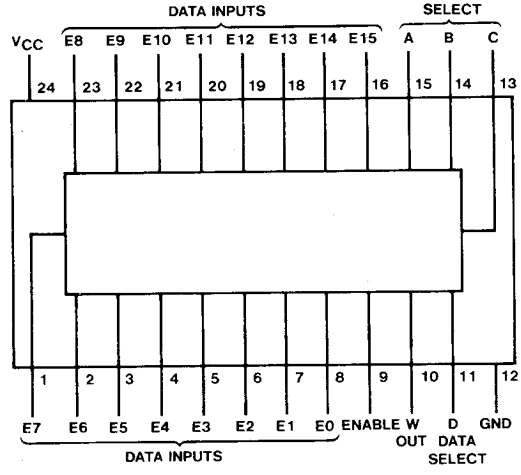
Features

- TRI-STATE pin equivalents to popular 54/74 TTL devices
  - DM7214/8214 — 54153/74153
  - DM7219/8219 — 54150/74150
- Typical propagation delay
  - DM7214/8214 13.5 ns
  - DM7219/8219 11 ns
- Typical power dissipation
  - DM7214/8214 170 mW
  - DM7219/8219 225 mW
- Strobe/enable override

Connection Diagrams



7214 (J,W); 8214 (N)



7219 (J,F); 8219 (N)

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Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM72/82						Units
				14			19			
				Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High Level Output Current		DM72			−2.0			−2.0	mA
			DM82			−5.2			−5.2	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 0.4 V			−40			−40	μA
			V_O = 2.4 V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		−18		−55	−28		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (3)	DM72		34	56		45	68	mA
			DM82		34	65		45	68	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for the DM7219/DM8219 duration of short circuit should not exceed one second.
Note 3: I_{CC} is measured with all inputs grounded.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		From (Input)	To (Output)	Conditions	DM72/82						Units
					14			19			
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 400 Ω		15	23		13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			12	18		9	14	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Output			20	34		21	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Output			20	34		22	33	ns
t_{ZH}	Output Enable Time to High Level	Enable	Output			12	18		15	23	ns
t_{ZL}	Output Enable Time to Low Level	Enable	Output			14	21		17	27	ns
t_{HZ}	Output Disable Time from High Level	Enable	Output	C_L = 5 pF, R_L = 400 Ω		5	10		5	10	ns
t_{LZ}	Output Disable Time from Low Level	Enable	Output			15	23		21	30	ns

Truth Tables

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Select Inputs		Data Inputs				Enable	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Hi-Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

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Select				Enable	Data Inputs														Output
D	C	B	A	$\overline{G}$	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	Y
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hi-Z
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
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H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
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H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

Logic Diagrams

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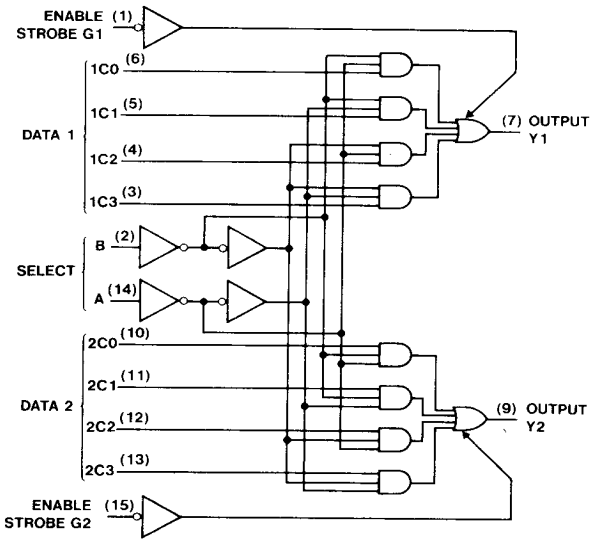

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