National Semiconductor

DM7520/DM8520 Modulo-N Dividers

General Description

Although extremely versatile in a number of applications, the primary uses of these circuits are in two areas:

1. **MODULO-N DIVIDER**
   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.
2. **SHIFT REGISTER**
   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial-out shifting is required.

(Continued)

Features

- Fully programmable divider—any number from 2 to ∞
- Also functions as a four-bit parallel shift register
- Typical propagation delay 36 ns
- Typical power dissipation 250 mW

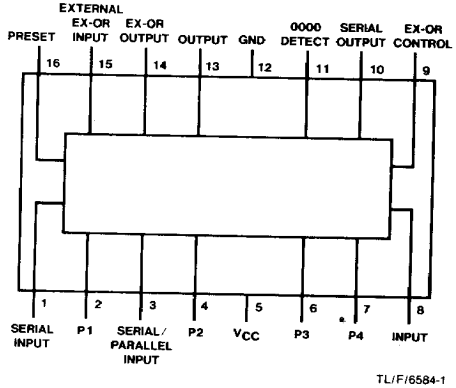
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6584-1

7520 (J) **8520 (N)**

Function Table

Table for Division By N

Setting				÷ BY
P1	P2	P3	P4	
H	H	H	L	2
H	H	L	L	3
H	L	L	L	4
L	L	L	H	5
L	L	H	L	6
L	H	L	L	7
H	L	L	H	8
L	L	H	H	9
L	H	H	L	10
H	H	L	H	11
H	L	H	L	12
L	H	L	H	13
H	L	H	H	14
L	H	H	H	15

General Description (Continued)

THEORY OF OPERATION

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed, the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is $2^n - 1$, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence this state is detected, and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16 m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidentally set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

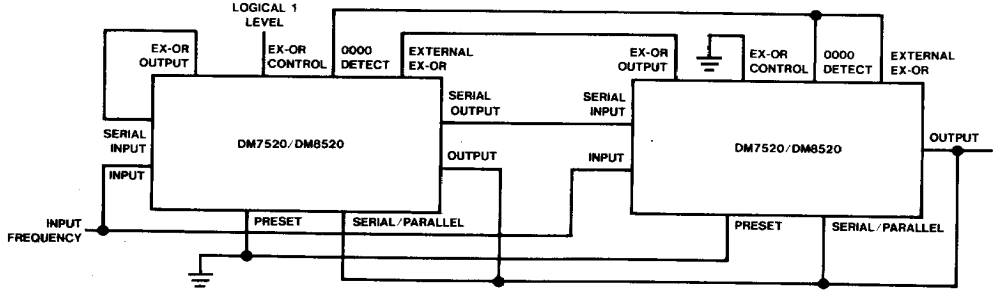
To summarize, the following connections should be made for operation of a single DM7520/DM8520.

Ex-Or Output to Serial Input
0000 Detect to External Ex-Or Input
Output to Serial/Parallel Input
Preset to Ground
Ex-Or Control to Ground

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs, thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255.

To divide by numbers between 16 and 255, the table in *Figure 2* will apply.



TL/F/6584-2

FIGURE 1. Connection for 2 Dividers for Maximum Frequency Division of 255

General Description (Continued)

Setting										Setting										Setting									
Divider 1				Divider 2				By		Divider 1				Divider 2				By		Divider 1				Divider 2				By	
P1	P2	P3	P4	P1	P2	P3	P4			P1	P2	P3	P4	P1	P2	P3	P4			P1	P2	P3	P4	P1	P2	P3	P4		
L	H	H	H	H	H	H	H	255		H	L	L	L	H	L	L	H	195		L	L	H	H	H	L	L	H	135	
H	L	H	H	H	H	H	H	254		H	H	L	L	L	H	L	L	194		H	L	L	H	H	H	L	L	134	
L	H	L	H	H	H	H	H	253		H	H	H	L	L	L	H	L	193		L	H	L	L	H	H	H	L	133	
L	L	H	L	H	H	H	H	252		L	H	H	H	L	L	L	H	192		H	L	H	L	L	H	H	H	132	
H	L	L	H	L	H	H	H	251		L	L	H	H	H	L	L	L	191		H	H	L	H	L	L	H	H	131	
L	H	L	L	H	L	H	H	250		L	L	L	H	H	H	L	L	190		L	H	H	L	H	L	L	H	130	
L	L	H	L	L	H	L	H	249		H	L	L	L	H	H	H	L	189		H	L	H	H	L	H	L	L	129	
L	L	L	H	L	L	H	L	248		L	H	L	L	L	H	H	H	188		L	H	L	H	H	L	H	L	128	
L	L	L	L	H	L	L	H	247		H	L	H	L	L	L	H	H	187		H	L	H	L	H	H	L	H	127	
L	L	L	L	L	H	L	L	246		H	H	L	H	L	L	L	H	186		L	H	L	H	L	H	H	L	126	
L	L	L	L	L	L	H	L	245		L	H	H	L	H	L	L	L	185		L	L	H	L	H	L	H	H	125	
L	L	L	L	L	L	L	H	244		L	L	H	H	L	H	L	L	184		H	L	L	H	L	H	L	H	124	
H	L	L	L	L	L	L	L	243		H	L	L	H	H	L	H	L	183		L	H	L	L	H	L	H	L	123	
H	H	L	L	L	L	L	L	242		L	H	L	L	H	H	L	H	182		H	L	H	L	L	H	L	H	122	
H	H	H	L	L	L	L	L	241		L	L	H	L	L	H	H	L	181		H	H	L	H	L	L	H	L	121	
L	H	H	H	L	L	L	L	240		H	L	L	H	L	L	H	H	180		H	H	H	L	H	L	L	H	120	
H	L	H	H	H	L	L	L	239		L	H	L	L	H	L	L	H	179		L	H	H	H	L	H	L	L	119	
H	H	L	H	H	H	L	L	238		L	L	H	L	L	H	L	L	178		H	L	H	H	H	L	H	L	118	
L	H	H	L	H	H	H	L	237		H	L	L	H	L	L	H	L	177		H	H	L	H	H	H	L	H	117	
L	L	H	H	L	H	H	H	236		H	H	L	L	H	L	L	H	176		H	H	H	L	H	H	H	L	116	
L	L	L	H	H	L	H	H	235		H	H	H	L	L	H	L	L	175		H	H	H	H	L	H	H	H	115	
L	L	L	L	H	H	L	H	234		L	H	H	H	L	L	H	L	174		H	H	H	H	H	L	H	H	114	
L	L	L	L	L	H	H	L	233		H	L	H	H	H	L	L	H	173		L	H	H	H	H	H	L	H	113	
L	L	L	L	L	L	H	H	232		L	H	L	H	H	H	L	L	172		H	L	H	H	H	H	H	L	112	
H	L	L	L	L	L	L	H	231		H	L	H	L	H	H	H	L	171		H	H	L	H	H	H	H	H	111	
L	H	L	L	L	L	L	L	230		H	H	L	H	L	H	H	H	170		H	H	H	L	H	H	H	H	110	
L	L	H	L	L	L	L	L	229		L	H	H	L	H	L	H	H	169		L	H	H	H	L	H	H	H	109	
H	L	L	H	L	L	L	L	228		H	L	H	H	L	H	L	H	168		L	L	H	H	H	L	H	H	108	
H	H	L	L	H	L	L	L	227		H	H	L	H	H	L	H	L	167		H	L	L	H	H	H	L	H	107	
L	H	H	L	L	H	L	L	226		L	H	H	L	H	H	L	H	166		H	H	L	L	H	H	H	L	106	
H	L	H	H	L	L	H	L	225		H	L	H	H	L	H	H	L	165		L	H	H	L	L	H	H	H	105	
L	H	L	H	H	L	L	H	224		L	H	L	H	H	L	H	H	164		L	L	H	H	L	L	H	H	104	
L	L	H	L	H	H	L	L	223		L	L	H	L	H	H	L	H	163		L	L	L	H	H	L	L	H	103	
L	L	L	H	L	H	H	L	222		H	L	L	H	L	H	H	L	162		L	L	L	L	H	H	L	L	102	
L	L	L	L	H	L	H	H	221		H	H	L	L	H	L	H	H	161		H	L	L	L	L	H	H	L	101	
L	L	L	L	L	H	L	H	220		H	H	H	L	L	H	L	H	160		H	H	L	L	L	L	H	H	100	
H	L	L	L	L	L	H	L	219		H	H	H	H	L	L	H	L	159		L	H	H	L	L	L	L	H	99	
H	H	L	L	L	L	L	H	218		L	H	H	H	H	L	L	H	158		L	L	H	H	L	L	L	L	98	
L	H	H	L	L	L	L	L	217		H	L	H	H	H	H	L	L	157		H	L	L	H	H	L	L	L	97	
H	L	H	H	L	L	L	L	216		H	H	L	H	H	H	H	L	156		L	H	L	L	H	H	L	L	96	
L	H	L	H	H	L	L	L	215		L	H	H	L	H	H	H	H	155		H	L	H	L	L	H	H	L	95	
H	L	H	L	H	H	L	L	214		H	L	H	H	L	H	H	H	154		L	H	L	H	L	L	H	H	94	
H	H	L	H	L	H	H	L	213		H	H	L	H	H	L	H	H	153		H	L	H	L	H	L	L	H	93	
H	H	H	L	H	L	H	H	212		H	H	H	L	H	H	L	H	152		L	H	L	H	L	H	L	L	92	
L	H	H	H	L	H	L	H	211		L	H	H	H	L	H	H	L	151		L	L	H	L	H	L	H	L	91	
L	L	H	H	H	L	H	L	210		H	L	H	H	H	L	H	H	150		L	L	L	H	L	H	L	H	90	
L	L	L	H	H	H	L	H	209		L	H	L	H	H	H	L	H	149		H	L	L	L	H	L	H	L	89	
L	L	L	L	H	H	H	L	208		L	L	H	L	H	H	H	L	148		L	H	L	L	L	H	L	H	88	
H	L	L	L	L	H	H	H	207		L	L	L	H	L	H	H	H	147		H	L	H	L	L	L	H	L	87	
L	H	L	L	L	L	H	H	206		H	L	L	L	H	L	H	H	146		L	H	L	H	L	L	L	H	86	
H	L	H	L	L	L	L	H	205		H	H	L	L	L	H	L	H	145		H	L	H	L	H	L	L	L	85	
H	H	L	H	L	L	L	L	204		L	H	H	L	L	L	H	L	144		H	H	L	H	L	H	L	L	84	
H	H	H	L	H	L	L	L	203		H	L	H	H	L	L	L	H	143		H	H	H	L	H	L	H	L	83	
H	H	H	H	L	H	L	L	202		H	H	L	H	H	L	L	L	142		H	H	H	H	L	H	L	H	82	
L	H	H	H	H	L	H	L	201		L	H	H	L	H	H	L	L	141		H	H	H	H	H	L	H	L	81	
L	L	H	H	H	H	L	H	200		L	L	H	H	L	H	H	L	140		H	H	H	H	H	H	L	H	80	
H	L	L	H	H	H	H	L	199		H	L	L	H	H	L	H	H	139		L	H	H	H	H	H	H	L	79	
L	H	L	L	H	H	H	H	198		H	H	L	L	H	H	L	H	138		L	L	H	H	H	H	H	H	78	
L	L	H	L	L	H	H	H	197		H	H	H	L	L	H	H	L	137		H	L	L	H	H	H	H	H	77	
L	L	L	H	L	L	H	H	196		L	H	H	H	L	L	H	H	136		H	H	L	L	H	H	H	H	76	

FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations)

General Description (Continued)

Setting									Setting									Setting								
Divider 1				Divider 2				By	Divider 1				Divider 2				By	Divider 1				Divider 2				By
P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4	
H	H	H	L	L	H	H	H	75	L	L	H	H	H	H	L	L	50	L	H	H	L	L	H	H	L	25
H	H	H	H	L	L	H	H	74	L	L	L	H	H	H	H	L	49	H	L	H	H	L	L	H	H	24
H	H	H	H	H	L	L	H	73	H	L	L	L	H	H	H	H	48	H	H	L	H	H	L	L	H	23
L	H	H	H	H	H	L	L	72	H	H	L	L	L	H	H	H	47	H	H	H	L	H	H	L	L	22
L	L	H	H	H	H	H	L	71	L	H	H	L	L	L	H	H	46	H	H	H	H	L	H	H	L	21
L	L	L	H	H	H	H	H	70	L	L	H	H	L	L	L	H	45	L	H	H	H	H	L	H	H	20
L	L	L	L	H	H	H	H	69	L	L	L	H	H	L	L	L	44	H	L	H	H	H	H	L	H	19
L	L	L	L	L	H	H	H	68	H	L	L	L	H	H	L	L	43	L	H	L	H	H	H	H	L	18
H	L	L	L	L	L	H	H	67	L	H	L	L	L	H	H	L	42	H	L	H	L	H	H	H	H	17
L	H	L	L	L	L	L	H	66	L	L	H	L	L	L	H	H	41	L	H	L	H	L	H	H	H	16
H	L	H	L	L	L	L	L	65	L	L	L	H	L	L	L	H	40	H	L	H	L	H	L	H	H	15
L	H	L	H	L	L	L	L	64	H	L	L	L	H	L	L	L	39	L	H	L	H	L	H	L	H	14
L	L	H	L	H	L	L	L	63	L	H	L	L	L	H	L	L	38	H	L	H	L	H	L	H	L	13
L	L	L	H	L	H	L	L	62	L	L	H	L	L	L	H	L	37	H	H	L	H	L	H	L	H	12
L	L	L	L	H	L	H	L	61	H	L	L	H	L	L	L	H	36	L	H	H	L	H	L	H	L	11
H	L	L	L	L	H	L	H	60	L	H	L	L	H	L	L	L	35	L	L	H	H	L	H	L	H	10
L	H	L	L	L	L	H	L	59	H	L	H	L	L	H	L	L	34	L	L	L	H	H	L	H	L	9
L	L	H	L	L	L	L	H	58	L	H	L	H	L	L	H	L	33	H	L	L	L	H	H	L	H	8
L	L	L	H	L	L	L	L	57	L	L	H	L	H	L	L	H	32	H	H	L	L	L	H	H	L	7
L	L	L	L	H	L	L	L	56	H	L	L	H	L	H	L	L	31	H	H	H	L	L	L	H	H	6
H	L	L	L	L	H	L	L	55	H	H	L	L	H	L	H	L	30	H	H	H	H	L	L	L	H	5
H	H	L	L	L	L	H	L	54	L	H	H	L	L	H	L	H	29	H	H	H	H	H	L	L	L	4
H	H	H	L	L	L	L	H	53	L	L	H	H	L	L	H	L	28	H	H	H	H	H	H	L	L	3
H	H	H	H	L	L	L	L	52	H	L	L	H	H	L	L	H	27	H	H	H	H	H	H	H	L	2
L	H	H	H	H	L	L	L	51	H	H	L	L	H	H	L	L	26									

FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations)

Recommended Operating Conditions

Symbol	Parameter	DM7520			DM8520			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
f_{CLK}	Clock Frequency	0		15	0		15	MHz
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	EX-OR			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	EX-OR			−3.2	mA
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−20		−55	mA
			DM85	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max			50	75	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 100Ω			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PLH} Propagation Delay Time Low to High Level Output			35	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output			38	55	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Logic Diagram

75/8520